Renesas Electronics America Inc - R5F51137ADFM#30 Datasheet

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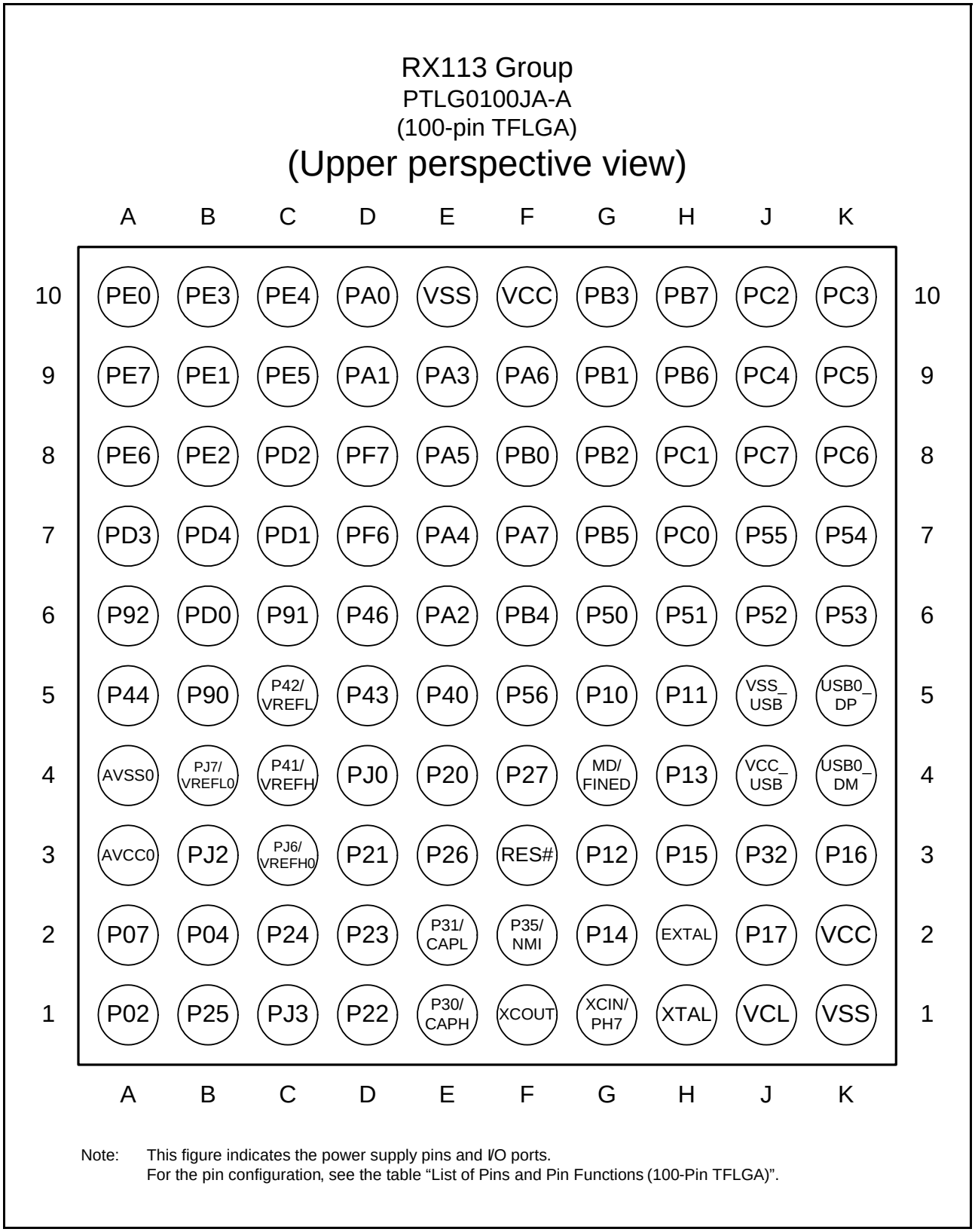
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51137adfm-30

Table 1.2 Comparison of Functions for Different Packages

Module/Functions		RX113 Group	
		100 Pins	64 Pins
Interrupts	External interrupts	NMI, IRQ0 to IRQ7	
DMA	Data transfer controller	Supported	
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)	
	Port output enable 2	Supported	
	Compare match timer	2 channels × 2 units	
	Realtime clock	Supported	
	Low power timer	1 channel	
	8-bit timer	2 channels × 2 units	
	Independent watchdog timer	Supported	
Communication functions	Serial communications interfaces (SCIe) [simple I²C, simple SPI]	7 channels (SCI0, 1, 2, 5, 6, 8, 9)	5 channels (SCI1, 5, 6, 8, 9)
	IrDA interface	1 channel (SCI5)	
	Serial communications interface (SCIf) [simple I²C, simple SPI]	1 channel (SCI12)	
	I²C bus interface	1 channel	
	Serial peripheral interface	1 channel	
	USB 2.0 host/function module (USBc)	1 channel	
	Serial sound interface	1 channel	
12-bit A/D converter (including high-precision channels)		17 channels (9 channels)	11 channels (3 channels)
Temperature sensor		Supported	
Comparator B		2 channels	
12-bit D/A converter		2 channels	
CRC calculator		Supported	
Event link controller		Supported	
Capacitive touch sensing unit		12 channels	Not supported
LCD		40 SEG × 4 COM 36 SEG × 8 COM	20 SEG × 4 COM 16 SEG × 8 COM
Packages		100-pin LFQFP 100-pin TFLGA	64-pin LFQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin TFLGA)”.

Figure 1.4 Pin Assignments of the 100-Pin TFLGA

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
1		P04	MTIOC0A/POE2#/TMCI3	SCK6	TS1	
2		PJ0				DA0
3		P02	MTIOC0D/POE3#/TMRI3	RXD6/SMISO6/SSCL6	TS2	
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	TS3	
5		P25	MTIOC4C/MTCLKB		TS4	ADTRG0#
6		P24	MTIOC4A/MTCLKA/ TMRI1		TS5	
7		P23	MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	TS6	
8		P22	MTIOC3B/MTCLKC/ TMO0	SCK0	TS7	
9		P21	MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0	TS8	
10		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	TS9	
11		P27	MTIOC2B/TMCI3	SCK12/SCK1/RXD6/SMISO6/ SSCL6	TS10	IRQ3/ADTRG0#/ CACREF/ CMPA2
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/TXD6/SMOSI6/ SSDA6	TSCAP	
13		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	CAPH	IRQ0
14		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	CAPL	IRQ1
15	MD					FINED
16	RES#					
17	XCOUT					
18	XCIN	PH7				
19	UPSEL	P35				NMI
20	XTAL					
21	EXTAL					
22	VCL					
23	VSS					
24	VDD					
25		P32	MTIOC0C/RTCOUT/ TMO3	TXD6/SMOSI6/SSDA6/CTS6#/ RTS6#/SS6#	TS11	IRQ2
26		P17	MTIOC0C/MTIOC3A/ MTIOC3B/POE8#/TMO1	SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12		IRQ7
27		P16	MTIOC3C/MTIOC3D/ RTCOUT/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
28		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1/RSPCKA		IRQ5/CLKOUT/ CACREF
29	UB#	P14	MTIOC0A/MTIOC3A/ MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/SSLA0/ TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/USB0_OVRCURA		IRQ4
30	VCC_USB					
31				USB0_DM		
32				USB0_DP		
33	VSS_USB					
34		P13	MTIOC0B/TMO3	CTS12#/RTS12#/SS12#/CTS0#/ RTS0#/SS0#	SEG00	IRQ3
35		P12	TMCI1	SCK12/SCK0	SEG01	IRQ2

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
D9		PA1	MTIOC0B/MTCLKC/ RTCOUT	SCK5/SSLA2	SEG23	
D10		PA0	MTIOC4A	SSLA1	SEG24	CACREF
E1		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	CAPH	IRQ0
E2		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	CAPL	IRQ1
E3		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/TXD6/SMOSI6/ SSDA6	TSCAP	
E4		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0	TS9	
E5		P40*2				AN000
E6		PA2		RXD5/SMISO5/SSCL5/IRRXD5/ SSLA3	SEG22	
E7		PA4	MTIOC2B/MTIC5U/ MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/IRTXD5/ SSLA0/CTS8#/RTS8#/SS8#	SEG20	IRQ5/CVREFB1
E8		PA5		SCK8	SEG19	
E9		PA3	MTIOC0D/MTIOC1B/ MTCLKD/POE0#	RXD5/SMISO5/SSCL5/IRRXD5/ MISOA	SEG21	IRQ6/CMPB1
E10	VSS					
F1	XCOUT					
F2	UPSEL	P35				NMI
F3	RES#					
F4		P27	MTIOC2B/TMCI3	SCK12/SCK1/RXD6/SMISO6/ SSCL6	TS10	IRQ3/ ADTRG0#/ CACREF/ CMPA2
F5		P56	MTIOC1A/MTIC5W/ POE2#	TXD1/SMOSI1/SSDA1	SEG4	IRQ5
F6		PB4		CTS9#/RTS9#/SS9#	SEG14	
F7		PA7		TXD8/SMOSI8/SSDA8	SEG18	
F8		PB0	MTIOC0C/MTIC5W/ RTCOUT	SCL0/RSPCKA/RXD6/SMISO6/ SSCL6		IRQ2/ADTRG0#
F9		PA6	MTIC5V/MTCLKB/ MTIOC2A/POE2#/TMCI3	CTS5#/RTS5#/SS5#/SDA0/MOSIA/ RXD8/SMISO8/SSCL8		IRQ3
F10	VCC					
G1	XCIN	PH7				
G2	UB#	P14	MTIOC0A/MTIOC3A/ MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/SSLA0/ TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/USB0_OVRCURA		IRQ4
G3		P12	TMCI1	SCK12/SCK0	SEG01	IRQ2
G4	MD					FINED
G5		P10	MTIC5V/POE1#	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/TXD0/SMOSI0/SSDA0	SEG03	IRQ6
G6		P50	MTIOC2A	MOSIA/TXD2/SMOSI2/SSDA2	SEG08	
G7		PB5	MTIOC1B/MTIOC2A/ POE1#/TMRI1	SCK9/SSISCK0	SEG13/ COM6	
G8		PB2		CTS6#/RTS6#/SS6#	SEG16	
G9		PB1	MTIOC0C/MTIOC4C/ TMCI0	TXD6/SMOSI6/SSDA6/SSIWS0	SEG17	IRQ4
G10		PB3	MTIOC0A/MTIOC3B/ MTIOC4A/POE3#/TMO0	SCK6/AUDIO_MCLK/ USB0_OVRCURA	SEG15/ COM7	

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
H1	XTAL					
H2	EXTAL					
H3		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1/RSPCKA		IRQ5/CLKOUT/ CACREF
H4		P13	MTIOC0B/TMO3	CTS12#/RTS12#/SS12#/CTS0#/ RTS0#/SS0#	SEG00	IRQ3
H5		P11	MTIC5U/POE0#	RXD12/RXDX12/SMISO12/ SSCL12/RXD0/SMISO0/SSCL0	SEG02	IRQ7
H6		P51	MTIOC4C	RSPCKA/SCK2	SEG07	
H7		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	SEG10	
H8		PC1	MTIOC3A	SCK5/SSLA2	SEG09	
H9		PB6	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/ COM5	
H10		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9/SSITXD0	SEG11/ COM4	
J1	VCL					
J2		P17	MTIOC0C/MTIOC3A/ MTIOC3B/POE8#/TMO1	SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12		IRQ7
J3		P32	MTIOC0C/RTCOUT/ TMO3	TXD6/SMOSI6/SSDA6/CTS6#/ RTS6#/SS6#	TS11	IRQ2
J4	VCC_USB					
J5	VSS_USB					
J6		P52		MISOA/RXD2/SMISO2/SSCL2	SEG06	
J7		P55	MTIOC4D/TMO3		VL1	
J8		PC7	MTIOC3A/MTCLKB/ TMO2	TXD1/SMOSI1/SSDA1/MISOA/ TXD8/SMOSI8/SSDA8/ USB0_OVRCURB	VL3	CACREF
J9		PC4	MTIOC3D/MTCLKC/ POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/ USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
J10		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
K1	VSS					
K2	VDD					
K3		P16	MTIOC3C/MTIOC3D/ RTCOUT/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
K4				USB0_DM		
K5				USB0_DP		
K6		P53	MTIOC2B	SSLA0/CTS2#/RTS2#/SS2#	SEG05	
K7		P54	MTIOC4B/TMCI1		VL2	
K8		PC6	MTIOC3C/MTCLKA/ TMCI2	RXD1/SMISO1/SSCL1/MOSIA/ RXD8/SMISO8/SSCL8/ USB0_EXICEN	VL4	
K9		PC5	MTIOC3B/MTCLKD/ TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
K10		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
1		PJ0				DA0
2		P27	MTIOC2B/TMCI3	SCK1/SCK12/RXD6/SMISO6/ SSCL6		IRQ3/CMPA2/ CACREF/ ADTRG0#
3		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/TXD6/SMOSI6/ SSDA6		
4		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	CAPH	IRQ0
5		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	CAPL	IRQ1
6	MD					FINED
7	RES#					
8	XCOUT					
9	XCIN	PH7				
10	UPSEL	P35				NMI
11	XTAL					
12	EXTAL					
13	VCL					
14	VSS					
15	VCC					
16		P32	MTIOC0C/RTCOUT/ TMO3	TXD6/SMOSI6/SSDA6/CTS6#/ RTS6#/SS6#		IRQ2
17		P17	MTIOC0C/MTIOC3A/ MTIOC3B/POE8#/TMO1	SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12		IRQ7
18		P16	MTIOC3C/MTIOC3D/ RTCOUT/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
19		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1/RSPCKA		IRQ5/CLKOUT/ CACREF
20	UB#	P14	MTIOC0A/MTIOC3A/ MTCLKA/TMRI2	CTS1#/RTS1#/SS1#/SSLA0/ TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/USB0_OVRCURA		IRQ4
21	VCC_USB					
22				USB0_DM		
23				USB0_DP		
24	VSS_USB					
25		P55	MTIOC4D/TMO3		VL1	
26		P54	MTIOC4B/TMCI1		VL2	
27		PC7	MTIOC3A/MTCLKB/ TMO2	TXD1/SMOSI1/SSDA1/MISOA/ TXD8/SMOSI8/SSDA8/ USB0_OVRCURB	VL3	CACREF
28		PC6	MTIOC3C/MTCLKA/ TMCI2	RXD1/SMISO1/SSCL1/MOSIA/ RXD8/SMISO8/SSCL8/ USB0_EXICEN	VL4	
29		PC5	MTIOC3B/MTCLKD/ TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
30		PC4	MTIOC3D/MTCLKC/ POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/ USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3/ IRRXD5	COM3	

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (12/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Ah	S12AD	A/D Temperature Sensor Data Register	ADTSDR	16	16	2 or 3 PCLKB
0008 901Ch	S12AD	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9028h	S12AD	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 902Ah	S12AD	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 902Ch	S12AD	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 902Eh	S12AD	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9030h	S12AD	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9032h	S12AD	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9034h	S12AD	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9036h	S12AD	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 9038h	S12AD	A/D Data Register 12	ADDR12	16	16	2 or 3 PCLKB
0008 903Ah	S12AD	A/D Data Register 13	ADDR13	16	16	2 or 3 PCLKB
0008 903Ch	S12AD	A/D Data Register 14	ADDR14	16	16	2 or 3 PCLKB
0008 903Eh	S12AD	A/D Data Register 15	ADDR15	16	16	2 or 3 PCLKB
0008 904Ah	S12AD	A/D Data Register 21	ADDR21	16	16	2 or 3 PCLKB
0008 9060h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 9061h	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 9070h	S12AD	A/D Sampling State Register T	ADSSTRT	8	8	2 or 3 PCLKB
0008 9071h	S12AD	A/D Sampling State Register O	ADSSTRO	8	8	2 or 3 PCLKB
0008 9073h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 9074h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 9075h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 9076h	S12AD	A/D Sampling State Register 4	ADSSTR4	8	8	2 or 3 PCLKB
0008 9077h	S12AD	A/D Sampling State Register 5	ADSSTR5	8	8	2 or 3 PCLKB
0008 9078h	S12AD	A/D Sampling State Register 6	ADSSTR6	8	8	2 or 3 PCLKB
0008 9079h	S12AD	A/D Sampling State Register 7	ADSSTR7	8	8	2 or 3 PCLKB
0008 907Ch	S12AD	A/D High-Side Reference Voltage Control Register	ADHVREFCNT	8	8	2 or 3 PCLKB
0008 9080h	S12AD	A/D Sampling State Register 21	ADSSTR21	8	8	2 or 3 PCLKB
0008 A000h	SCI0	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A001h	SCI0	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A002h	SCI0	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A003h	SCI0	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A004h	SCI0	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A005h	SCI0	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A006h	SCI0	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A007h	SCI0	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A008h	SCI0	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A009h	SCI0	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A00Ah	SCI0	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A00Bh	SCI0	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A00Ch	SCI0	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A00Dh	SCI0	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A020h	SCI1	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A021h	SCI1	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A022h	SCI1	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A023h	SCI1	Transmit Data Register	TDR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (22/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0840h	LCDC	LCD Display Data Register 00	SEG00	8	8	1 or 2 PCLKB
000A 0841h	LCDC	LCD Display Data Register 01	SEG01	8	8	1 or 2 PCLKB
000A 0842h	LCDC	LCD Display Data Register 02	SEG02	8	8	1 or 2 PCLKB
000A 0843h	LCDC	LCD Display Data Register 03	SEG03	8	8	1 or 2 PCLKB
000A 0844h	LCDC	LCD Display Data Register 04	SEG04	8	8	1 or 2 PCLKB
000A 0845h	LCDC	LCD Display Data Register 05	SEG05	8	8	1 or 2 PCLKB
000A 0846h	LCDC	LCD Display Data Register 06	SEG06	8	8	1 or 2 PCLKB
000A 0847h	LCDC	LCD Display Data Register 07	SEG07	8	8	1 or 2 PCLKB
000A 0848h	LCDC	LCD Display Data Register 08	SEG08	8	8	1 or 2 PCLKB
000A 0849h	LCDC	LCD Display Data Register 09	SEG09	8	8	1 or 2 PCLKB
000A 084Ah	LCDC	LCD Display Data Register 10	SEG10	8	8	1 or 2 PCLKB
000A 084Bh	LCDC	LCD Display Data Register 11	SEG11	8	8	1 or 2 PCLKB
000A 084Ch	LCDC	LCD Display Data Register 12	SEG12	8	8	1 or 2 PCLKB
000A 084Dh	LCDC	LCD Display Data Register 13	SEG13	8	8	1 or 2 PCLKB
000A 084Eh	LCDC	LCD Display Data Register 14	SEG14	8	8	1 or 2 PCLKB
000A 084Fh	LCDC	LCD Display Data Register 15	SEG15	8	8	1 or 2 PCLKB
000A 0850h	LCDC	LCD Display Data Register 16	SEG16	8	8	1 or 2 PCLKB
000A 0851h	LCDC	LCD Display Data Register 17	SEG17	8	8	1 or 2 PCLKB
000A 0852h	LCDC	LCD Display Data Register 18	SEG18	8	8	1 or 2 PCLKB
000A 0853h	LCDC	LCD Display Data Register 19	SEG19	8	8	1 or 2 PCLKB
000A 0854h	LCDC	LCD Display Data Register 20	SEG20	8	8	1 or 2 PCLKB
000A 0855h	LCDC	LCD Display Data Register 21	SEG21	8	8	1 or 2 PCLKB
000A 0856h	LCDC	LCD Display Data Register 22	SEG22	8	8	1 or 2 PCLKB
000A 0857h	LCDC	LCD Display Data Register 23	SEG23	8	8	1 or 2 PCLKB
000A 0858h	LCDC	LCD Display Data Register 24	SEG24	8	8	1 or 2 PCLKB
000A 0859h	LCDC	LCD Display Data Register 25	SEG25	8	8	1 or 2 PCLKB
000A 085Ah	LCDC	LCD Display Data Register 26	SEG26	8	8	1 or 2 PCLKB
000A 085Bh	LCDC	LCD Display Data Register 27	SEG27	8	8	1 or 2 PCLKB
000A 085Ch	LCDC	LCD Display Data Register 28	SEG28	8	8	1 or 2 PCLKB
000A 085Dh	LCDC	LCD Display Data Register 29	SEG29	8	8	1 or 2 PCLKB
000A 085Eh	LCDC	LCD Display Data Register 30	SEG30	8	8	1 or 2 PCLKB
000A 085Fh	LCDC	LCD Display Data Register 31	SEG31	8	8	1 or 2 PCLKB
000A 0860h	LCDC	LCD Display Data Register 32	SEG32	8	8	1 or 2 PCLKB
000A 0861h	LCDC	LCD Display Data Register 33	SEG33	8	8	1 or 2 PCLKB
000A 0862h	LCDC	LCD Display Data Register 34	SEG34	8	8	1 or 2 PCLKB
000A 0863h	LCDC	LCD Display Data Register 35	SEG35	8	8	1 or 2 PCLKB
000A 0864h	LCDC	LCD Display Data Register 36	SEG36	8	8	1 or 2 PCLKB
000A 0865h	LCDC	LCD Display Data Register 37	SEG37	8	8	1 or 2 PCLKB
000A 0866h	LCDC	LCD Display Data Register 38	SEG38	8	8	1 or 2 PCLKB
000A 0867h	LCDC	LCD Display Data Register 39	SEG39	8	8	1 or 2 PCLKB
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	1 or 2 PCLKB
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	1 or 2 PCLKB
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	1 or 2 PCLKB
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Time Register	CTSUSST	8	8	1 or 2 PCLKB
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	1 or 2 PCLKB
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	1 or 2 PCLKB
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	1 or 2 PCLKB
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	1 or 2 PCLKB
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	1 or 2 PCLKB
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	1 or 2 PCLKB
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	1 or 2 PCLKB
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	1 or 2 PCLKB

5.2 DC Characteristics

Table 5.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)	V_{IH}	VCC × 0.7	—	5.8	V	
	Ports P16, P17, port PA6, port PB0 (5 V tolerant)		VCC × 0.8	—	5.8		
	Ports P02, P04, P07, ports P10 to P15, ports P20 to P27, ports P30 to P32, P35, ports P50 to P56, ports PA0 to PA5, PA7, ports PB1 to PB7, ports PC0 to PC7, ports PD0 to PD4, ports PE0 to PE7, ports PF6, PF7, port PH7, ports PJ0*1, PJ2*1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Other than RIIC input pin		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Other than RIIC input pin		VCC × 0.1	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	XTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		AVCC0 × 0.7	—	AVCC0 + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	XTAL (external clock input)		–0.3	—	VCC × 0.2		
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		–0.3	—	AVCC0 × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		

Note 1. There are restrictions on AVCC0 and VCC depending on the usage conditions for the 12-bit D/A converter and I/O ports. When using ports PJ0 and PJ2 multiplexed with DA0 and DA1 as general I/O ports, make sure that VCC ≤ AVCC0.

Table 5.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB < 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports P16, P17, port PA6, port PB0 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports P02, P04, P07, ports P10 to P15, ports P20 to P27, ports P30 to P32, P35, ports P50 to P56, ports PA0 to PA5, PA7 ports PB1 to PB7, ports PC0 to PC7, ports PD0 to PD4, ports PE0 to PE7, ports PF6, PF7, port PH7, ports PJ0*1, PJ2*1, PJ3, RES#		VCC × 0.8	—	VCC + 0.3		
	All pins	V_{IL}	–0.3	—	VCC × 0.2		
	All pins	ΔV_T	VCC × 0.01	—	—		
Input voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	XTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		AVCC0 × 0.7	—	AVCC0 + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	XTAL (external clock input)		–0.3	—	VCC × 0.2		
	Ports P40 to P44, P46, ports P90 to P92, ports PJ6, PJ7		–0.3	—	AVCC0 × 0.3		

Note 1. There are restrictions on AVCC0 and VCC depending on the usage conditions for the 12-bit D/A converter and I/O ports. When using ports PJ0 and PJ2 multiplexed with DA0 and DA1 as general I/O ports, make sure that VCC ≤ AVCC0.

Table 5.5 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port P35, port PH7	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, 5.8 V
	Pins other than above		—	—	1.0		V_{in} = 0 V, VCC
Input capacitance	All input pins (except for port P16, port P35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF	V_{in} = 0 V Frequency: 1 MHz T_a = 25°C
	Port P16, port P35, USB0_DM, USB0_DP		—	—	30		

Table 5.6 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for ports P35, PH7)	R_U	10	20	100	kΩ	V_{in} = 0 V

Table 5.7 DC Characteristics (5) (1/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 32 MHz	I_{CC}	3.6	—	mA	
				ICLK = 16 MHz		2.4	—		
				ICLK = 8 MHz		1.8	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		14.0	—		
				ICLK = 16 MHz		7.9	—		
				ICLK = 8 MHz		4.9	—		
			All peripheral operation: Max.*3	ICLK = 32 MHz		—	30.0		
		Sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.9	—		
				ICLK = 16 MHz		1.5	—		
				ICLK = 8 MHz		1.3	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		8.2	—		
				ICLK = 16 MHz		4.8	—		
				ICLK = 8 MHz		3.1	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 32 MHz		1.1	—		
				ICLK = 16 MHz		0.95	—		
				ICLK = 8 MHz		0.86	—		
			All peripheral operation: Normal*3	ICLK = 32 MHz		6.4	—		
				ICLK = 16 MHz		3.8	—		
				ICLK = 8 MHz		2.4	—		
		Increase during flash rewrite*5				2.5	—		
	Middle-speed operating modes	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.1	—	mA	
				ICLK = 8 MHz		1.4	—		
				ICLK = 1 MHz		0.77	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		6.3	—		
				ICLK = 8 MHz		4.6	—		
				ICLK = 1 MHz		1.6	—		
			All peripheral operation: Max.*7	ICLK = 12 MHz		—	14.2		
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.4	—		
				ICLK = 8 MHz		0.90	—		
				ICLK = 1 MHz		0.68	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.9	—		
				ICLK = 8 MHz		2.9	—		
				ICLK = 1 MHz		1.4	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.1	—		
				ICLK = 8 MHz		0.63	—		
				ICLK = 1 MHz		0.55	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		3.3	—		
				ICLK = 8 MHz		2.4	—		
				ICLK = 1 MHz		1.2	—		
		Increase during flash rewrite*5				2.5	—		

Table 5.9 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Permissible total consumption power*1	Pd	—	300	mW	D version (T_a = -40 to 85°C)
		—	105		G version (T_a = -40 to 105°C)*2

Note 1. Total power dissipated by the entire chip (including output currents).
Note 2. Please contact Renesas Electronics sales office for derating under T_a = +85°C to 105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 5.10 DC Characteristics (8) (1/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.2	mA	
	During D/A conversion (per channel)		—	0.4	0.8		
	Waiting for A/D and D/A conversion (all units)		—	—	0.4	µA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	52	µA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
	During D/A conversion	I_{REFH}	—	50	100	µA	
	Waiting for D/A conversion (all units)		—	—	100	nA	
LDV1, 2	Per channel	I_{LVD}	—	0.15	—	µA	
Temperature sensor*6	—	I_{TEMP}	—	75	—	µA	
Comparator B operating current*6	Window mode	I_{CMP}*4	—	12.5	—	µA	
	Comparator high-speed mode		—	6.5	—	µA	
	Comparator low-speed mode		—	1.7	—	µA	
LCD operating current*6	External resistance division method*8 $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice	I_{LCD1}*5	—	0.04	—	µA	
	Internal voltage boosting method (VLCD.VLCD = 04) $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice	I_{LCD2}*5	—	0.85	—	µA	
	Internal voltage boosting method (VLCD.VLCD = 12) $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice	I_{LCD2}*5	—	1.55	—	µA	
	Capacitor split method $f_{LCD} = f_{SUB}$ = 128 Hz, 1/3 bias, and 4-time slice	I_{LCD3}*5	—	0.20	—	µA	

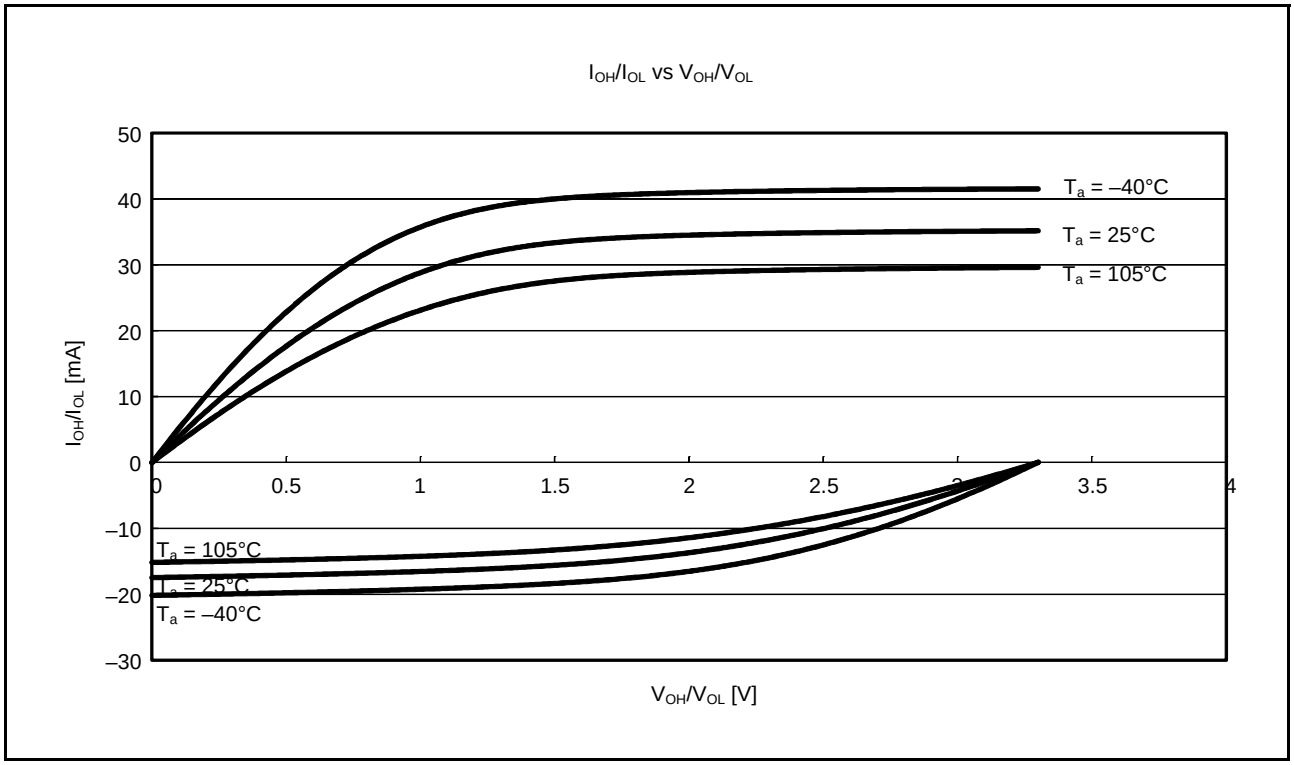


Figure 5.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of General Ports (Except for RIIC Output Pin, Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7) at VCC = 3.3 V (Reference Data)

5.3.2 Reset Timing

Table 5.23 Reset Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 5.26
	Other than above	t_{RESW}	30	—	—	µs	Figure 5.27
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 5.26
	During fast startup time*2	t_{RESWT}	—	560	—	µs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	114	—	µs	Figure 5.27
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 5.28
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESW2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESW2}	—	168	—	µs	

Note 1. When OFS1.(STUPLVD1REN, FASTSTUP) = 11b.
Note 2. When OFS1.(STUPLVD1REN, FASTSTUP) ≠ 11b.
Note 3. When IWDTCR.CKS[3:0] = 0000b.

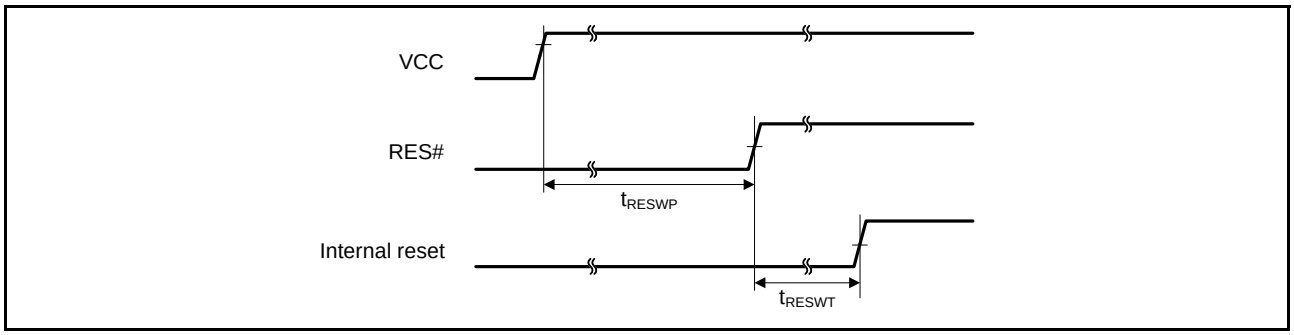


Figure 5.26 Reset Input Timing at Power-On

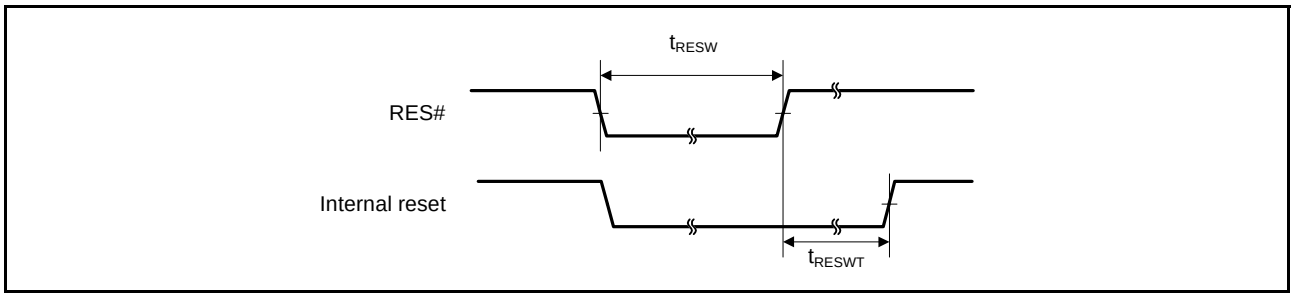


Figure 5.27 Reset Input Timing (1)

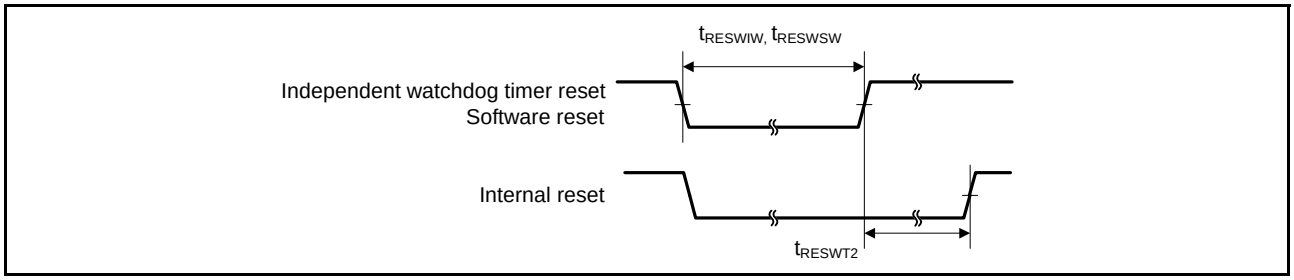


Figure 5.28 Reset Input Timing (2)

Table 5.45 D/A Conversion Characteristics (3)

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential nonlinearity error	—	±2.0	±16.0	LSB	
INL integral nonlinearity error	—	±8.0	±16.0	LSB	
Offset error	—	—	±30	mV	
Output resistance	—	75	—	Ω	
Conversion time	—	—	30	μs	

5.7 Temperature Sensor Characteristics

Table 5.46 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

5.8 Comparator Characteristics

Table 5.47 Comparator Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 or CVREFB1 input reference voltage		VREF	0	—	VCC - 1.4	V	
CMPB0 or CMPB1 input voltage		VI	–0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	µs	VCC = 3 V, input slew rate ≥ 50 mV/us
	Comparator high-speed mode Window function enabled	Tdw	—	—	2	µs	
	Comparator low-speed mode	Td	—	—	5	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	µs	

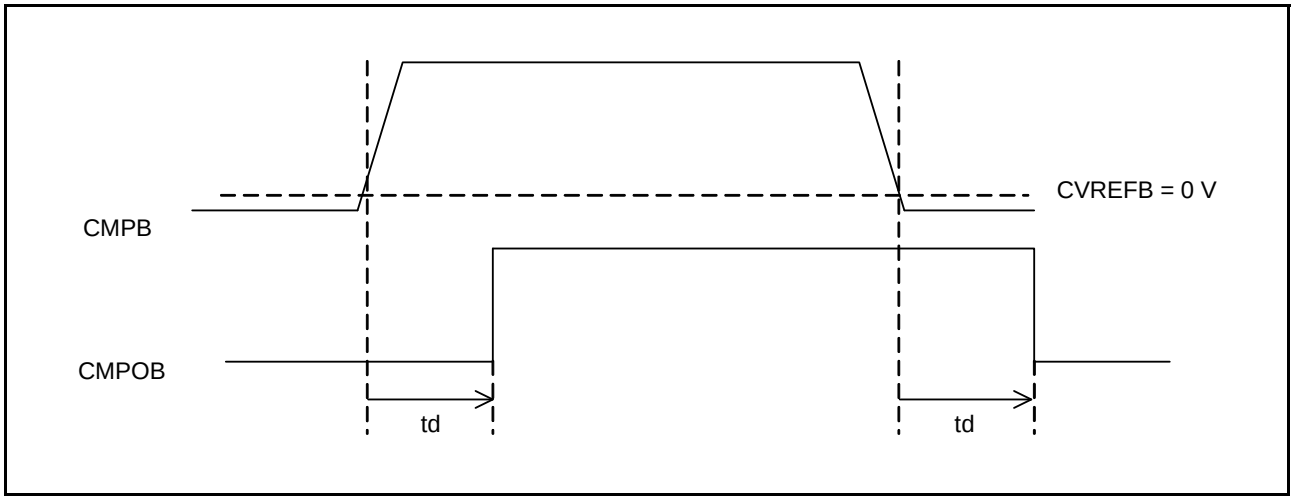


Figure 5.59 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

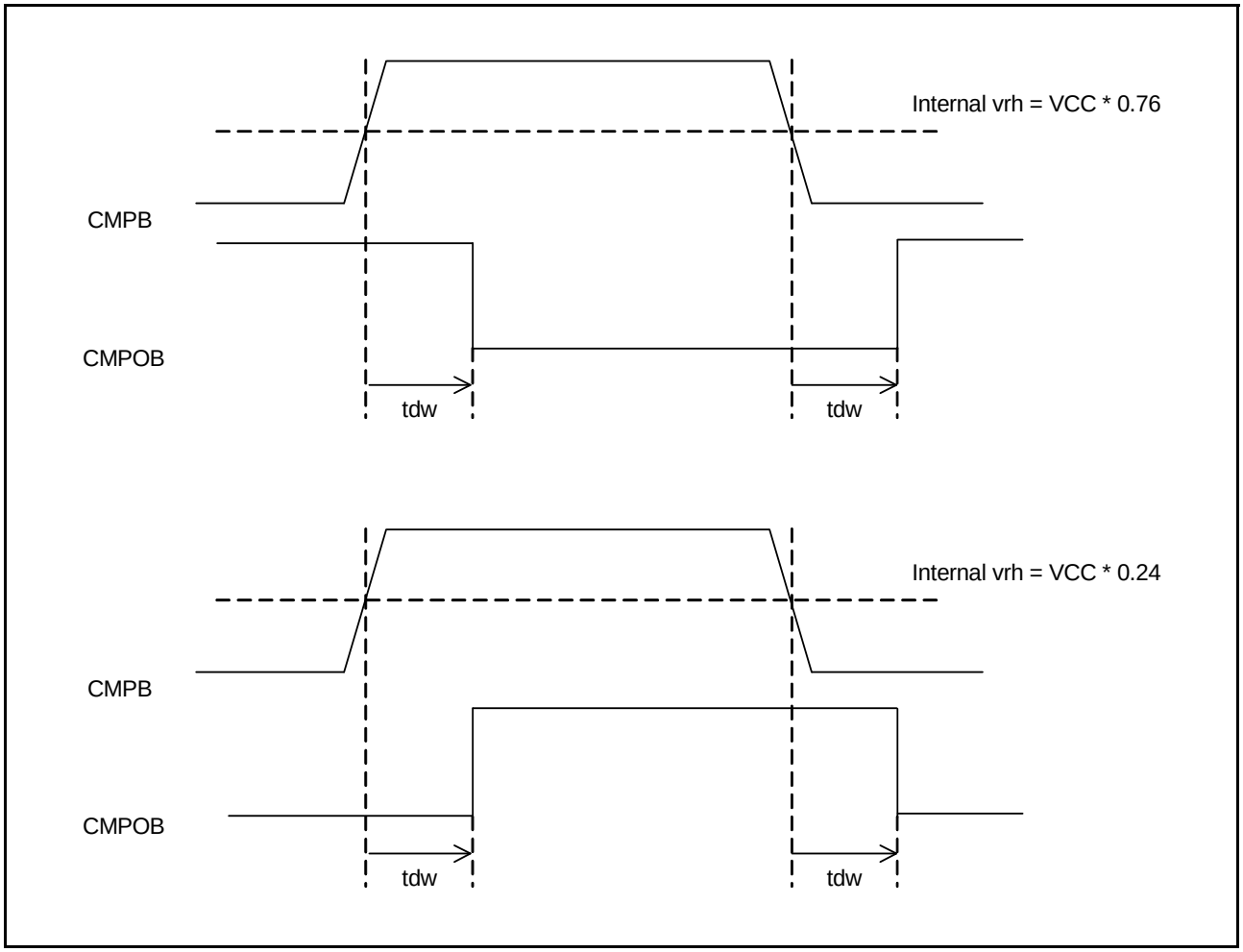


Figure 5.60 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

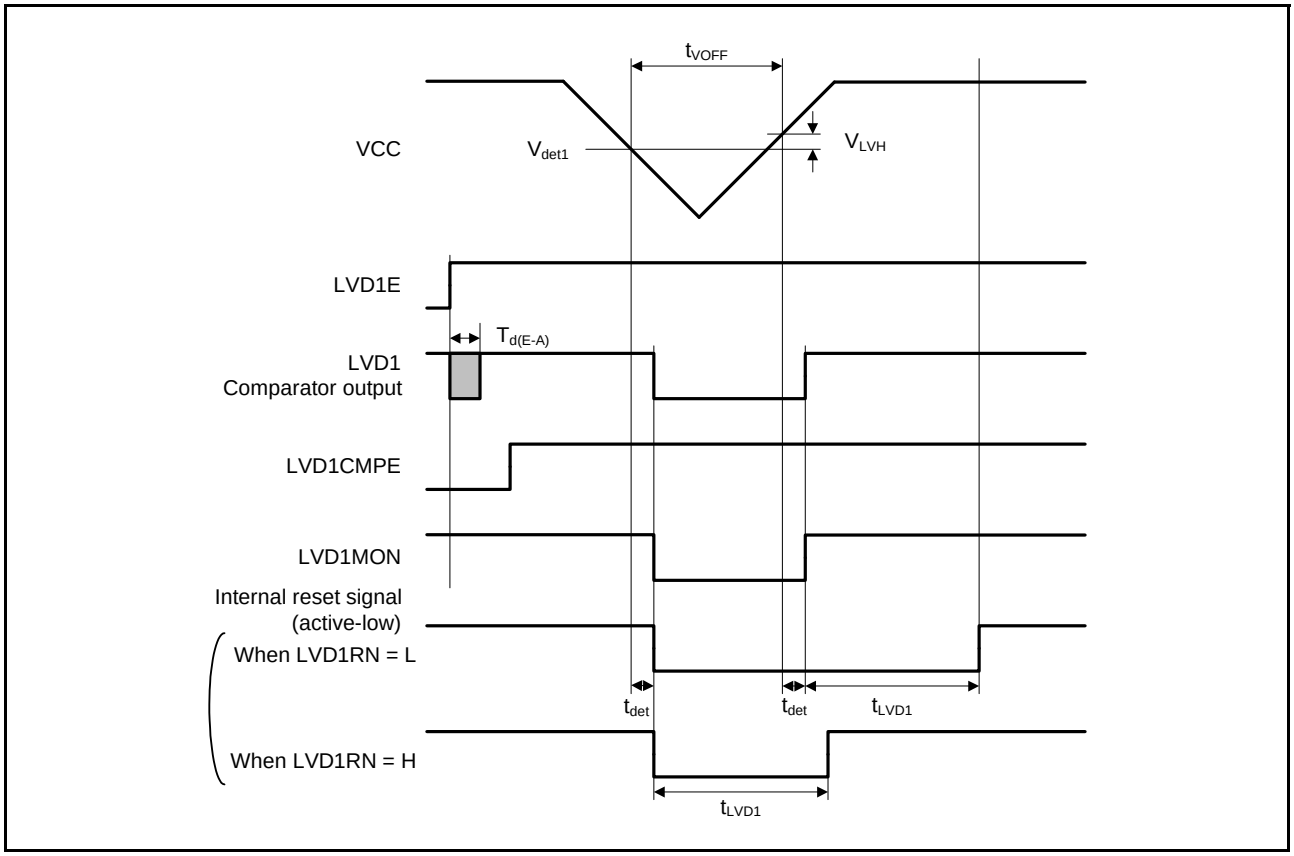


Figure 5.64 Voltage Detection Circuit Timing (V_{det1})

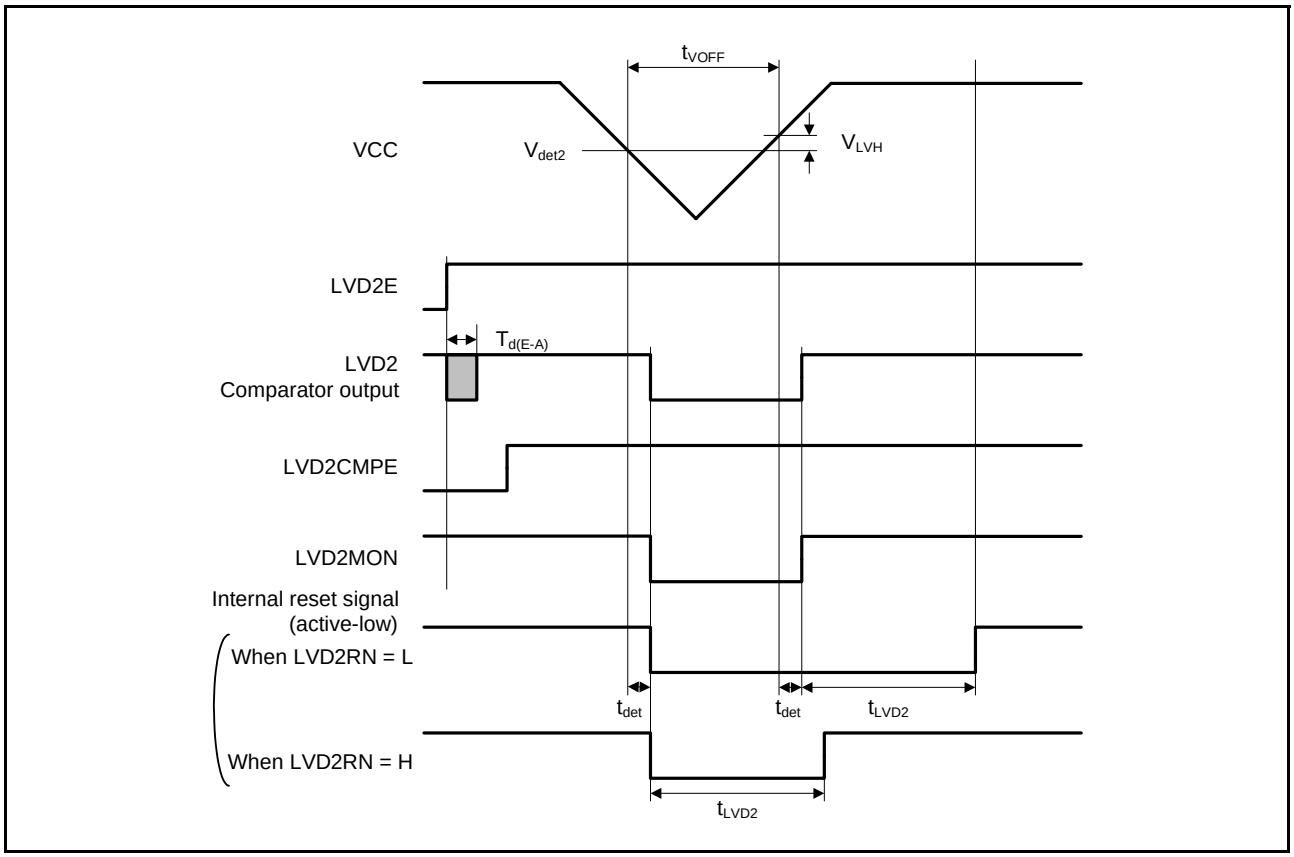
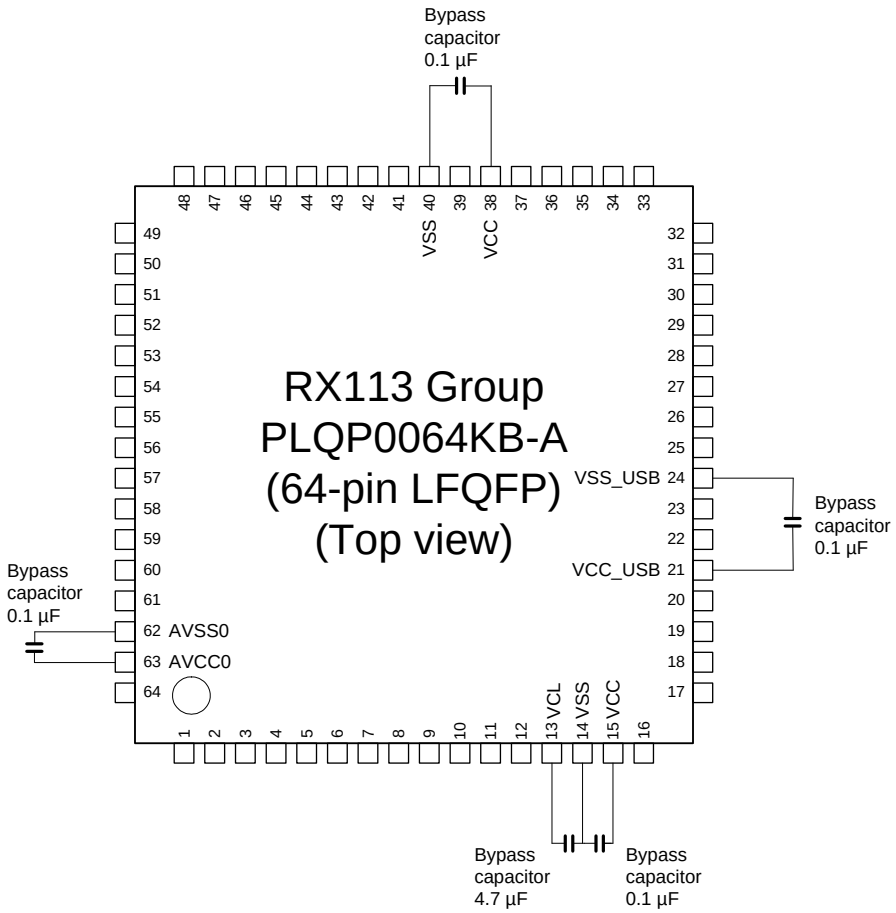


Figure 5.65 Voltage Detection Circuit Timing (V_{det2})



Note. Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.68 Connecting Capacitors (64 Pins)