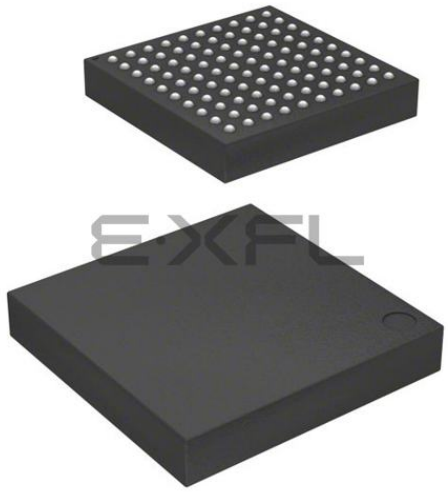
Renesas Electronics America Inc - R5F51137ADLJ#20 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51137adlj-20

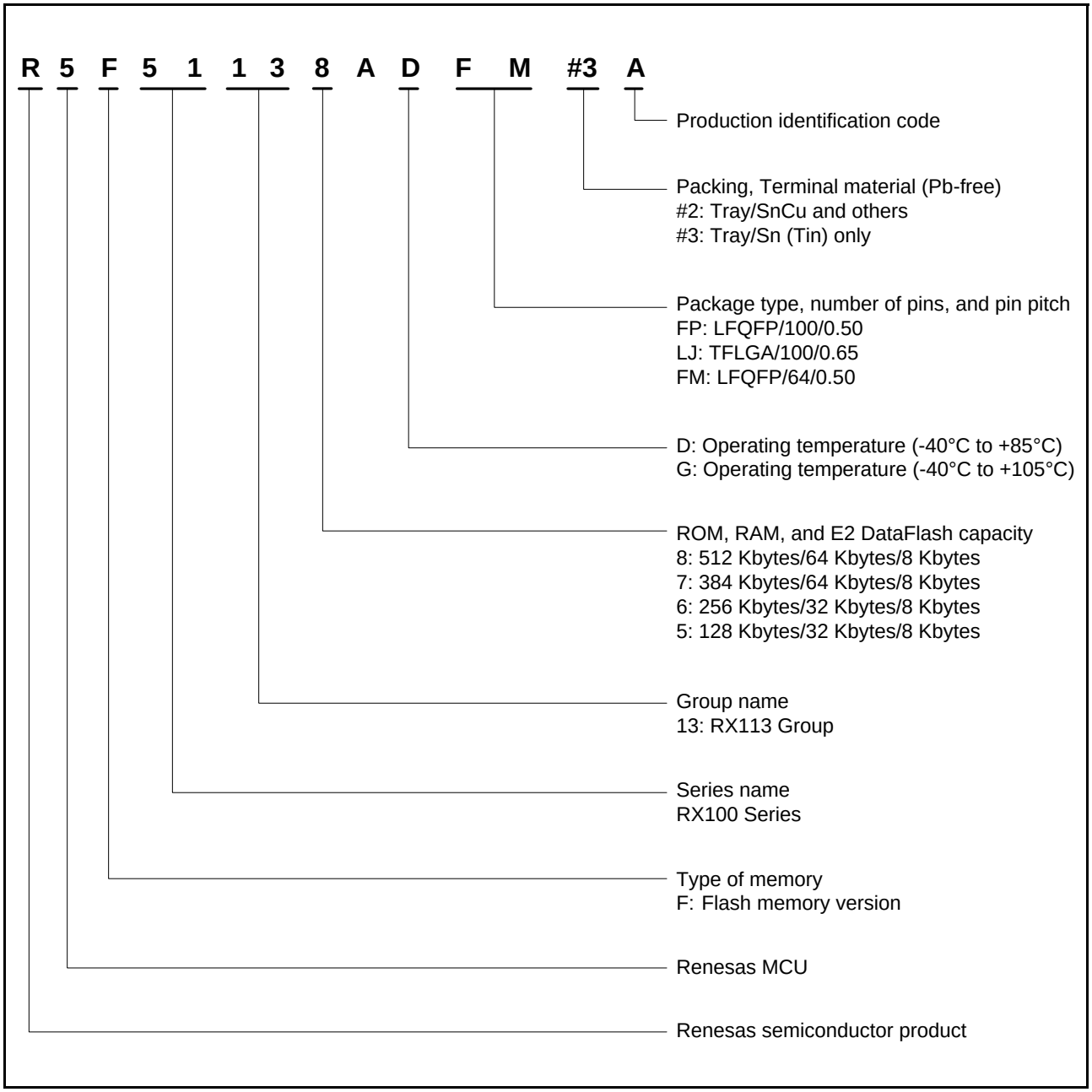
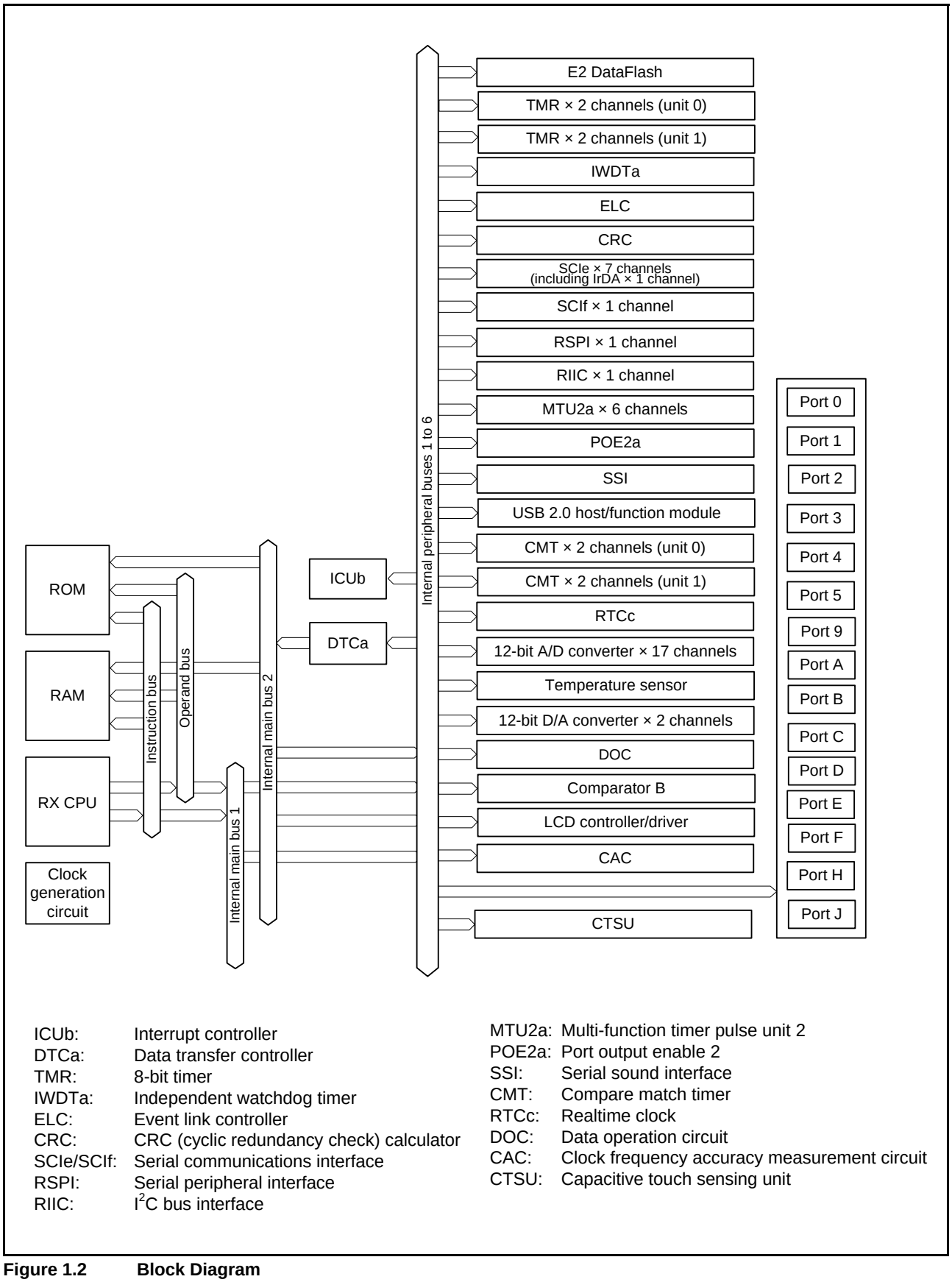


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICUb: Interrupt controller
DTCa: Data transfer controller
TMR: 8-bit timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIe/SCIf: Serial communications interface
RSPI: Serial peripheral interface
RIIC: I^2C bus interface

MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
SSI: Serial sound interface
CMT: Compare match timer
RTCc: Realtime clock
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit
CTSU: Capacitive touch sensing unit

Figure 1.2 Block Diagram

Table 1.4 Pin Functions (4/4)

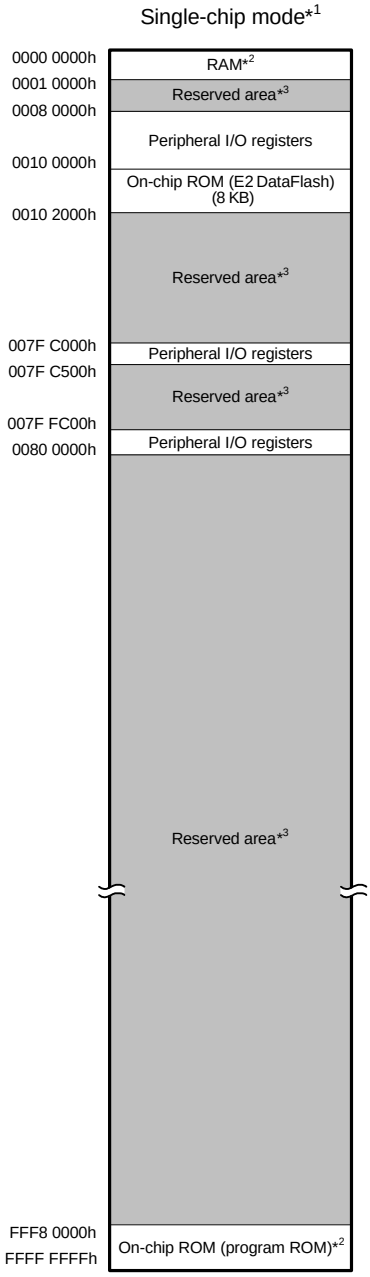
Classifications	Pin Name	I/O	Description
Comparator B	CMPB0	Input	Input pin for the analog signal to be processed by comparator B0.
	CVREFB0	Input	Analog reference voltage supply pin for comparator B0.
	CMPB1	Input	Input pin for the analog signal to be processed by comparator B1.
	CVREFB1	Input	Analog reference voltage supply pin for comparator B1.
	CMPOB0	Output	Output pin for comparator B0.
	CMPOB1	Output	Output pin for comparator B1.
LCD	VL1, VL2, VL3, VL4	I/O	Voltage pin for driving the LCD.
	CAPH, CAPL	I/O	Capacitor connection pin for the LCD controller/driver.
	COM0 to COM7	Output	Common signal output pins for the LCD controller/driver.
	SEG00 to SEG39	Output	Segment signal output pins for the LCD controller/driver.
CTSU	TS0 to TS11	Input	Capacitive touch detection pins (touch pins).
	TSCAP	I/O	Secondary power supply pin for the touch driver.
I/O ports	P02, P04, P07	I/O	3-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P32, P35	I/O	4-bit input/output pins (P35 input pin).
	P40 to P44, P46	I/O	6-bit input/output pins.
	P50 to P56	I/O	7-bit input/output pins.
	P90 to P92	I/O	3-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD4	I/O	5-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF6, PF7	I/O	2-bit input/output pins.
	PH7	Input	1-bit input pin.
	PJ0, PJ2, PJ3, PJ6, PJ7	I/O	5-bit input/output pins.

Note 1. For external clock input.

Table 1.6 List of Pins and Pin Functions (100-Pin TFLGA) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIe, SCIf, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
H1	XTAL					
H2	EXTAL					
H3		P15	MTIOC0B/MTCLKB/ TMCI2	RXD1/SMISO1/SSCL1/RSPCKA		IRQ5/CLKOUT/ CACREF
H4		P13	MTIOC0B/TMO3	CTS12#/RTS12#/SS12#/CTS0#/ RTS0#/SS0#	SEG00	IRQ3
H5		P11	MTIC5U/POE0#	RXD12/RXDX12/SMISO12/ SSCL12/RXD0/SMISO0/SSCL0	SEG02	IRQ7
H6		P51	MTIOC4C	RSPCKA/SCK2	SEG07	
H7		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1	SEG10	
H8		PC1	MTIOC3A	SCK5/SSLA2	SEG09	
H9		PB6	MTIOC3D	RXD9/SMISO9/SSCL9/SSIRXD0	SEG12/ COM5	
H10		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9/SSITXD0	SEG11/ COM4	
J1	VCL					
J2		P17	MTIOC0C/MTIOC3A/ MTIOC3B/POE8#/TMO1	SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12		IRQ7
J3		P32	MTIOC0C/RTCOUT/ TMO3	TXD6/SMOSI6/SSDA6/CTS6#/ RTS6#/SS6#	TS11	IRQ2
J4	VCC_USB					
J5	VSS_USB					
J6		P52		MISOA/RXD2/SMISO2/SSCL2	SEG06	
J7		P55	MTIOC4D/TMO3		VL1	
J8		PC7	MTIOC3A/MTCLKB/ TMO2	TXD1/SMOSI1/SSDA1/MISOA/ TXD8/SMOSI8/SSDA8/ USB0_OVRCURB	VL3	CACREF
J9		PC4	MTIOC3D/MTCLKC/ POE0#/TMCI1	SSLA0/CTS8#/RTS8#/SS8#/SCK5/ USB0_VBUSEN/USB0_VBUS *1	COM1	IRQ2/CLKOUT
J10		PC2	MTIOC4B	RXD5/SMOSI5/SSCL5/IRRXD5/ SSLA3	COM3	
K1	VSS					
K2	VDD					
K3		P16	MTIOC3C/MTIOC3D/ RTCOUT/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
K4				USB0_DM		
K5				USB0_DP		
K6		P53	MTIOC2B	SSLA0/CTS2#/RTS2#/SS2#	SEG05	
K7		P54	MTIOC4B/TMCI1		VL2	
K8		PC6	MTIOC3C/MTCLKA/ TMCI2	RXD1/SMISO1/SSCL1/MOSIA/ RXD8/SMISO8/SSCL8/ USB0_EXICEN	VL4	
K9		PC5	MTIOC3B/MTCLKD/ TMRI2	SCK1/RSPCKA/SCK8/USB0_ID	COM0	
K10		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5/IRTXD5	COM2	

Note 1. Not 5 V tolerant.
Note 2. The power source of the I/O buffer for these pins is AVCC0.



Note 1. The address space in boot mode is the same as the address space in single-chip mode.
Note 2. The capacity of ROM/RAM differs depending on the products.

ROM (bytes)		RAM (bytes)	
Capacity	**Address**	**Capacity**	**Address**
512 K	FFF8 0000h to FFFF FFFFh	64 K	0000 0000h to 0000 FFFFh
384 K	FFFA 0000h to FFFF FFFFh		
256 K	FFFC 0000h to FFFF FFFFh	32 K	0000 0000h to 0000 7FFFh
128 K	FFFE 0000h to FFFF FFFFh		

Note: See Table 1.3, List of Products, for the product type name.

Note 3. Reserved areas should not be accessed.

Figure 3.1 Memory Map

Table 4.1 List of I/O Registers (Address Order) (13/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 A024h	SCI1	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A025h	SCI1	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A026h	SCI1	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A027h	SCI1	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A028h	SCI1	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A029h	SCI1	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A02Ah	SCI1	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A02Bh	SCI1	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A02Ch	SCI1	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A02Dh	SCI1	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A040h	SCI2	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A041h	SCI2	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A042h	SCI2	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A043h	SCI2	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A044h	SCI2	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A045h	SCI2	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A046h	SCI2	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A047h	SCI2	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A048h	SCI2	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A049h	SCI2	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A04Ah	SCI2	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A04Bh	SCI2	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A04Ch	SCI2	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A04Dh	SCI2	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0A0h	SCI5	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0A1h	SCI5	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0A2h	SCI5	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0A3h	SCI5	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0A4h	SCI5	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0A5h	SCI5	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0A6h	SCI5	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0A7h	SCI5	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0A8h	SCI5	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0A9h	SCI5	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0AAh	SCI5	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0ABh	SCI5	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0ACh	SCI5	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0ADh	SCI5	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0C6h	SCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0C9h	SCI6	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0CAh	SCI6	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0CBh	SCI6	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0CCh	SCI6	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A109h	SCI8	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A10Ah	SCI8	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A10Bh	SCI8	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A10Ch	SCI8	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A129h	SCI9	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A12Ah	SCI9	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A12Bh	SCI9	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A12Ch	SCI9	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A500h	SSI0	Control Register	SSICR	32	32	2 or 3 PCLKB
0008 A504h	SSI0	Status Register	SSISR	32	32	2 or 3 PCLKB
0008 A510h	SSI0	FIFO Control Register	SSIFCR	32	32	2 or 3 PCLKB
0008 A514h	SSI0	FIFO Status Register	SSIFSR	32	32	2 or 3 PCLKB
0008 A518h	SSI0	Transmit FIFO Data Register	SSIFTDR	32	32	2 or 3 PCLKB
0008 A51Ch	SSI0	Receive FIFO Data Register	SSIFRDR	32	32	2 or 3 PCLKB
0008 A520h	SSI0	TDM Mode Register	SSITDMR	32	32	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 or 3 PCLKB
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 or 3 PCLKB
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 or 3 PCLKB
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 or 3 PCLKB
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 or 3 PCLKB
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (20/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-Of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3 or 4 PCLKB
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLK or more
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLK or more
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3 or 4 PCLKB
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3 or 4 PCLKB
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3 or 4 PCLKB
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3 or 4 PCLKB
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3 or 4 PCLKB
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3 or 4 PCLKB
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3 or 4 PCLKB
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3 or 4 PCLKB
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3 or 4 PCLKB
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more

Table 4.1 List of I/O Registers (Address Order) (22/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0840h	LCDC	LCD Display Data Register 00	SEG00	8	8	1 or 2 PCLKB
000A 0841h	LCDC	LCD Display Data Register 01	SEG01	8	8	1 or 2 PCLKB
000A 0842h	LCDC	LCD Display Data Register 02	SEG02	8	8	1 or 2 PCLKB
000A 0843h	LCDC	LCD Display Data Register 03	SEG03	8	8	1 or 2 PCLKB
000A 0844h	LCDC	LCD Display Data Register 04	SEG04	8	8	1 or 2 PCLKB
000A 0845h	LCDC	LCD Display Data Register 05	SEG05	8	8	1 or 2 PCLKB
000A 0846h	LCDC	LCD Display Data Register 06	SEG06	8	8	1 or 2 PCLKB
000A 0847h	LCDC	LCD Display Data Register 07	SEG07	8	8	1 or 2 PCLKB
000A 0848h	LCDC	LCD Display Data Register 08	SEG08	8	8	1 or 2 PCLKB
000A 0849h	LCDC	LCD Display Data Register 09	SEG09	8	8	1 or 2 PCLKB
000A 084Ah	LCDC	LCD Display Data Register 10	SEG10	8	8	1 or 2 PCLKB
000A 084Bh	LCDC	LCD Display Data Register 11	SEG11	8	8	1 or 2 PCLKB
000A 084Ch	LCDC	LCD Display Data Register 12	SEG12	8	8	1 or 2 PCLKB
000A 084Dh	LCDC	LCD Display Data Register 13	SEG13	8	8	1 or 2 PCLKB
000A 084Eh	LCDC	LCD Display Data Register 14	SEG14	8	8	1 or 2 PCLKB
000A 084Fh	LCDC	LCD Display Data Register 15	SEG15	8	8	1 or 2 PCLKB
000A 0850h	LCDC	LCD Display Data Register 16	SEG16	8	8	1 or 2 PCLKB
000A 0851h	LCDC	LCD Display Data Register 17	SEG17	8	8	1 or 2 PCLKB
000A 0852h	LCDC	LCD Display Data Register 18	SEG18	8	8	1 or 2 PCLKB
000A 0853h	LCDC	LCD Display Data Register 19	SEG19	8	8	1 or 2 PCLKB
000A 0854h	LCDC	LCD Display Data Register 20	SEG20	8	8	1 or 2 PCLKB
000A 0855h	LCDC	LCD Display Data Register 21	SEG21	8	8	1 or 2 PCLKB
000A 0856h	LCDC	LCD Display Data Register 22	SEG22	8	8	1 or 2 PCLKB
000A 0857h	LCDC	LCD Display Data Register 23	SEG23	8	8	1 or 2 PCLKB
000A 0858h	LCDC	LCD Display Data Register 24	SEG24	8	8	1 or 2 PCLKB
000A 0859h	LCDC	LCD Display Data Register 25	SEG25	8	8	1 or 2 PCLKB
000A 085Ah	LCDC	LCD Display Data Register 26	SEG26	8	8	1 or 2 PCLKB
000A 085Bh	LCDC	LCD Display Data Register 27	SEG27	8	8	1 or 2 PCLKB
000A 085Ch	LCDC	LCD Display Data Register 28	SEG28	8	8	1 or 2 PCLKB
000A 085Dh	LCDC	LCD Display Data Register 29	SEG29	8	8	1 or 2 PCLKB
000A 085Eh	LCDC	LCD Display Data Register 30	SEG30	8	8	1 or 2 PCLKB
000A 085Fh	LCDC	LCD Display Data Register 31	SEG31	8	8	1 or 2 PCLKB
000A 0860h	LCDC	LCD Display Data Register 32	SEG32	8	8	1 or 2 PCLKB
000A 0861h	LCDC	LCD Display Data Register 33	SEG33	8	8	1 or 2 PCLKB
000A 0862h	LCDC	LCD Display Data Register 34	SEG34	8	8	1 or 2 PCLKB
000A 0863h	LCDC	LCD Display Data Register 35	SEG35	8	8	1 or 2 PCLKB
000A 0864h	LCDC	LCD Display Data Register 36	SEG36	8	8	1 or 2 PCLKB
000A 0865h	LCDC	LCD Display Data Register 37	SEG37	8	8	1 or 2 PCLKB
000A 0866h	LCDC	LCD Display Data Register 38	SEG38	8	8	1 or 2 PCLKB
000A 0867h	LCDC	LCD Display Data Register 39	SEG39	8	8	1 or 2 PCLKB
000A 0900h	CTSU	CTSU Control Register 0	CTSUCR0	8	8	1 or 2 PCLKB
000A 0901h	CTSU	CTSU Control Register 1	CTSUCR1	8	8	1 or 2 PCLKB
000A 0902h	CTSU	CTSU Synchronous Noise Reduction Setting Register	CTSUSDPRS	8	8	1 or 2 PCLKB
000A 0903h	CTSU	CTSU Sensor Stabilization Wait Time Register	CTSUSST	8	8	1 or 2 PCLKB
000A 0904h	CTSU	CTSU Measurement Channel Register 0	CTSUMCH0	8	8	1 or 2 PCLKB
000A 0905h	CTSU	CTSU Measurement Channel Register 1	CTSUMCH1	8	8	1 or 2 PCLKB
000A 0906h	CTSU	CTSU Channel Enable Control Register 0	CTSUCHAC0	8	8	1 or 2 PCLKB
000A 0907h	CTSU	CTSU Channel Enable Control Register 1	CTSUCHAC1	8	8	1 or 2 PCLKB
000A 090Bh	CTSU	CTSU Channel Transmit/Receive Control Register 0	CTSUCHTRC0	8	8	1 or 2 PCLKB
000A 090Ch	CTSU	CTSU Channel Transmit/Receive Control Register 1	CTSUCHTRC1	8	8	1 or 2 PCLKB
000A 0910h	CTSU	CTSU High-Pass Noise Reduction Control Register	CTSUDCLKC	8	8	1 or 2 PCLKB
000A 0911h	CTSU	CTSU Status Register	CTSUST	8	8	1 or 2 PCLKB

Table 5.7 DC Characteristics (5) (2/2)

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item					Symbol	Typ *4	Max	Unit	Test Conditions
Supply current*1	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32.768 kHz	I_{CC}	4.3	—	μA	
			All peripheral operation: Normal*9, *10	ICLK = 32.768 kHz		15.0	—		
			All peripheral operation: Max.*9, *10	ICLK = 32.768kHz		—	62		
		Sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		2.3	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		8.6	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32.768 kHz		1.7	—		
			All peripheral operation: Normal*9	ICLK = 32.768 kHz		7.0	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK and PCLK are set to the same frequency as ICLK.
Note 4. Values when VCC = 3.3 V.
Note 5. This is the increase for programming or erasure of the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK = 12 MHz, and HOCO otherwise. FCLK and PCLK are set to the same frequency as ICLK.
Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub-clock oscillator. FCLK and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub-clock oscillator. FCLK and PCLK are set to the same frequency as ICLK.
Note 10. Values when the MSTPCRA.MSTPA17 bit (12-bit A/D converter module stop bit) is set to “transition to the module stop state is made”.

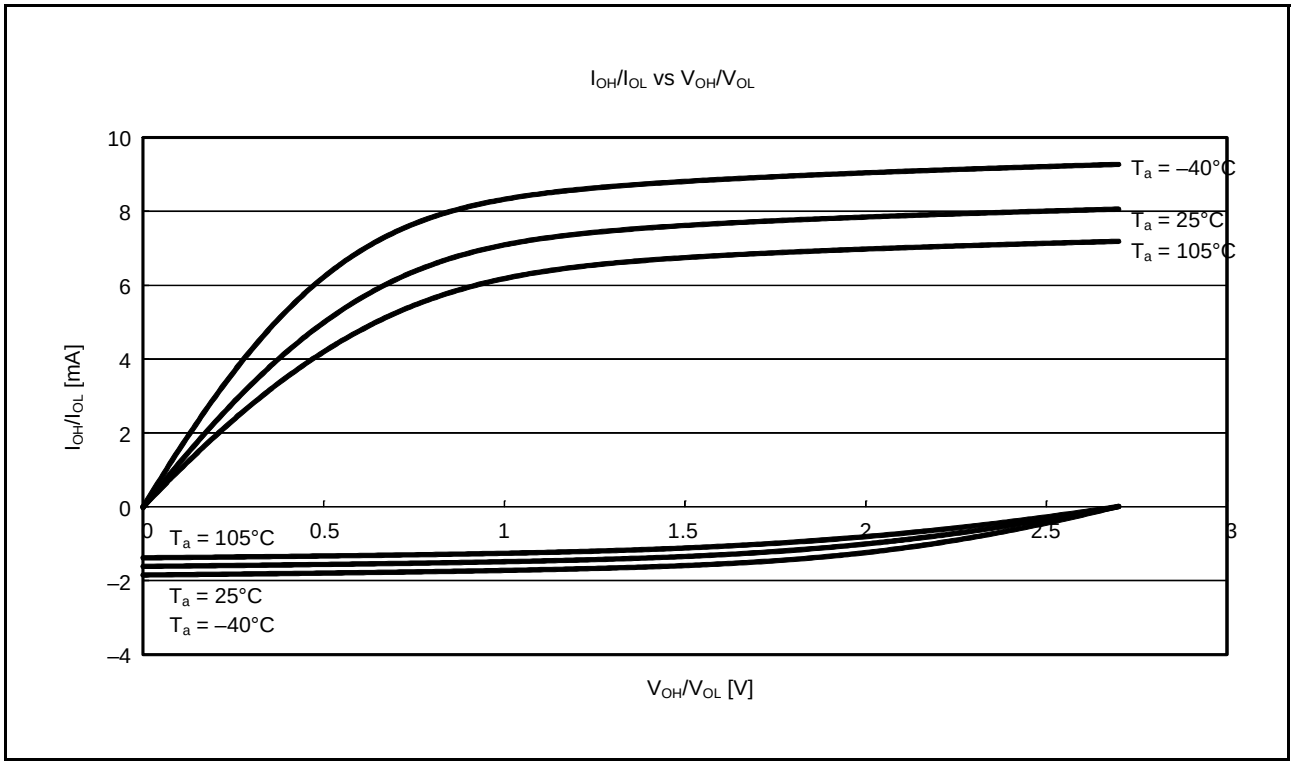


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7 at VCC = 2.7 V (Reference Data)

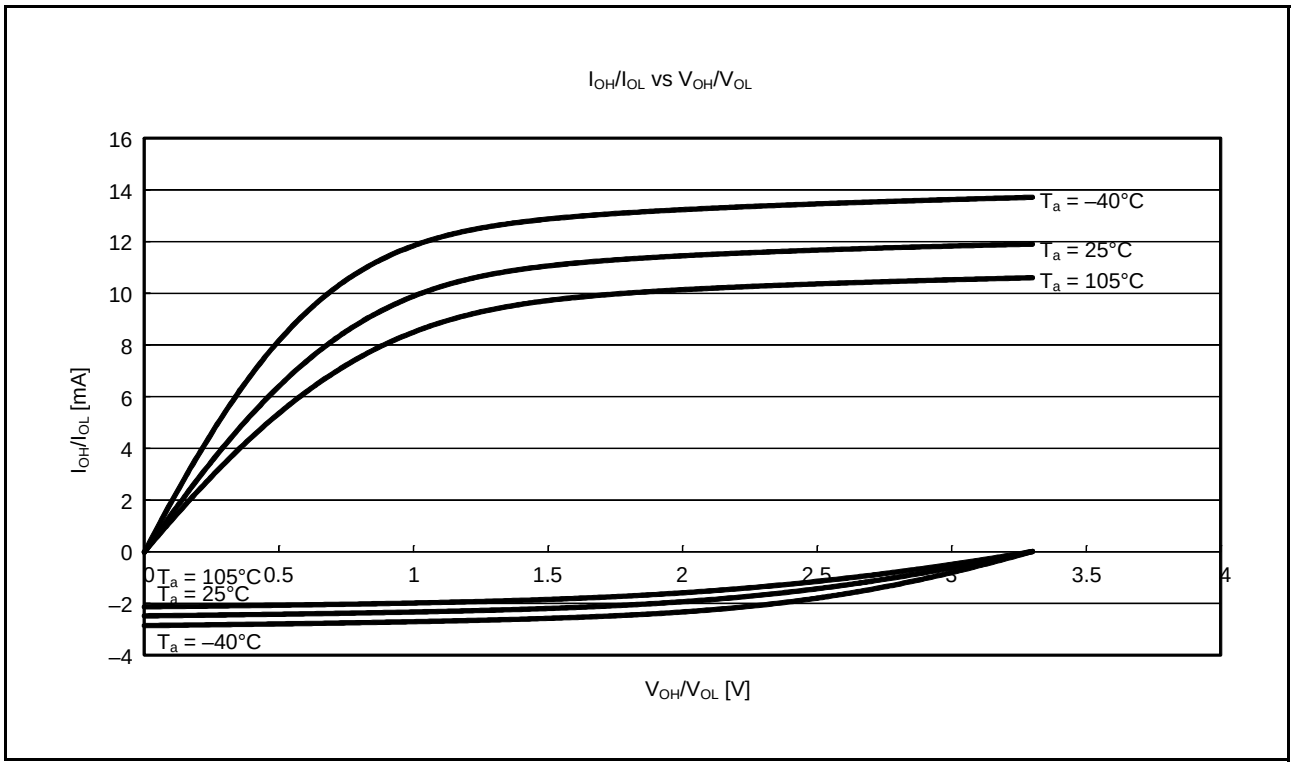


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Ports P40 to P44, P46, Ports P90 to P92, Ports PJ6, PJ7 at VCC = 3.3 V (Reference Data)

Table 5.22 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
XTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 5.18
XTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
XTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
XTAL external clock rising time		t_{Xr}	—	—	5	ns	
XTAL external clock falling time		t_{Xf}	—	—	5	ns	
XTAL external clock input wait time*1		t_{EXWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	2.4 ≤ VCC ≤ 3.6	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 5.19
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 5.20
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 5.21
HOCO clock oscillation frequency		f_{HOCO}	31.52	32	32.48	MHz	T_a = –40 to 85°C
			31.68	32	32.32		T_a = –20 to 85°C
			31.36	32	32.64		T_a = –40 to 105°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	56	μs	Figure 5.23
PLL input frequency*3		f_{PLLIN}	4	—	8	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	32	—	48	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.24
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	6, 8*6	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 5.24
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 5.25

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

Note 3. The VCC range should be 2.4 to 3.6 V when the PLL is used.

Note 4. After changing the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit so that the sub-clock oscillator operates, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Reference value when a 32.768-kHz resonator is used.

Note 5. The VCC range should be 3.0 to 3.6 V when the USBPLL is used.

Note 6. The input frequency can be set to 6 or 8 MHz only and the oscillation frequency can be set to 48 MHz only.

Note 7. Only 32.768 kHz can be used.

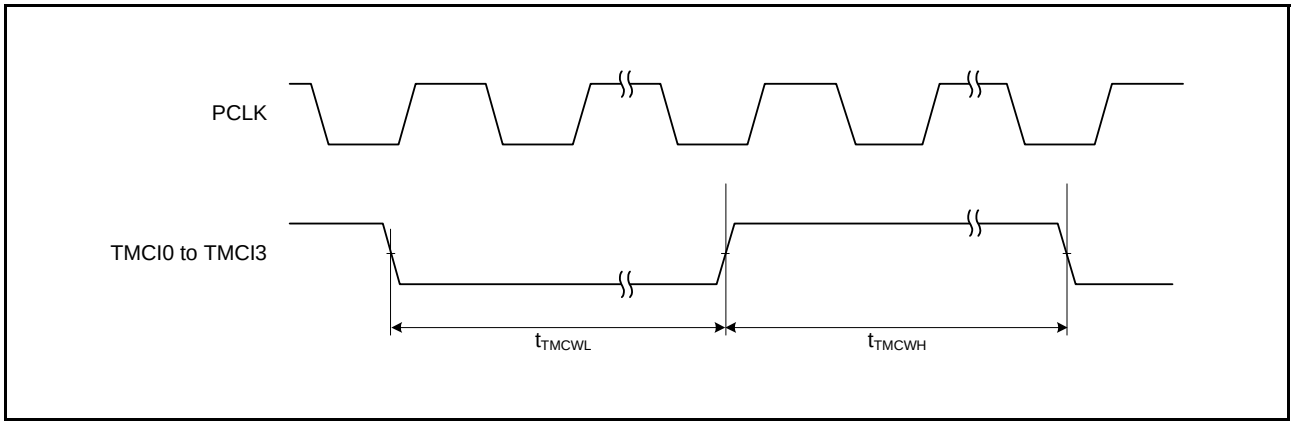


Figure 5.37 TMR Clock Input Timing

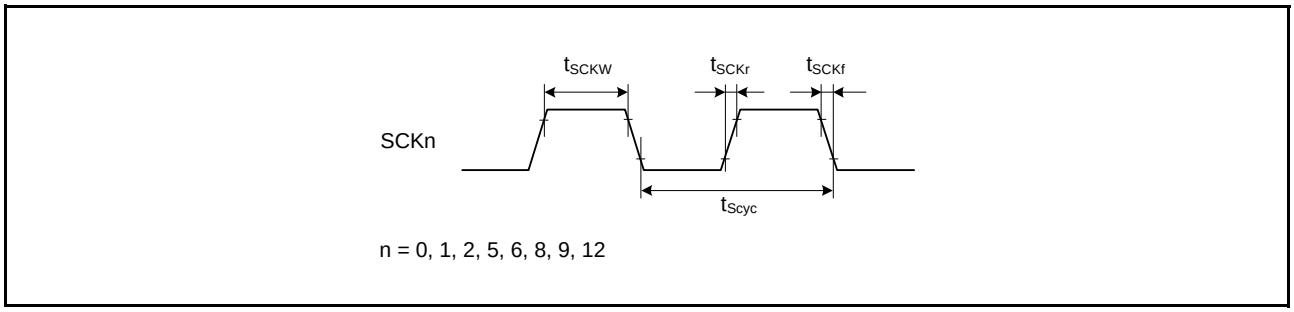


Figure 5.38 SCK Clock Input Timing

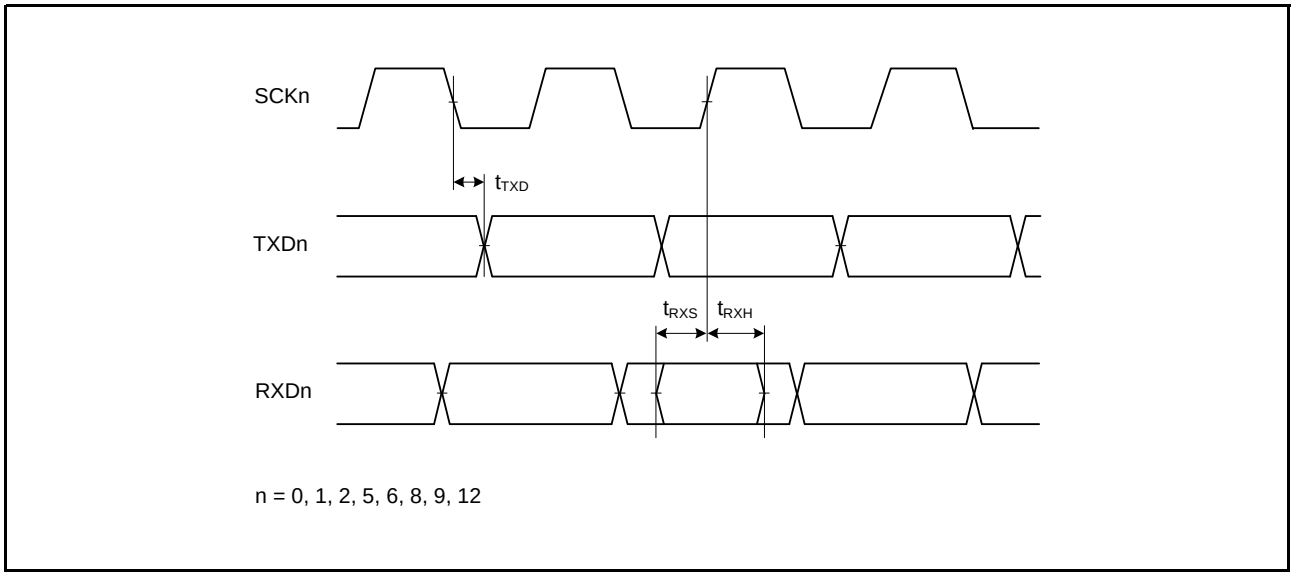


Figure 5.39 SCI Input/Output Timing: Clock Synchronous Mode

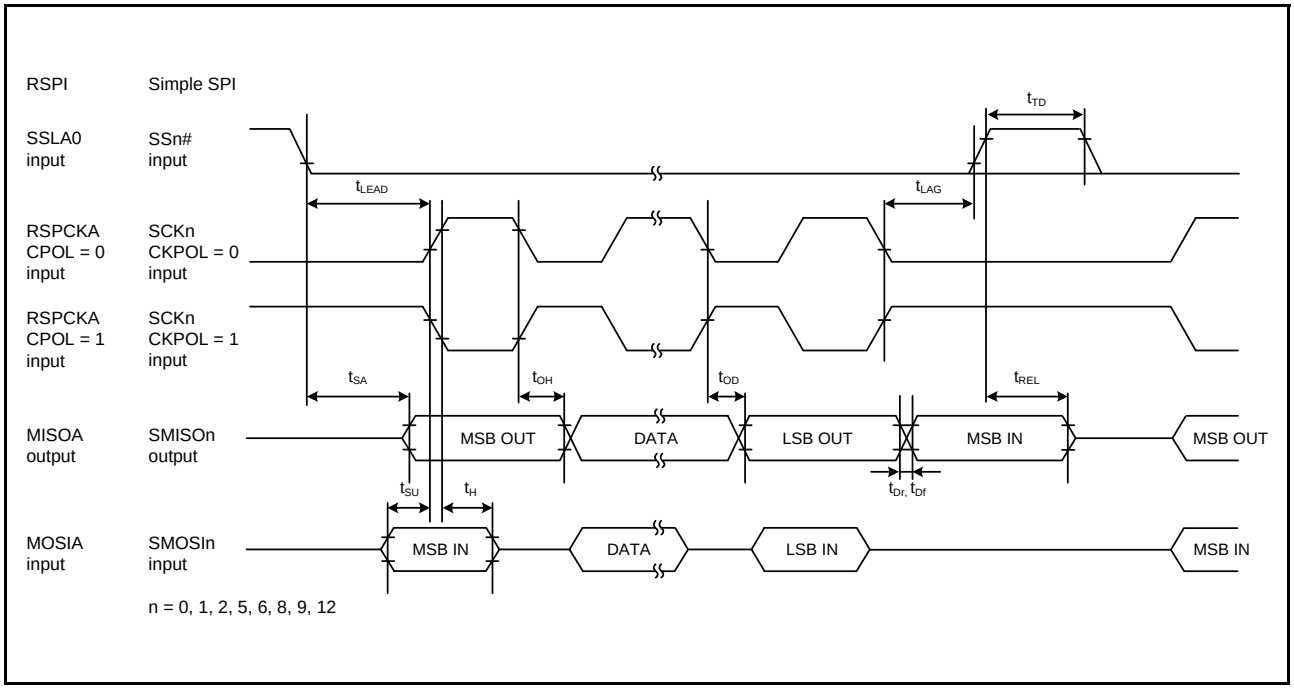


Figure 5.47 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

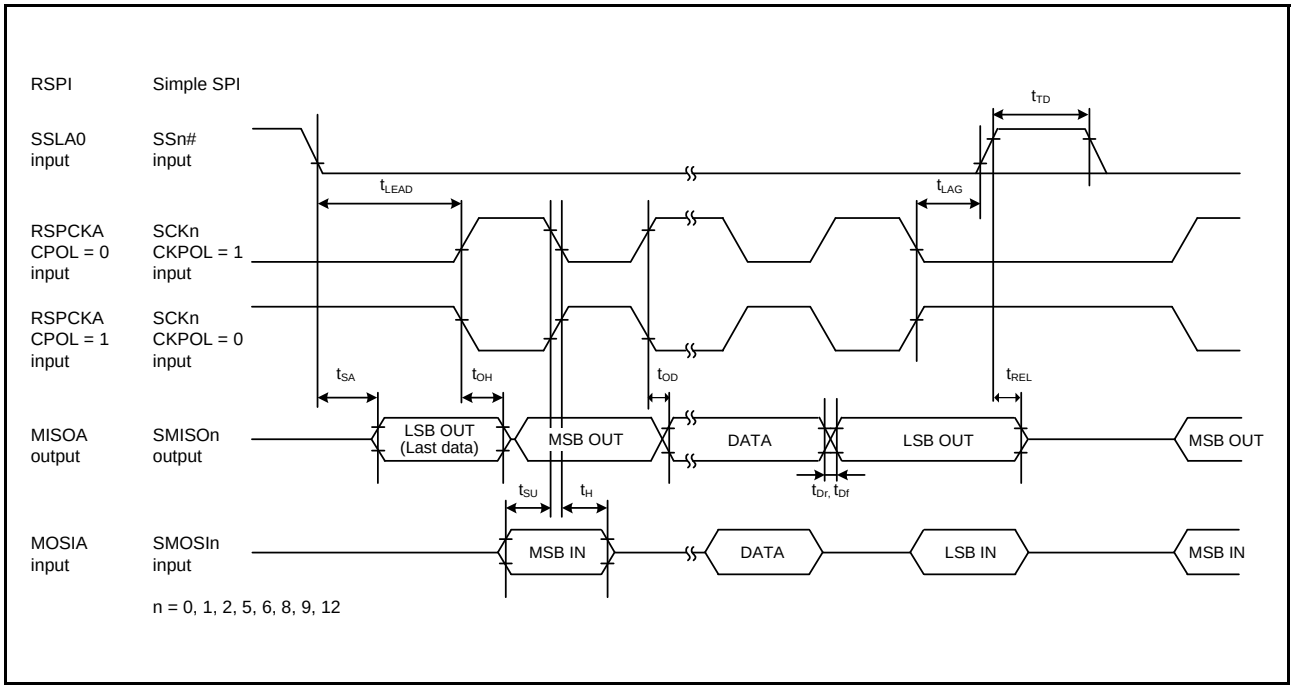


Figure 5.48 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

Table 5.40 A/D Conversion Characteristics (4)

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V,
ADHVREFCNT.OCSVSEL = 1 (internal reference voltage selected as high-side reference voltage),
PJ7PFS.ASEL = 0 (AVSS0 pin selected as low-side reference power supply ground pin)
T_a = –40 to +105°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	2	MHz	
Resolution		—	—	12	Bit	
Internal reference voltage		1.36	1.43	1.50	V	
Conversion time*1 (Operation at PCLKD = 2 MHz)	Permissible signal source impedance (Max.) = 5.0 kΩ	16 (1.5)*2	—	—	µs	High-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 02h
		17.5 (3.0)*2	—	—		Normal-precision channel ADCSR.ADHSC bit = 0 ADSSTRn.SST[7:0] bits = 05h
Analog input effective range		0	—	Internal reference voltage	V	
Offset error		—	—	±24.0	LSB	
DNL differential nonlinearity error		—	±16.0	—	LSB	
INL integral nonlinearity error		—	±16.0	±32.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.
Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 5.41 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007, AN021	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN007 and AN021 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN008 to AN015		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	

Table 5.42 A/D Internal Reference Voltage Characteristics

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V*1, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.
Note 2. The A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the A/D converter.

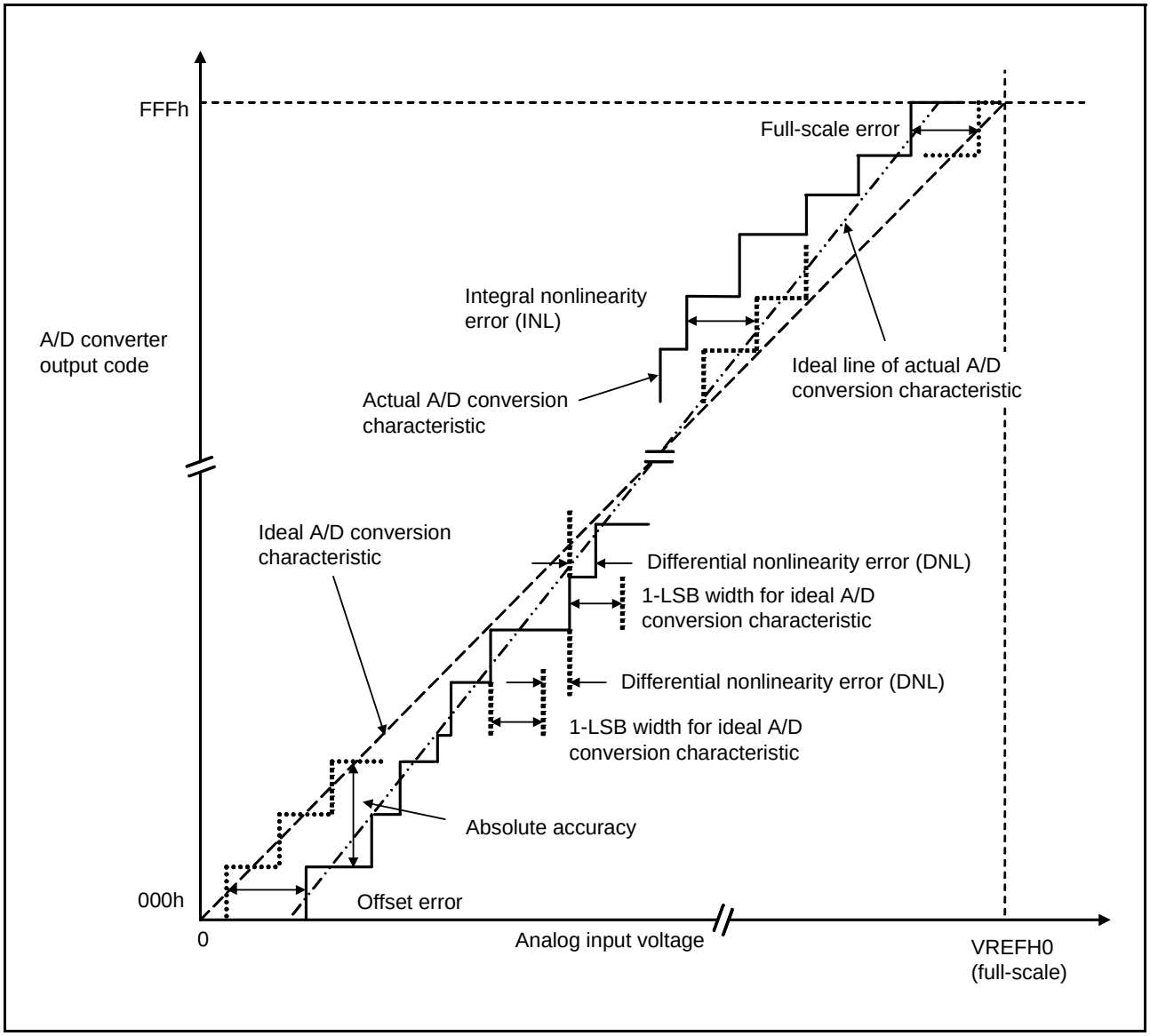


Figure 5.57 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Table 5.45 D/A Conversion Characteristics (3)

Conditions: 2.0 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.0 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C
Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential nonlinearity error	—	±2.0	±16.0	LSB	
INL integral nonlinearity error	—	±8.0	±16.0	LSB	
Offset error	—	—	±30	mV	
Output resistance	—	75	—	Ω	
Conversion time	—	—	30	μs	

5.9.3 Capacitor Split Method

Table 5.54 Capacitor Split Method

Conditions: 2.2 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.2 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected between CAPH and CAPL pins	C1	0.33	0.47	0.61	µF	
External capacitor connected to V_{L1} pin	C2	0.33	0.47	0.61	µF	
External capacitor connected to V_{L2} pin	C3	0.33	0.47	0.61	µF	
External capacitor connected to V_{L3} pin	C4	0.33	0.47	0.61	µF	
External capacitor connected to V_{L4} pin	C5	0.33	0.47	0.61	µF	

(1) 1/3 Bias Method

Table 5.55 Capacitor Split Method LCD Characteristics

Conditions: 2.2 V ≤ VCC = VCC_USB ≤ 3.6 V, 2.2 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Conditions
V_{L4} voltage*1	V_{L4}	C1 to C4 connected	—	VCC	—	V	
V_{L2} voltage*1	V_{L2}	C1 to C4 connected	$2/3V_{L4}$-0.07	$2/3V_{L4}$	$2/3V_{L4}$+0.07	V	
V_{L1} voltage**1	V_{L1}	C1 to C4 connected	$1/3V_{L4}$-0.08	$2/3V_{L4}$	$2/3V_{L4}$+0.08	V	
Capacitor split wait time*1	t_{WAIT}		100	—	—	ms	

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

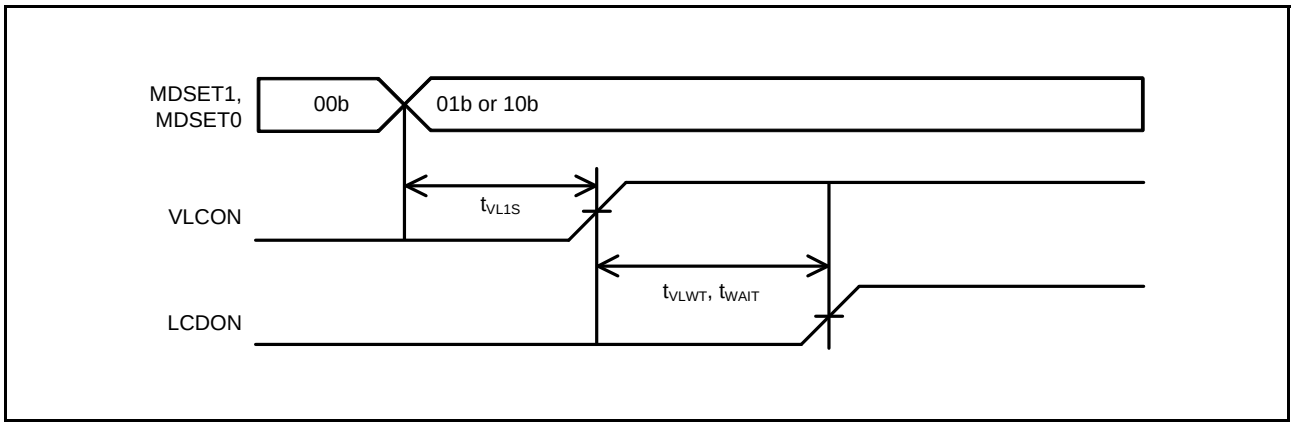


Figure 5.61 LCD Reference Voltage Setup Time, Voltage Boosting Wait Time, and Capacitor Split Wait Time

5.10 CTSU Characteristics

Table 5.56 CTSU Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V, T_a = –40 to +105°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	

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