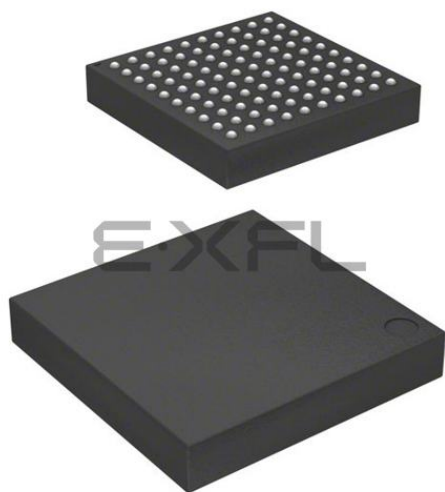




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Last Time Buy
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SCI, SPI, SSI, USB OTG
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f51138adlj-30

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
DMA	Data transfer controller (DTCa)	- Transfer modes: Normal transfer, repeat transfer, and block transfer - Activation sources: Interrupts - Chain transfer function
I/O ports	General I/O ports	100-pin /64-pin - I/O: 82/46 - Input: 2/2 - Pull-up resistors: 69/38 - Open-drain outputs: 61/34 5-V tolerance: 4/4
Event link controller (ELC)		- Event signals of 44 types can be directly connected to the module - Operations of timer modules are selectable at event input - Capable of event link operation for port B
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	(16 bits × 6 channels) × 1 unit - Time bases for the six 16-bit timer channels can be provided via up to 16 pulse-input/output lines and three pulse-input lines - Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. - Input capture function 21 output compare/input capture registers - Pulse output mode - Complementary PWM output mode - Reset synchronous PWM mode - Phase-counting mode - Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	(16 bits × 2 channels) × 2 units - Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	14 bits × 1 channel - Count clock: Dedicated low-speed on-chip oscillator for the IWDT - Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCA)	- Clock source: Sub-clock - Calendar count mode or binary count mode selectable - Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPT)	16 bits × 1 channel - Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT - Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	(8 bits × 2 channels) × 2 units - Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected - Pulse output and PWM output with any duty cycle are available - Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIE, SCIf)	8 channels (channel 0, 1, 2, 5, 6, 8, and 9: SCIE, channel 12: SCIf) - Serial communications modes: Asynchronous, clock synchronous, and smart card interface - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Average transfer rate clock can be input from MTU2 timers - Simple I²C - Simple SPI - Master/slave mode supported (SCIf only) - Start frame and information frame are included (SCIf only) - Start-bit detection in asynchronous mode: Low level or falling edge is selectable
	IrDA interface (IRDA)	1 channel (SCI5 used) - Supports encoding/decoding of waveforms conforming to IrDA standard 1.0
	I ² C bus interface (RIIC)	1 channel - Communications formats: - I²C bus format/SMBus format - Master mode or slave mode selectable - Supports fast mode

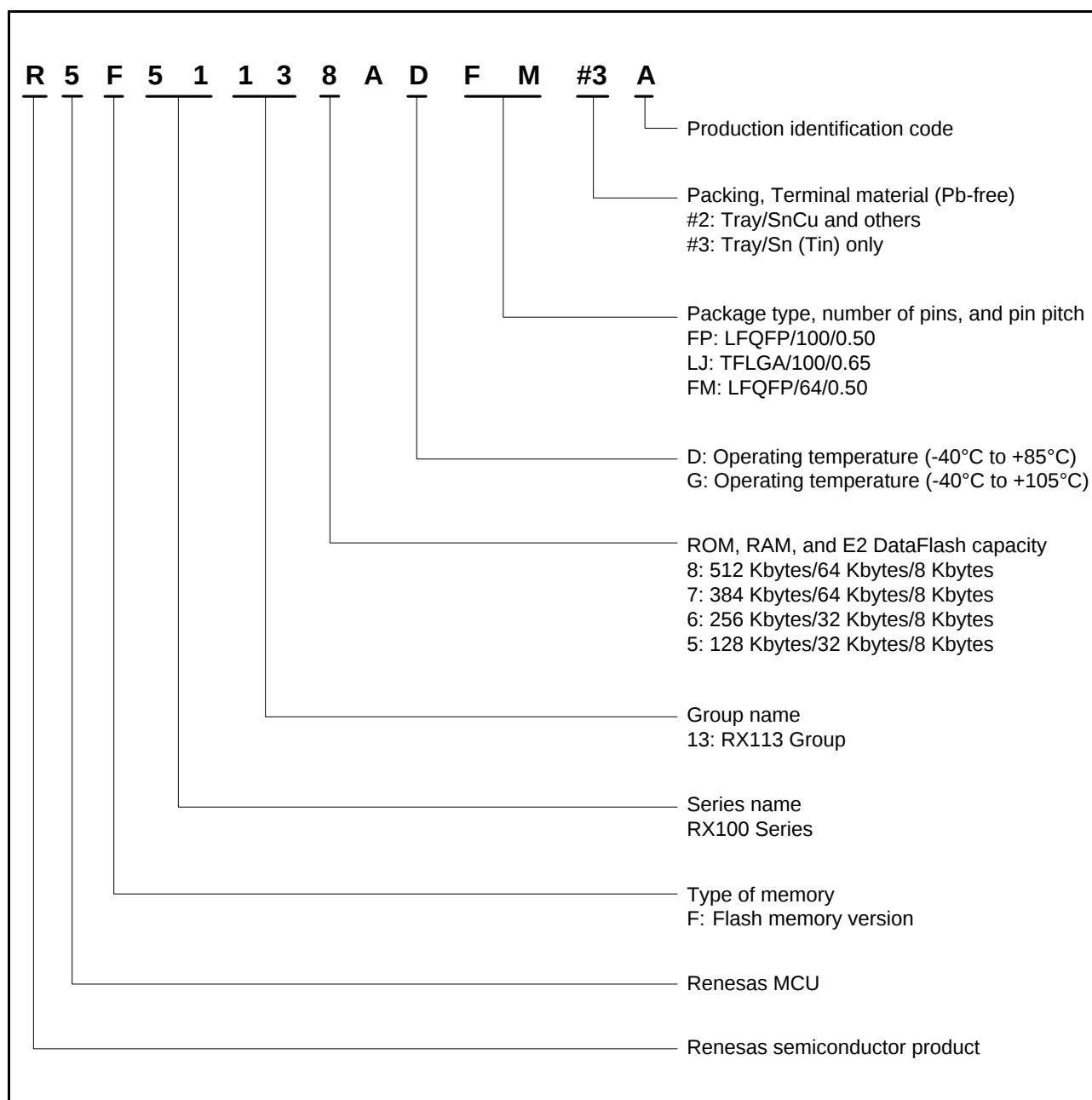


Figure 1.1 How to Read the Product Part No., Memory Capacity, and Package Type

1.3 Block Diagram

Figure 1.2 shows a block diagram.

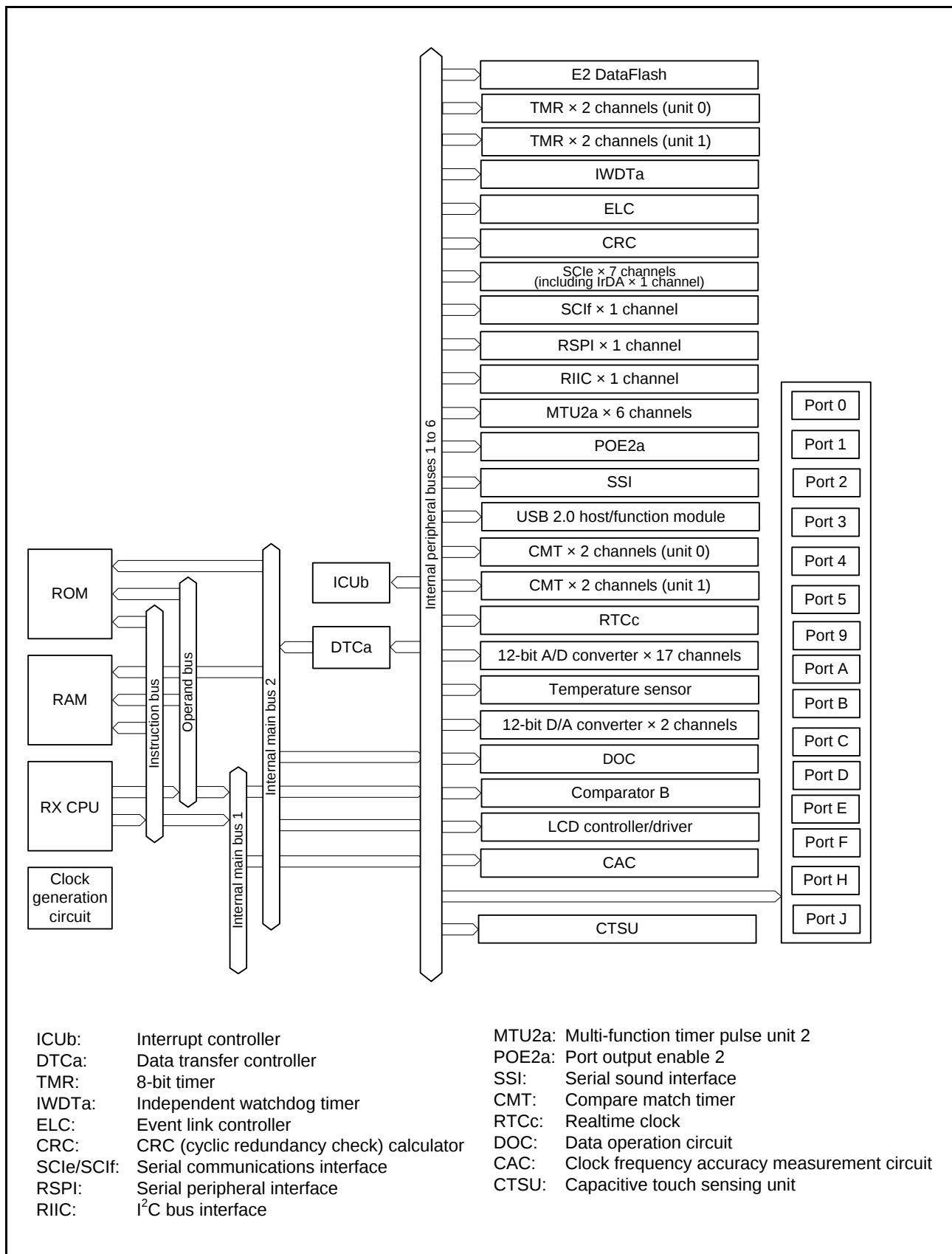


Figure 1.2 Block Diagram

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCle, SCIf, RSPI, RiIC, USB, SSI)	LCD, Touch	Others
1		P04	MTIOC0A/POE2#/TMC13	SCK6	TS1	
2		PJ0				DA0
3		P02	MTIOC0D/POE3#/TMR13	RXD6/SMISO6/SSCL6	TS2	
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#	TS3	
5		P25	MTIOC4C/MTCLKB		TS4	ADTRG0#
6		P24	MTIOC4A/MTCLKA/TMR11		TS5	
7		P23	MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#	TS6	
8		P22	MTIOC3B/MTCLKC/TMO0	SCK0	TS7	
9		P21	MTIOC1B/TMC10	RXD0/SMISO0/SSCL0	TS8	
10		P20	MTIOC1A/TMR10	TXD0/SMOSI0/SSDA0	TS9	
11		P27	MTIOC2B/TMC13	SCK12/SCK1/RXD6/SMISO6/SSCL6	TS10	IRQ3/ADTRG0#/ CACREF/ CMPA2
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/TXD6/SMOSI6/ SSDA6	TSCAP	
13		P30	MTIOC4B/POE8#/TMR13	RXD1/SMISO1/SSCL1	CAPH	IRQ0
14		P31	MTIOC4D/TMC12	CTS1#/RTS1#/SS1#	CAPL	IRQ1
15	MD					FINED
16	RES#					
17	XCOUT					
18	XCIN	PH7				
19	UPSEL	P35				NMI
20	XTAL					
21	EXTAL					
22	VCL					
23	VSS					
24	VDD					
25		P32	MTIOC0C/RTCOUT/TMO3	TXD6/SMOSI6/SSDA6/CTS6#/ RTS6#/SS6#	TS11	IRQ2
26		P17	MTIOC0C/MTIOC3A/ MTIOC3B/POE8#/TMO1	SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12		IRQ7
27		P16	MTIOC3C/MTIOC3D/ RTCOUT/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB		IRQ6/ADTRG0#
28		P15	MTIOC0B/MTCLKB/TMC12	RXD1/SMISO1/SSCL1/RSPCKA		IRQ5/CLKOUT/ CACREF
29	UB#	P14	MTIOC0A/MTIOC3A/ MTCLKA/TMR12	CTS1#/RTS1#/SS1#/SSLA0/ TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12/USB0_OVRCURA		IRQ4
30	VCC_USB					
31				USB0_DM		
32				USB0_DP		
33	VSS_USB					
34		P13	MTIOC0B/TMO3	CTS12#/RTS12#/SS12#/CTS0#/ RTS0#/SS0#	SEG00	IRQ3
35		P12	TMC11	SCK12/SCK0	SEG01	IRQ2

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, POE, RTC, TMR)	Communication (SCIE, SCIF, RSPI, RIIC, USB, SSI)	LCD, Touch	Others
68		PA2		RXD5/SMISO5/SSCL5/IRRXD5/SSLA3	SEG22	
69		PA1	MTIOC0B/MTCLKC/RTCOUT	SCK5/SSLA2	SEG23	
70		PA0	MTIOC4A	SSLA1	SEG24	CACREF
71		PF7	MTIOC3A		SEG25	
72		PF6	MTIOC3C		SEG26	
73		PE5	MTIOC2B/MTIOC4C	MISOA/TXD9/SMOSI9/SSDA9	SEG27	IRQ5/AN013/CMPOB1
74		PE4	MTIOC1A/MTIOC3A/MTIOC4D	MOSIA/RXD9/SMISO9/SSCL9/SSIWS0	SEG28	IRQ4/AN012
75		PE3	MTIOC0A/MTIOC1B/MTIOC4B/POE8#	CTS12#/RTS12#/SS12#/RSPCKA/SCK9/AUDIO_MCLK	SEG29	IRQ3/AN011
76		PE2	MTIOC4A	RXD12/RXD12/SMISO12/SSCL12/SSIRXD0	SEG30	IRQ7/AN010/CVREFB0
77		PE1	MTIOC4C	TXD12/TXD12/SIOX12/SMOSI12/SSDA12/SSITXD0	SEG31	IRQ1/AN009/CMPB0
78		PE0	MTIOC2A/POE3#	SCK12/CTS9#/RTS9#/SS9#/SSISCK0	SEG32	IRQ0/AN008
79		PE7			SEG33	IRQ7/AN015/CMPOB0
80		PE6			SEG34	IRQ6/AN014
81		PD4	POE3#		SEG35	IRQ4
82		PD3	POE8#		SEG36	IRQ3
83		PD2	MTIOC4D		SEG37	IRQ2
84		PD1	MTIOC4B		SEG38	IRQ1
85		PD0			SEG39	IRQ0
86		P92*2				AN021
87		P91*2				AN007
88		P46*2				AN006
89		P90*2				AN005
90		P44*2				AN004
91		P43*2				AN003
92	VREFL	P42*2				AN002
93	VREFH	P41*2				AN001
94	VREFL0	PJ7*2				
95		P40*2				AN000
96	VREFH0	PJ6*2				
97	AVSS0					
98	AVCC0					
99		P07		TXD6/SMOSI6/SSDA6	TS0	ADTRG0#
100		PJ2				DA1

Note 1. Not 5 V tolerant.

Note 2. The power source of the I/O buffer for these pins is AVCC0.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 001Ch	SYSTEM	Module Stop Control Register D	MSTPCRD	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 002Ch	SYSTEM	USB-dedicated PLL Control Register	UPLLCR	16	16	3 ICLK
0008 002Eh	SYSTEM	USB-dedicated PLL Control Register 2	UPLLCR2	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0033h	SYSTEM	Sub-Clock Oscillator Control Register	SOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 003Eh	SYSTEM	CLKOUT Output Control Register	CKOCR	16	16	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 0050h	SYSTEM	LCD Source Clock Control Register	LCDSCLKCR	8	8	3 ICLK
0008 0051h	SYSTEM	LCD Source Clock Control Register 2	LCDSCLKCR2	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00AAh	SYSTEM	Sub Operating Power Control Register	SOPCCR	8	8	3 ICLK
0008 00B0h	LPT	Low-power Timer Control Register 1	LPTCR1	8	8	3 ICLK
0008 00B1h	LPT	Low-power Timer Control Register 2	LPTCR2	8	8	3 ICLK
0008 00B2h	LPT	Low-power Timer Control Register 3	LPTCR3	8	8	3 ICLK
0008 00B4h	LPT	Low-Power Timer Cycle Setting Register	LPTPRD	16	16	3 ICLK
0008 00B8h	LPT	Low-Power Timer Compare Register 0	LPCMR0	16	16	3 ICLK
0008 00BCh	LPT	Low-Power Timer Standby Wakeup Enable Register	LPWUCR	16	16	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (15/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 or 3 PCLKB
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 or 3 PCLKB
0008 B10Fh	ELC	Event Link Setting Register 14	ELSR14	8	8	2 or 3 PCLKB
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 or 3 PCLKB
0008 B112h	ELC	Event Link Setting Register 17	ELSR17	8	8	2 or 3 PCLKB
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 or 3 PCLKB
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2 or 3 PCLKB
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 or 3 PCLKB
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 or 3 PCLKB
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 or 3 PCLKB
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 or 3 PCLKB
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 or 3 PCLKB
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 or 3 PCLKB
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 or 3 PCLKB
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 or 3 PCLKB
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 or 3 PCLKB
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 or 3 PCLKB
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 or 3 PCLKB
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 or 3 PCLKB
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 or 3 PCLKB
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 or 3 PCLKB
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 B309h	SCI12	I ² C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 B30Ah	SCI12	I ² C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 B30Bh	SCI12	I ² C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 B30Ch	SCI12	I ² C Status Register	SISR	8	8	2 or 3 PCLKB
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 B320h	SCI12	Extended Serial Mode Enable Register	ESMER	8	8	2 or 3 PCLKB
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 or 3 PCLKB
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 or 3 PCLKB
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 or 3 PCLKB
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 or 3 PCLKB
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 or 3 PCLKB
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 or 3 PCLKB
0008 B327h	SCI12	Status Register	STR	8	8	2 or 3 PCLKB
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 or 3 PCLKB
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 or 3 PCLKB
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 or 3 PCLKB
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 or 3 PCLKB
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 or 3 PCLKB
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 or 3 PCLKB
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 or 3 PCLKB
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 or 3 PCLKB
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (20/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
0008 C402h	RTC	Binary Counter 0	BCNT0	8	8	2 or 3 PCLKB
0008 C404h	RTC	Minute Counter	RMINCNT	8	8	2 or 3 PCLKB
0008 C404h	RTC	Binary Counter 1	BCNT1	8	8	2 or 3 PCLKB
0008 C406h	RTC	Hour Counter	RHRCNT	8	8	2 or 3 PCLKB
0008 C406h	RTC	Binary Counter 2	BCNT2	8	8	2 or 3 PCLKB
0008 C408h	RTC	Day-Of-Week Counter	RWKCNT	8	8	2 or 3 PCLKB
0008 C408h	RTC	Binary Counter 3	BCNT3	8	8	2 or 3 PCLKB
0008 C40Ah	RTC	Date Counter	RDAYCNT	8	8	2 or 3 PCLKB
0008 C40Ch	RTC	Month Counter	RMONCNT	8	8	2 or 3 PCLKB
0008 C40Eh	RTC	Year Counter	RYRCNT	16	16	2 or 3 PCLKB
0008 C410h	RTC	Second Alarm Register	RSECAR	8	8	2 or 3 PCLKB
0008 C410h	RTC	Binary Counter 0 Alarm Register	BCNT0AR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Minute Alarm Register	RMINAR	8	8	2 or 3 PCLKB
0008 C412h	RTC	Binary Counter 1 Alarm Register	BCNT1AR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Hour Alarm Register	RHRAR	8	8	2 or 3 PCLKB
0008 C414h	RTC	Binary Counter 2 Alarm Register	BCNT2AR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Day-of-Week Alarm Register	RWKAR	8	8	2 or 3 PCLKB
0008 C416h	RTC	Binary Counter 3 Alarm Register	BCNT3AR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Date Alarm Register	RDAYAR	8	8	2 or 3 PCLKB
0008 C418h	RTC	Binary Counter 0 Alarm Enable Register	BCNT0AER	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Month Alarm Register	RMONAR	8	8	2 or 3 PCLKB
0008 C41Ah	RTC	Binary Counter 1 Alarm Enable Register	BCNT1AER	8	8	2 or 3 PCLKB
0008 C41Ch	RTC	Year Alarm Register	RYRAR	16	16	2 or 3 PCLKB
0008 C41Ch	RTC	Binary Counter 2 Alarm Enable Register	BCNT2AER	16	16	2 or 3 PCLKB
0008 C41Eh	RTC	Year Alarm Enable Register	RYRAREN	8	8	2 or 3 PCLKB
0008 C41Eh	RTC	Binary Counter 3 Alarm Enable Register	BCNT3AER	8	8	2 or 3 PCLKB
0008 C422h	RTC	RTC Control Register 1	RCR1	8	8	2 or 3 PCLKB
0008 C424h	RTC	RTC Control Register 2	RCR2	8	8	2 or 3 PCLKB
0008 C426h	RTC	RTC Control Register 3	RCR3	8	8	2 or 3 PCLKB
0008 C42Eh	RTC	Time Error Adjustment Register	RADJ	8	8	2 or 3 PCLKB
0008 C580h	CMPB	Comparator B Control Register 1	CPBCNT1	8	8	2 or 3 PCLKB
0008 C581h	CMPB	Comparator B Control Register 2	CPBCNT2	8	8	2 or 3 PCLKB
0008 C582h	CMPB	Comparator B Flag Register	CPBFLG	8	8	2 or 3 PCLKB
0008 C583h	CMPB	Comparator B Interrupt Control Register	CPBINT	8	8	2 or 3 PCLKB
0008 C584h	CMPB	Comparator B Filter Select Register	CPBF	8	8	2 or 3 PCLKB
0008 C585h	CMPB	Comparator B Mode Select Register	CPBMD	8	8	2 or 3 PCLKB
0008 C586h	CMPB	Comparator B Reference Input Voltage Select Register	CPBREF	8	8	2 or 3 PCLKB
0008 C587h	CMPB	Comparator B Output Control Register	CPBOCR	8	8	2 or 3 PCLKB
000A 0000h	USB0	System Configuration Control Register	SYSCFG	16	16	3 or 4 PCLKB
000A 0004h	USB0	System Configuration Status Register 0	SYSSTS0	16	16	9 PCLK or more
000A 0008h	USB0	Device State Control Register 0	DVSTCTR0	16	16	9 PCLK or more
000A 0014h	USB0	CFIFO Port Register	CFIFO	16	16	3 or 4 PCLKB
000A 0018h	USB0	D0FIFO Port Register	D0FIFO	16	16	3 or 4 PCLKB
000A 001Ch	USB0	D1FIFO Port Register	D1FIFO	16	16	3 or 4 PCLKB
000A 0020h	USB0	CFIFO Port Select Register	CFIFOSEL	16	16	3 or 4 PCLKB
000A 0028h	USB0	D0FIFO Port Select Register	D0FIFOSEL	16	16	3 or 4 PCLKB
000A 002Ch	USB0	D1FIFO Port Select Register	D1FIFOSEL	16	16	3 or 4 PCLKB
000A 0022h	USB0	CFIFO Port Control Register	CFIFOCTR	16	16	3 or 4 PCLKB
000A 002Ah	USB0	D0FIFO Port Control Register	D0FIFOCTR	16	16	3 or 4 PCLKB
000A 002Eh	USB0	D1FIFO Port Control Register	D1FIFOCTR	16	16	3 or 4 PCLKB
000A 0030h	USB0	Interrupt Enable Register 0	INTENB0	16	16	9 PCLKB or more
000A 0032h	USB0	Interrupt Enable Register 1	INTENB1	16	16	9 PCLKB or more

Table 4.1 List of I/O Registers (Address Order) (23/23)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States
000A 0912h	CTSU	CTSU High-Pass Noise Spectrum Diffusion Control Register	CTSUSSC	16	16	1 or 2 PCLKB
000A 0914h	CTSU	CTSU Sensor Offset Register 0	CTSUSO0	16	16	1 or 2 PCLKB
000A 0916h	CTSU	CTSU Sensor Offset Register 1	CTSUSO1	16	16	1 or 2 PCLKB
000A 0918h	CTSU	CTSU Sensor Counter	CTSUSC	16	16	1 or 2 PCLKB
000A 091Ah	CTSU	CTSU Reference Counter	CTSURC	16	16	1 or 2 PCLKB
000A 091Ch	CTSU	CTSU Error Status Register	CTSUERRS	16	16	1 or 2 PCLKB
007F C090h	FLASH	E2 DataFlash Control Register	DFCTL	8	8	2 or 3 FCLK
007F C0ACh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRL	8	8	1 or 2 PCLKB
007F C0ADh	TEMPS	Temperature Sensor Calibration Data Register	TSCDRH	8	8	1 or 2 PCLKB
007F C0B0h	FLASH	Flash Start-Up Setting Monitor Register	FSCMR	16	16	2 or 3 FCLK
007F C0B2h	FLASH	Flash Access Window Start Address Monitor	FAWSMR	16	16	2 or 3 FCLK
007F C0B4h	FLASH	Flash Access Window End Address Monitor Register	FAWEMR	16	16	2 or 3 FCLK
007F C0B6h	FLASH	Flash Initial Setting Register	FISR	8	8	2 or 3 FCLK
007F C0B7h	FLASH	Flash Extra Area Control Register	FEXCR	8	8	2 or 3 FCLK
007F C0B8h	FLASH	Flash Error Address Monitor Register L	FEAML	16	16	2 or 3 FCLK
007F C0BAh	FLASH	Flash Error Address Monitor Register H	FEAMH	8	8	2 or 3 FCLK
007F C0C0h	FLASH	Protection Unlock Register	FPR	8	8	2 or 3 FCLK
007F C0C1h	FLASH	Protection Unlock Status Register	FPSR	8	8	2 or 3 FCLK
007F C0C2h	FLASH	Flash Read Buffer Register L	FRBL	16	16	2 or 3 FCLK
007F C0C4h	FLASH	Flash Read Buffer Register H	FRBH	16	16	2 or 3 FCLK
007F FF80h	FLASH	Flash P/E Mode Control Register	FPMCR	8	8	2 or 3 FCLK
007F FF81h	FLASH	Flash Area Select Register	FASR	8	8	2 or 3 FCLK
007F FF82h	FLASH	Flash Processing Start Address Register L	FSARL	16	16	2 or 3 FCLK
007F FF84h	FLASH	Flash Processing Start Address Register H	FSARH	8	8	2 or 3 FCLK
007F FF85h	FLASH	Flash Control Register	FCR	8	8	2 or 3 FCLK
007F FF86h	FLASH	Flash Processing End Address Register L	FEARL	16	16	2 or 3 FCLK
007F FF88h	FLASH	Flash Processing End Address Register H	FEARH	8	8	2 or 3 FCLK
007F FF89h	FLASH	Flash Reset Register	FRESETR	8	8	2 or 3 FCLK
007F FF8Ah	FLASH	Flash Status Register 0	FSTATR0	8	8	2 or 3 FCLK
007F FF8Bh	FLASH	Flash Status Register 1	FSTATR1	8	8	2 or 3 FCLK
007F FF8Ch	FLASH	Flash Write Buffer Register L	FWBL	16	16	2 or 3 FCLK
007F FF8Eh	FLASH	Flash Write Buffer Register H	FWBH	16	16	2 or 3 FCLK
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 or 3 FCLK

Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMRO or TMR2 register. Table 22.4 lists register allocation for 16-bit access in the User's Manual: Hardware.

Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCTL register. Table 30.6 lists register allocation for 16-bit access in the User's Manual: Hardware.

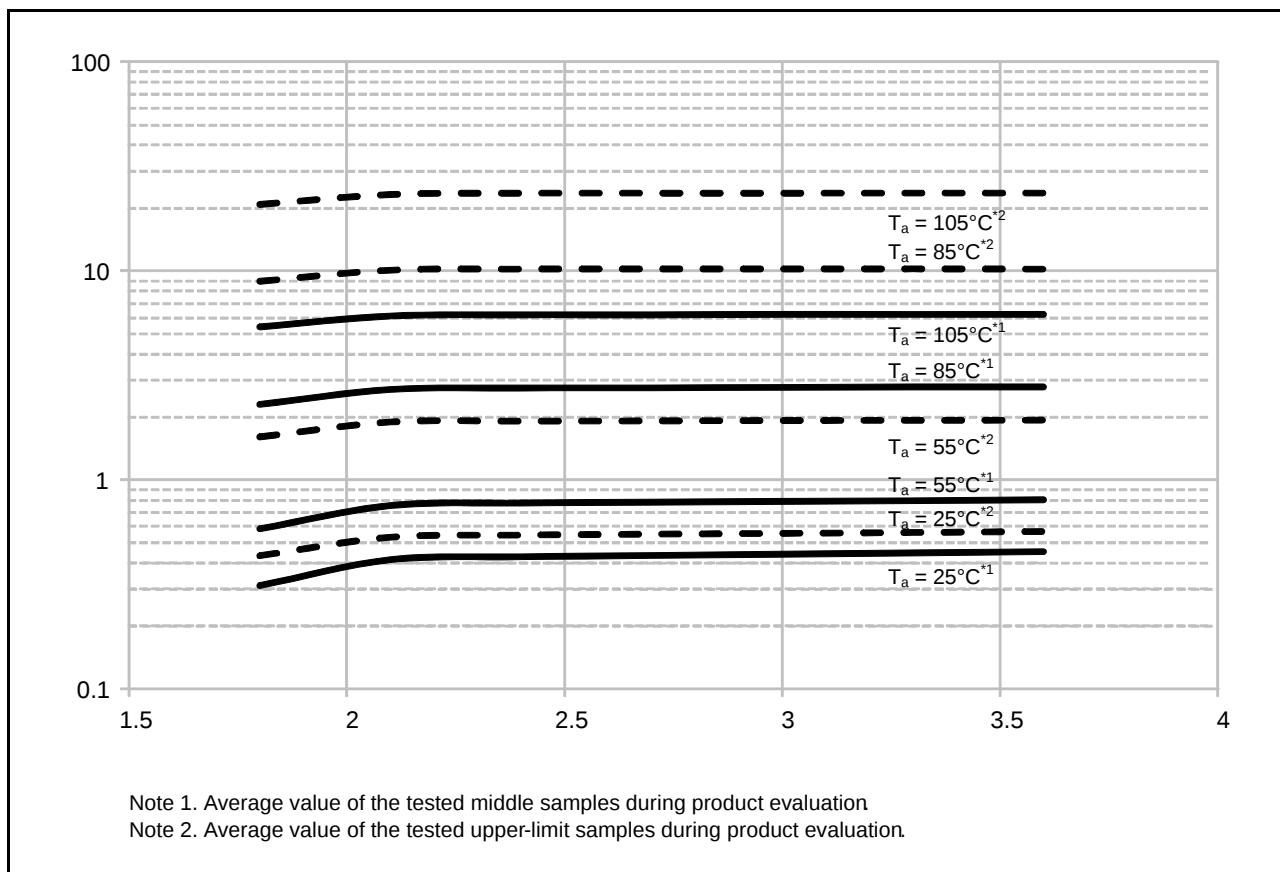


Figure 5.4 Voltage Dependency in Software Standby Mode (Reference Data)

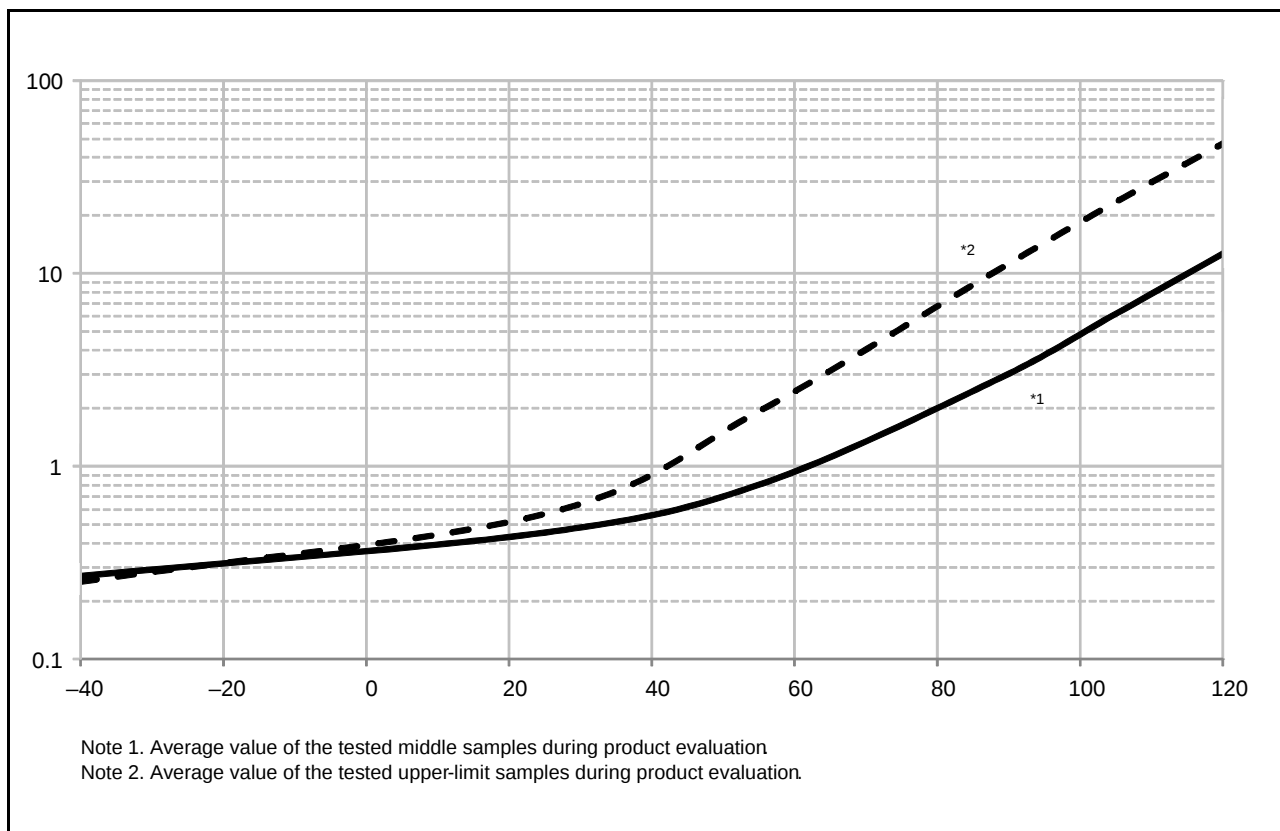


Figure 5.5 Temperature Dependency in Software Standby Mode (Reference Data)

5.2.2 Standard I/O Pin Output Characteristics (2)

Figure 5.11 to Figure 5.13 show the characteristics of the RIIC output pin.

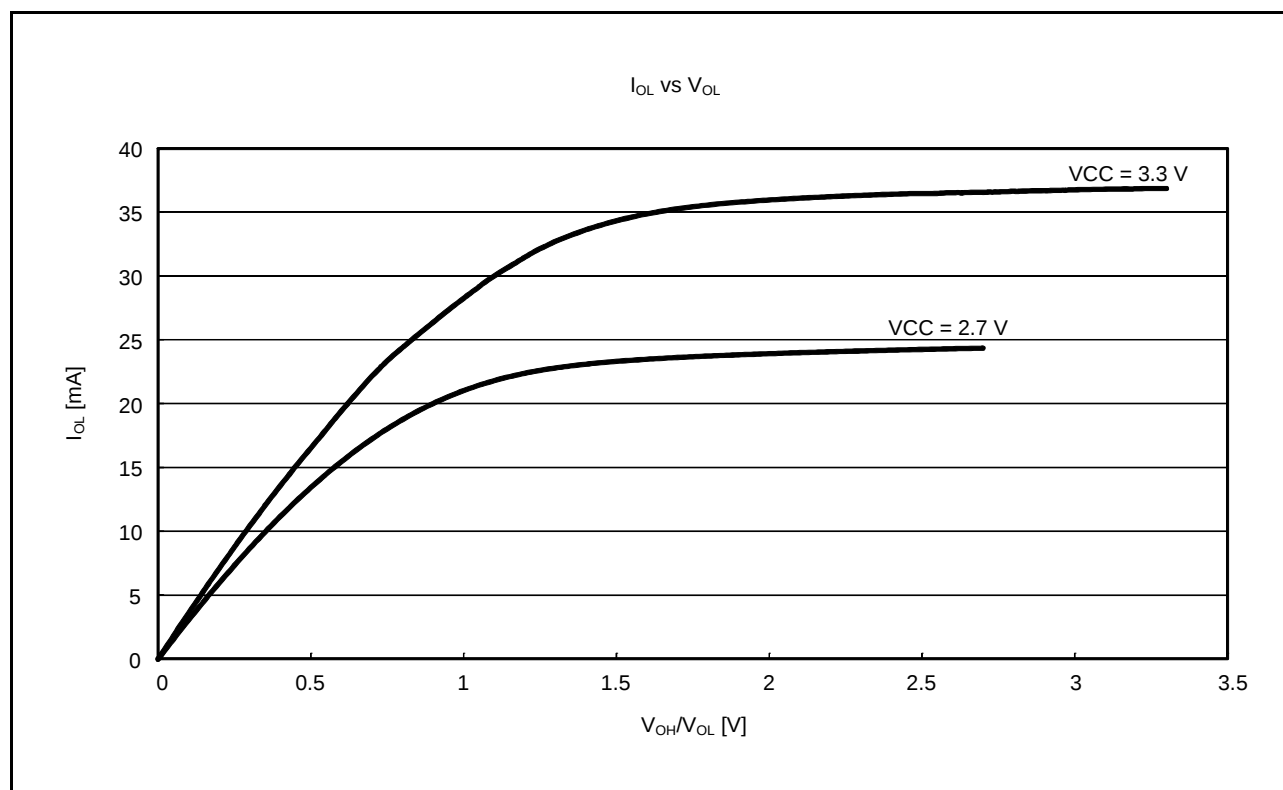


Figure 5.11 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

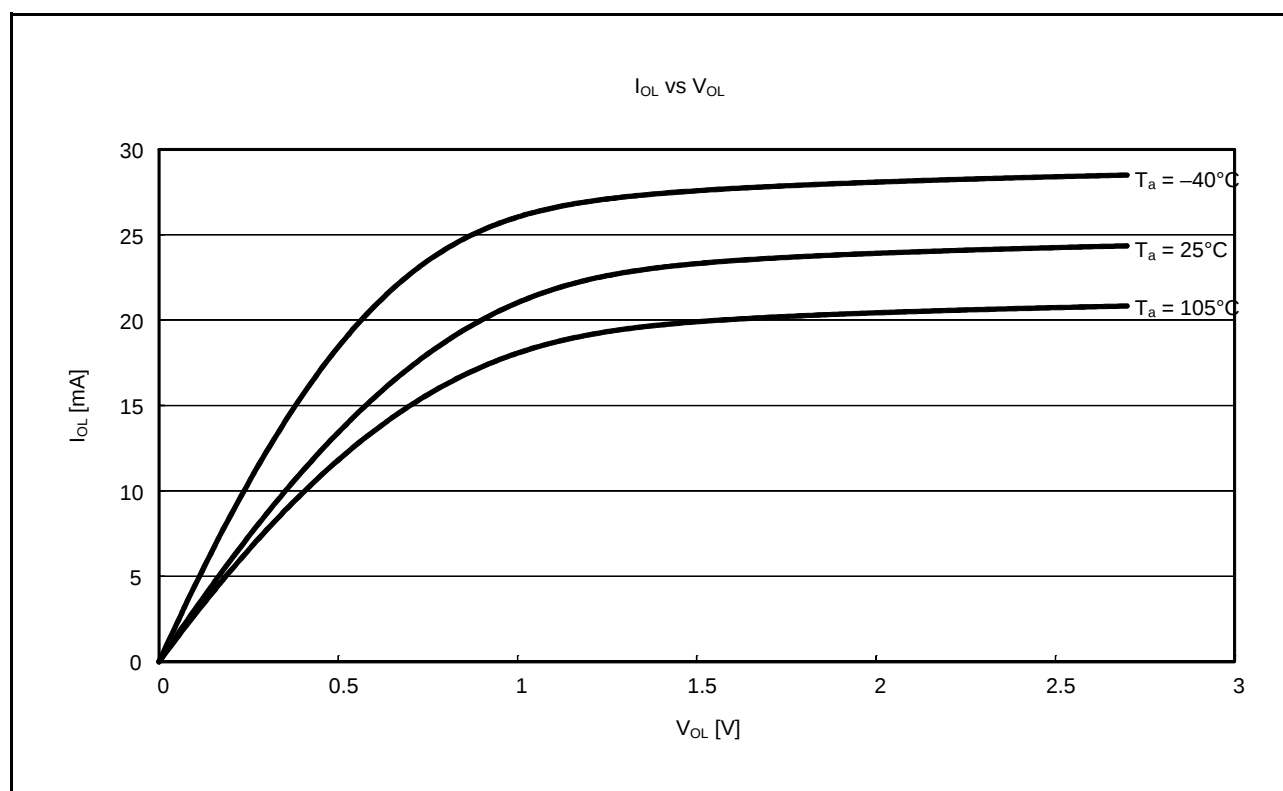


Figure 5.12 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

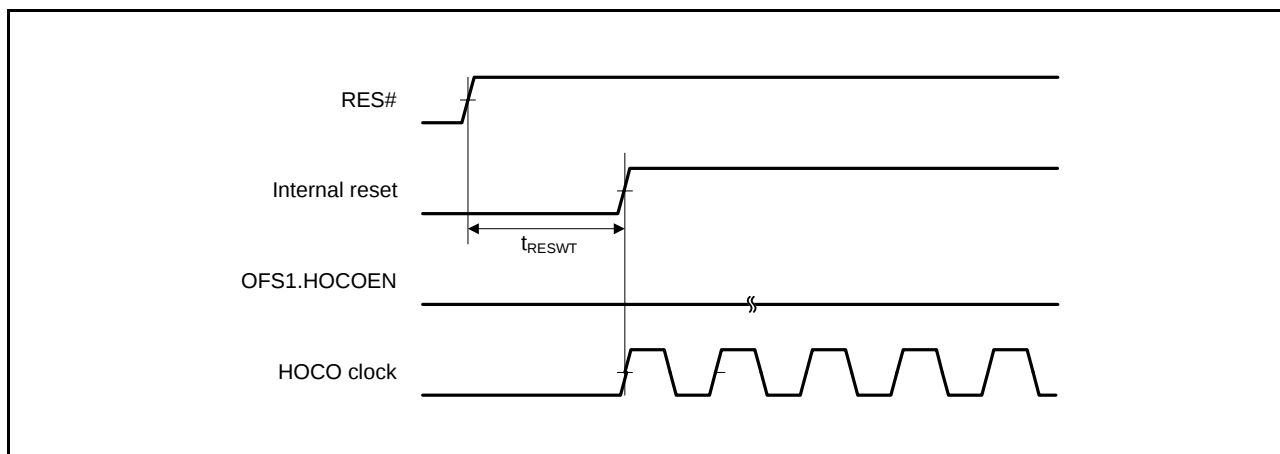


Figure 5.22 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

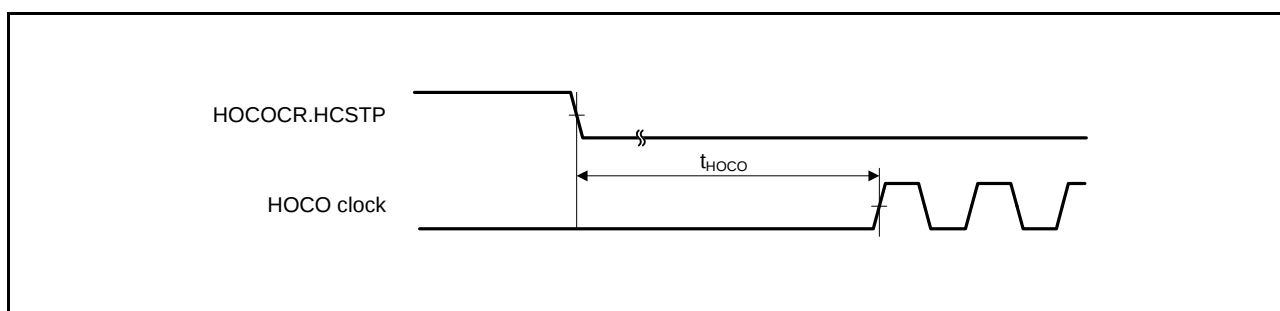


Figure 5.23 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

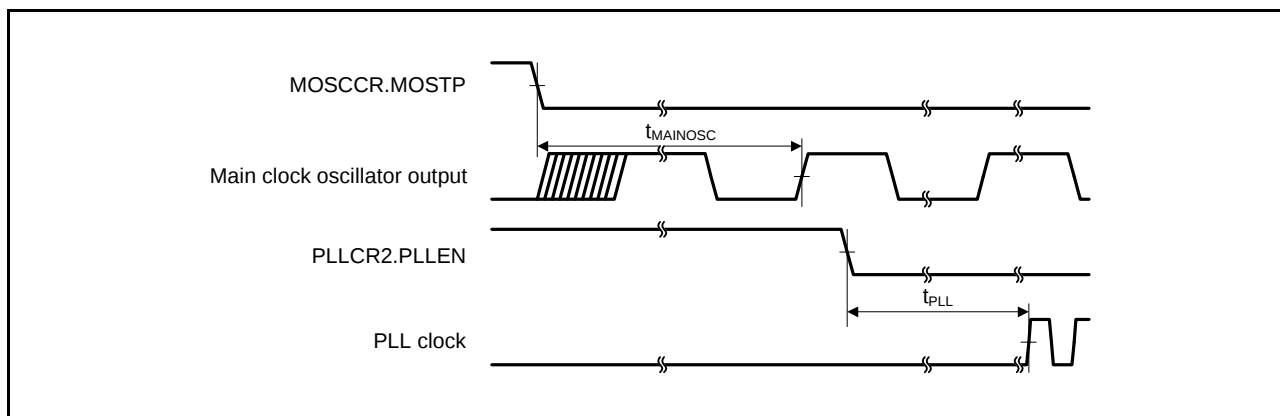


Figure 5.24 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

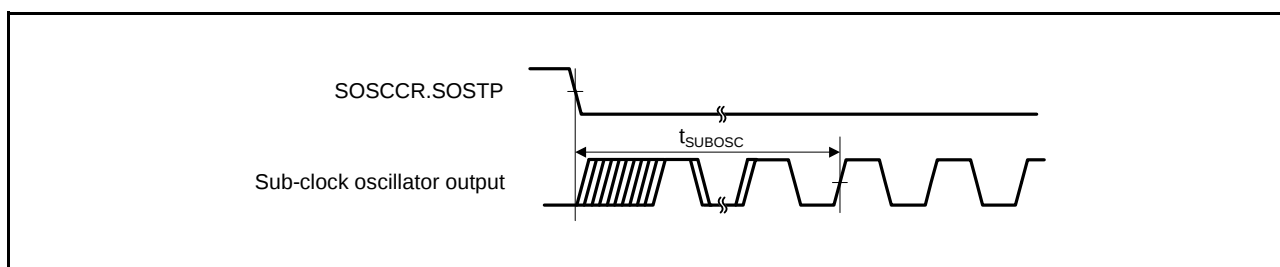


Figure 5.25 Sub-Clock Oscillation Start Timing

Note 6. When the frequency of HOCO is 8 MHz.

When the high-speed clock oscillator wait control register (HOCOWTCR) is set to 05h.

Table 5.26 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	μs	Figure 5.29

Note: When the division ratios of PCLKB, PCLKD, FCLK, and ICLK are all set to 1.

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

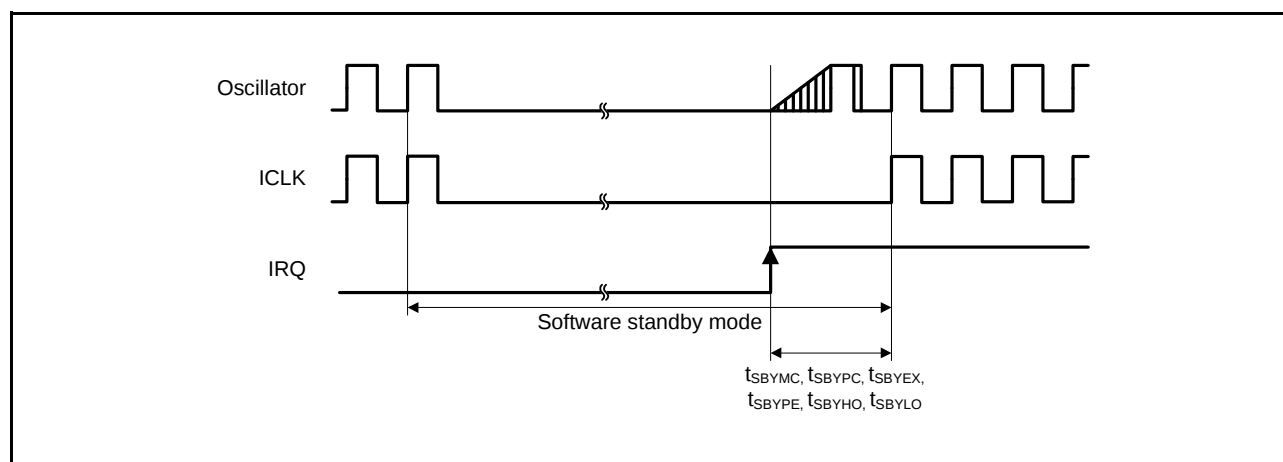


Figure 5.29 Software Standby Mode Recovery Timing

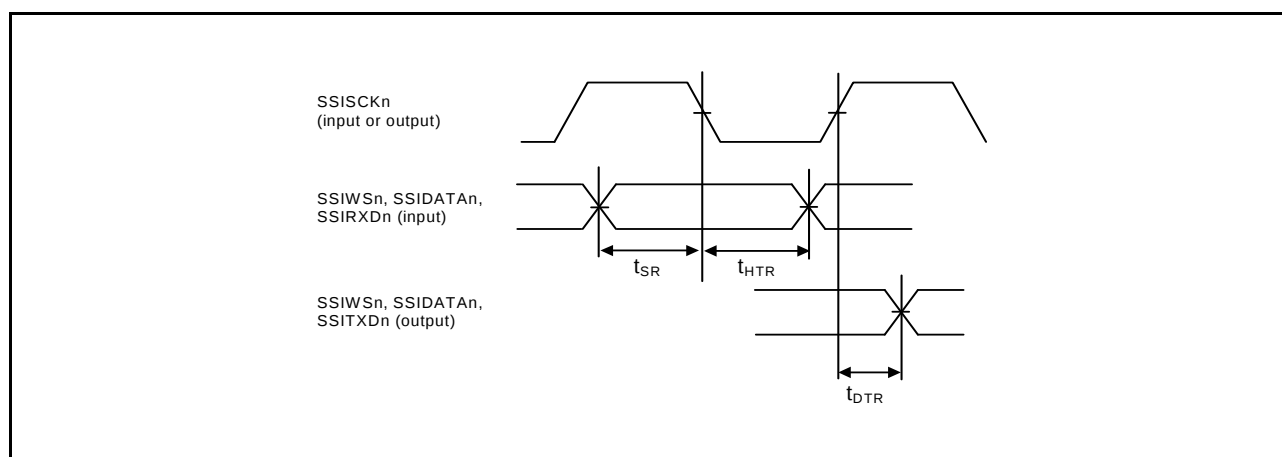


Figure 5.52 Transmission/Reception Timing (Synchronized with SSISCKn Falling Edge)

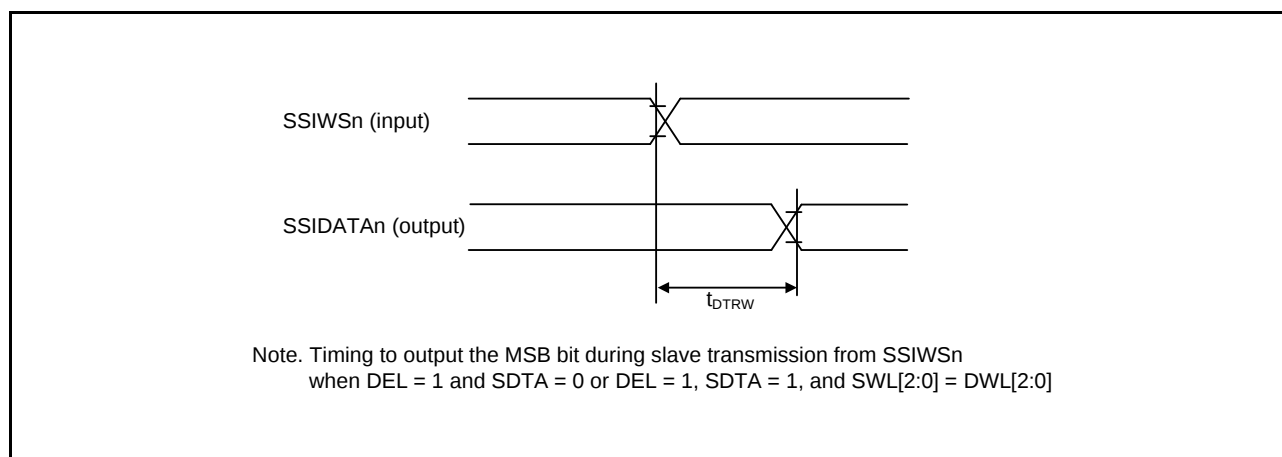


Figure 5.53 SSIDATA Output Delay After SSIWSn Changing Edge

5.7 Temperature Sensor Characteristics

Table 5.46 Temperature Sensor Characteristics

Conditions: $2.0\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $2.0\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	± 1.5	—	$^\circ\text{C}$	2.4 V or above
		—	± 2.0	—		Below 2.4 V
Temperature slope	—	—	-3.65	—	mV/ $^\circ\text{C}$	
Output voltage (25 $^\circ\text{C}$)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	μs	
Sampling time	—	5	—	—	μs	

5.8 Comparator Characteristics

Table 5.47 Comparator Characteristics

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB0 or CVREFB1 input reference voltage		VREF	0	—	VCC - 1.4	V	
CMPB0 or CMPB1 input voltage		VI	-0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	μs	VCC = 3 V, input slew rate $\geq 50\text{ mV}/\mu\text{s}$
	Comparator high-speed mode Window function enabled	Tdw	—	—	2	μs	
	Comparator low-speed mode	Td	—	—	5	μs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	μs	

5.9 LCD Characteristics

5.9.1 External Resistance Division Method

(1) Static Display Mode

Table 5.48 LCD Characteristics

Conditions: $2.0\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.0\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.0	—	VCC	V	

(2) 1/2 Bias Method, 1/4 Bias Method

Table 5.49 LCD Characteristics

Conditions: $2.7\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.7\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.7	—	VCC	V	

(3) 1/3 Bias Method

Table 5.50 LCD Characteristics

Conditions: $2.5\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $2.5\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LCD drive voltage	V_{L4}	2.5	—	VCC	V	

5.10 CTSU Characteristics

Table 5.56 CTSU Characteristics

Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	

5.11 Power-On Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.57 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (1)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	1.35	1.50	1.65	V	Figure 5.62, Figure 5.63
	Voltage detection circuit (LVD1)*1	V _{det1_4}	3.00	3.10	3.20	V	Figure 5.64 At falling edge VCC
		V _{det1_5}	2.91	3.00	3.09		
		V _{det1_6}	2.81	2.90	2.99		
		V _{det1_7}	2.70	2.79	2.88		
		V _{det1_8}	2.60	2.68	2.76		
		V _{det1_9}	2.50	2.58	2.66		
		V _{det1_A}	2.40	2.48	2.56		
		V _{det1_B}	1.99	2.06	2.13		
		V _{det1_C}	1.90	1.96	2.02		
		V _{det1_D}	1.80	1.86	1.92		

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD2), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol $V_{\text{det1_n}}$ denotes the value of the LVDLVL.R.LVD1LVL[3:0] bits.

Table 5.58 Power-On Reset Circuit and Voltage Detection Circuit Characteristics (2)Conditions: $1.8\text{ V} \leq \text{VCC} = \text{VCC_USB} \leq 3.6\text{ V}$, $1.8\text{ V} \leq \text{AVCC0} \leq 3.6\text{ V}$, $\text{VSS} = \text{AVSS0} = \text{VSS_USB} = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Voltage detection circuit (LVD2)*1	V _{det2_0}	2.71	2.90	3.09	V	Figure 5.65 At falling edge VCC
		V _{det2_1}	2.43	2.60	2.77		
		V _{det2_2}	1.87	2.00	2.13		
		V _{det2_3} *2	1.69	1.80	1.91		
Wait time after power-on reset cancellation	At normal startup*3	t _{POR}	—	9.1	—	ms	Figure 5.63
	During fast startup time*4	t _{POR}	—	1.6	—		
Wait time after voltage monitoring 1 reset cancellation	Power-on voltage monitoring 1 reset disabled*3	t _{LVD1}	—	568	—	μs	Figure 5.64
	Power-on voltage monitoring 1 reset enabled*4		—	100	—		
Wait time after voltage monitoring 2 reset cancellation		t _{LVD2}	—	100	—	μs	Figure 5.65
Response delay time		t _{det}	—	—	350	μs	Figure 5.62
Minimum VCC down time*5		t _{VOFF}	350	—	—	μs	Figure 5.62, VCC = 1.0 V or above
Power-on reset enable time		t _W (POR)	1	—	—	ms	Figure 5.63, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		T _d (E-A)	—	—	300	μs	Figure 5.64, Figure 5.65
Hysteresis width (LVD1 and LVD2)		V _{LVH}	—	70	—	mV	Vdet1_4 selected
			—	60	—		Vdet1_5 to 9, LVD2 selected
			—	50	—		When selection is from among Vdet1_A to B.
			—	40	—		When selection is from among Vdet1_C to D.

Note: These characteristics apply when noise is not superimposed on the power supply. When a setting is made so that the voltage detection level overlaps with that of the voltage detection circuit (LVD1), it cannot be specified which of LVD1 and LVD2 is used for voltage detection.

Note 1. n in the symbol $V_{\text{det2_n}}$ denotes the value of the LVDLVL.R.LVD2LVL[3:0] bits.

Note 2. Vdet2_3 selection can be used only when the CMPA2 pin input voltage is selected and cannot be used when the power supply voltage (VCC) is selected.

Note 3. When $\text{OFS1}(\text{STUPLVD1REN}, \text{FASTSTUP}) = 11\text{b}$.

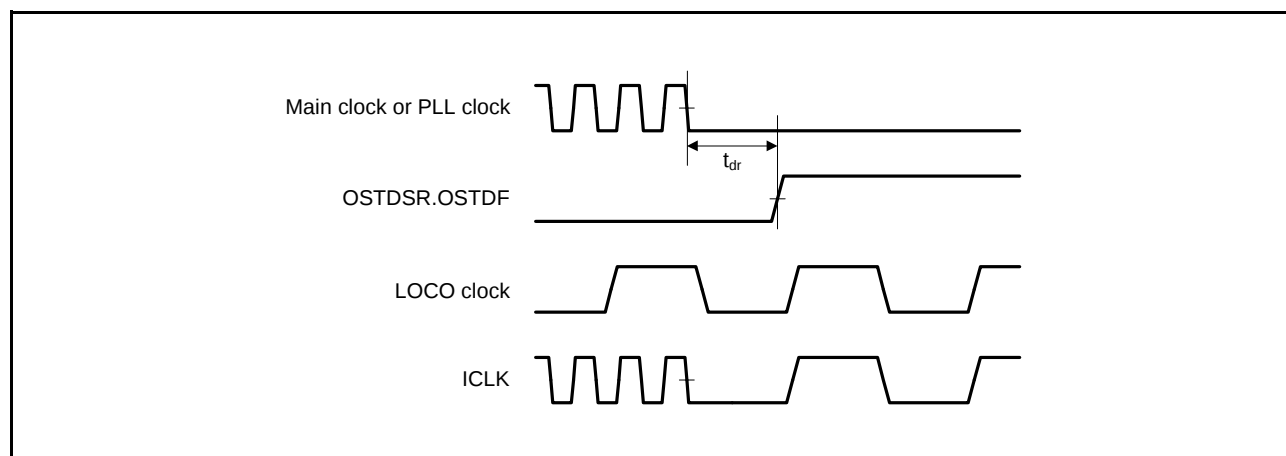
Note 4. When $\text{OFS1}(\text{STUPLVD1REN}, \text{FASTSTUP}) \neq 11\text{b}$.

Note 5. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

5.12 Oscillation Stop Detection Timing

Table 5.59 Oscillation Stop Detection Circuit CharacteristicsConditions: $1.8\text{ V} \leq VCC = VCC_USB \leq 3.6\text{ V}$, $1.8\text{ V} \leq AVCC0 \leq 3.6\text{ V}$, $VSS = AVSS0 = VSS_USB = 0\text{ V}$, $T_a = -40\text{ to }+105^\circ\text{C}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.66

**Figure 5.66 Oscillation Stop Detection Timing**

5.14 E2 DataFlash Characteristics

Table 5.63 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N _{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N _{DPEC}	t _{DDRP}	20*2, *3	—	—	Year	T _a = +85°C
	After 100000 times of N _{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N _{DPEC}		—	1*2, *3	—	Year	T _a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.

Note 3. These results are obtained from reliability testing.

**Table 5.64 E2 DataFlash Characteristics (2)
: high-speed operating mode**

Conditions: 2.7 V ≤ VCC ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = −40 to +105°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t _{DP1}	—	86	761	—	40.5	374	μs
Erasure time	1-Kbyte	t _{DE1K}	—	17.4	456	—	6.15	228	ms
	8-Kbyte	t _{DE8K}	—	60.4	499	—	9.3	231	ms
Blank check time	1-byte	t _{DBC1}	—	—	48	—	—	15.9	μs
	1-Kbyte	t _{DBC1K}	—	—	1.58	—	—	0.127	ms
Erase operation forcible stop time		t _{DSER}	—	—	21.5	—	—	12.8	μs
DataFlash STOP recovery time		t _{DSTOP}	5	—	—	5	—	—	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.

**Table 5.65 E2 DataFlash Characteristics (3)
: middle-speed operating mode**

Conditions: 1.8 V ≤ VCC ≤ 3.6 V, 1.8 V ≤ AVCC0 ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = −40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t _{DP1}	—	126	1160	—	85.4	818	μs
Erasure time	1-Kbyte	t _{DE1K}	—	17.5	457	—	7.76	259	ms
	8-Kbyte	t _{DE8K}	—	60.5	500	—	16.7	267.6	ms
Blank check time	1-byte	t _{DBC1}	—	—	78	—	—	50	μs
	1-Kbyte	t _{DBC1K}	—	—	1.61	—	—	0.369	ms
Erase operation forcible stop time		t _{DSER}	—	—	33.5	—	—	25.5	μs
DataFlash STOP recovery time		t _{DSTOP}	720	—	—	720	—	—	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%. Confirm the frequency accuracy of the clock source.