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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4/M0 |
| Core Size | 32-Bit Dual-Core |
| Speed | 204MHz |
| Connectivity | CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, WDT |
| Number of I/O | 49 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 16K x 8 |
| RAM Size | 104K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.2V ~ 3.6V |
| Data Converters | A/D 4x10b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TFBGA |
| Supplier Device Package | 100-TFBGA (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4313jet100e |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P2_2 | M15 | F5 | 121 | 84 | [2] | N; PU | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **U0_UCLK —** Serial clock input/output for USART0 in synchronous mode. |
| | | | | | | | I/O | **EMC_A11 —** External memory address line 11. |
| | | | | | | | O | **USB0_IND1 —** USB0 port indicator LED control output 1. |
| | | | | | | | I/O | **GPIO5[2] —** General purpose digital input/output pin. |
| | | | | | | | I | **CTIN_6 —** SCT input 6. Capture input 1 of timer 3. |
| | | | | | | | I | **T3_CAP2 —** Capture input 2 of timer 3. |
| | | | | | | | O | **EMC_CS1 —** LOW active Chip Select 1 signal. |
| P2_3 | J12 | D8 | 127 | 87 | [3] | N; PU | I/O | **SGPIO12 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2C1_SDA —** I$^2$C1 data input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. See Table 4 for ISP mode. |
| | | | | | | | I | **CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2. |
| | | | | | | | I/O | **GPIO5[3] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT0 —** Match output 0 of timer 3. |
| | | | | | | | O | **USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH).<br>Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts. |
| P2_4 | K11 | D9 | 128 | 88 | [3] | N; PU | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2C1_SCL —** I$^2$C1 clock input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. See Table 4 for ISP mode. |
| | | | | | | | I | **CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3. |
| | | | | | | | I/O | **GPIO5[4] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT1 —** Match output 1 of timer 3. |
| | | | | | | | I | **USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition). |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P4_0 | D5 | - | 1 | 1 | [2] | N; PU | I/O | **GPIO2[0] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCOA0 —** Motor control PWM channel 0, output A. |
| | | | | | | | I | **NMI —** External interrupt input to NMI. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD13 —** LCD data. |
| | | | | | | | I/O | **U3_UCLK —** Serial clock input/output for USART3 in synchronous mode. |
| | | | | | | | - | **R —** Function reserved. |
| P4_1 | A1 | - | 3 | 3 | [5] | N; PU | I/O | **GPIO2[1] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_1 —** SCT output 1. Match output 3 of timer 3. |
| | | | | | | | O | **LCD_VD0 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | O | **U3_TXD —** Transmitter output for USART3. |
| | | | | | | | I | **ENET_COL —** Ethernet Collision detect (MII interface). |
| | | | | | | | AI | **ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| P4_2 | D3 | - | 12 | 8 | [2] | N; PU | I/O | **GPIO2[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_0 —** SCT output 0. Match output 0 of timer 0. |
| | | | | | | | O | **LCD_VD3 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD12 —** LCD data. |
| | | | | | | | I | **U3_RXD —** Receiver input for USART3. |
| | | | | | | | I/O | **SGPIO8 —** General purpose digital input/output pin. |
| P4_3 | C2 | - | 10 | 7 | [5] | N; PU | I/O | **GPIO2[3] —** General purpose digital input/output pin. |
| | | | | | | | O | **CTOUT_3 —** SCT output 3. Match output 3 of timer 0. |
| | | | | | | | O | **LCD_VD2 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD21 —** LCD data. |
| | | | | | | | I/O | **U3_BAUD —** Baud pin for USART3. |
| | | | | | | | I/O | **SGPIO9 —** General purpose digital input/output pin. |
| | | | | | | | AI | **ADC0_0 —** DAC, ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P8_2 | K4 | - | 36 | - | [3] | N; PU | I/O | **GPIO4[2] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB0_IND0 —** USB0 port indicator LED control output 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **MCI0 —** Motor control PWM channel 0, input. |
| | | | | | | | I/O | **SGPIO10 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT2 —** Match output 2 of timer 0. |
| P8_3 | J3 | - | 37 | - | [2] | N; PU | I/O | **GPIO4[3] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D2 —** ULPI link bidirectional data line 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD12 —** LCD data. |
| | | | | | | | O | **LCD_VD19 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T0_MAT3 —** Match output 3 of timer 0. |
| P8_4 | J2 | - | 39 | - | [2] | N; PU | I/O | **GPIO4[4] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D1 —** ULPI link bidirectional data line 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD7 —** LCD data. |
| | | | | | | | O | **LCD_VD16 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP0 —** Capture input 0 of timer 0. |
| P8_5 | J1 | - | 40 | - | [2] | N; PU | I/O | **GPIO4[5] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB1_ULPI_D0 —** ULPI link bidirectional data line 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD6 —** LCD data. |
| | | | | | | | O | **LCD_VD8 —** LCD data. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP1 —** Capture input 1 of timer 0. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| P8_6 | K3 | - | 43 | - | [2] | N; PU | I/O | **GPIO4[6] —** General purpose digital input/output pin. |
| | | | | | | | I | **USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD5 —** LCD data. |
| | | | | | | | O | **LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP2 —** Capture input 2 of timer 0. |
| P8_7 | K1 | - | 45 | - | [2] | N; PU | I/O | **GPIO4[7] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD4 —** LCD data. |
| | | | | | | | O | **LCD_PWR —** LCD panel power enable. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T0_CAP3 —** Capture input 3 of timer 0. |
| P8_8 | L1 | - | 49 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **CGU_OUT0 —** CGU spare clock output 0. |
| | | | | | | | O | **I2S1_TX_MCLK —** I2S1 transmit master clock. |
| P9_0 | T1 | - | 59 | - | [2] | N; PU | I/O | **GPIO4[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **MCABORT —** Motor control PWM, LOW-active fast abort. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_CRS —** Ethernet Carrier Sense (MII interface). |
| | | | | | | | I/O | **SGPIO0 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PC_6 | H6 | - | 22 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D2 —** ULPI link bidirectional data line 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RXD2 —** Ethernet receive data 2 (MII interface). |
| | | | | | | | I/O | **GPIO6[5] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP3 —** Capture input 3 of timer 3. |
| | | | | | | | I/O | **SD_DAT2 —** SD/MMC data bus line 2. |
| PC_7 | G5 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D1 —** ULPI link bidirectional data line 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RXD3 —** Ethernet receive data 3 (MII interface). |
| | | | | | | | I/O | **GPIO6[6] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT0 —** Match output 0 of timer 3. |
| | | | | | | | I/O | **SD_DAT3 —** SD/MMC data bus line 3. |
| PC_8 | N4 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **USB1_ULPI_D0 —** ULPI link bidirectional data line 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface). |
| | | | | | | | I/O | **GPIO6[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT1 —** Match output 1 of timer 3. |
| | | | | | | | I | **SD_CD —** SD/MMC card detect input. |
| PC_9 | K2 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **ENET_RX_ER —** Ethernet receive error (MII interface). |
| | | | | | | | I/O | **GPIO6[8] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT2 —** Match output 2 of timer 3. |
| | | | | | | | O | **SD_POW —** SD/MMC power monitor output. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PC_14 | N1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART 1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[13] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **SGPIO13 —** General purpose digital input/output pin. |
| | | | | | | | O | **ENET_TX_ER —** Ethernet Transmit Error (MII interface). |
| | | | | | | | I/O | **SD_DAT7 —** SD/MMC data bus line 7. |
| PD_0 | N2 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_15 —** SCT output 15. Match output 3 of timer 3. |
| | | | | | | | O | **EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[14] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO4 —** General purpose digital input/output pin. |
| PD_1 | P1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **EMC_CKEOUT2 —** SDRAM clock enable 2. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[15] —** General purpose digital input/output pin. |
| | | | | | | | O | **SD_POW —** SD/MMC power monitor output. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| PD_2 | R1 | - | - | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_7 —** SCT output 7. Match output 3 of timer 1. |
| | | | | | | | I/O | **EMC_D16 —** External memory data line 16. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **GPIO6[16] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PE_6 | M16 | - | 124 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_2 —** SCT output 2. Match output 2 of timer 0. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART 1. |
| | | | | | | | I/O | **EMC_D25 —** External memory data line 25. |
| | | | | | | | I/O | **GPIO7[6] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_7 | F15 | - | 149 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_5 —** SCT output 5. Match output 3 of timer 3. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART1. |
| | | | | | | | I/O | **EMC_D26 —** External memory data line 26. |
| | | | | | | | I/O | **GPIO7[7] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_8 | F14 | - | 150 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | O | **CTOUT_4 —** SCT output 4. Match output 3 of timer 3. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART 1. |
| | | | | | | | I/O | **EMC_D27 —** External memory data line 27. |
| | | | | | | | I/O | **GPIO7[8] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| PE_9 | E16 | - | 152 | - | [2] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I | **CTIN_4 —** SCT input 4. Capture input 2 of timer 1. |
| | | | | | | | I | **U1_DCD —** Data Carrier Detect input for UART 1. |
| | | | | | | | I/O | **EMC_D28 —** External memory data line 28. |
| | | | | | | | I/O | **GPIO7[9] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |

**Table 3. Pin description** *…continued*

| Pin name | LBGA256 | TFBGA100 | LQFP208 | LQFP144 | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|---|---|
| PF_6 | E7 | - | 192 | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | O | **TRACEDATA[1] —** Trace data, bit 1. |
| | | | | | | | I/O | **GPIO7[20] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO5 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*. |
| | | | | | | | AI | **ADC1_3 —** ADC1 and ADC0, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_7 | B7 | - | 193 | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U3_BAUD —** Baud pin for USART3. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave in for SSP1. |
| | | | | | | | O | **TRACEDATA[2] —** Trace data, bit 2. |
| | | | | | | | I/O | **GPIO7[21] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO6 —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*. |
| | | | | | | | AI/ O | **ADC1_7 —** ADC1 and ADC0, input channel 7 or band gap output. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |
| PF_8 | E6 | - | - | - | [5] | N; PU | - | **R —** Function reserved. |
| | | | | | | | I/O | **U0_UCLK —** Serial clock input/output for USART0 in synchronous mode. |
| | | | | | | | I | **CTIN_2 —** SCT input 2. Capture input 2 of timer 0. |
| | | | | | | | O | **TRACEDATA[3] —** Trace data, bit 3. |
| | | | | | | | I/O | **GPIO7[22] —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SGPIO7 —** General purpose digital input/output pin. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | AI | **ADC0_2 —** ADC0 and ADC1, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC. |

## 7.5 AHB multilayer matrix

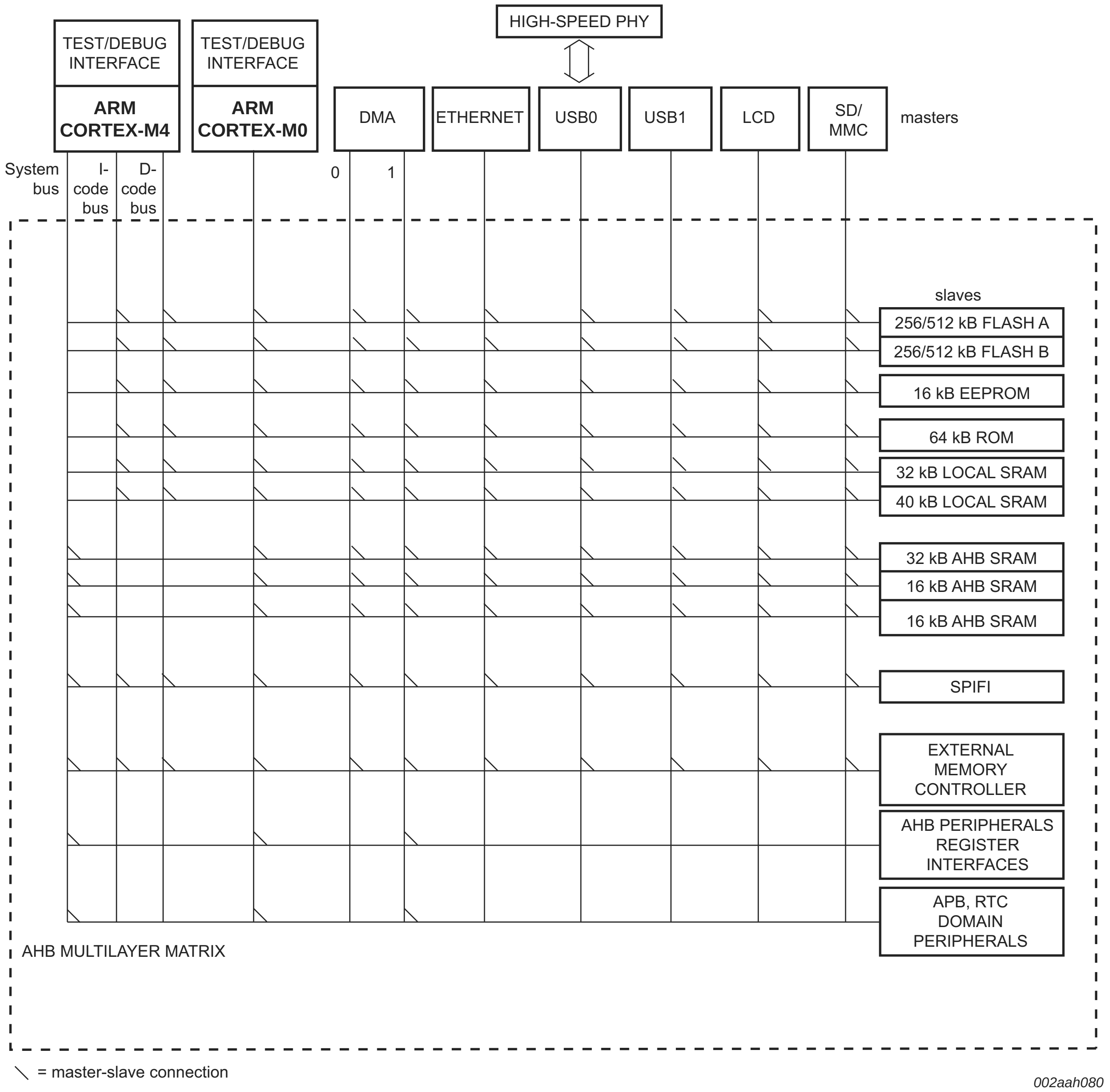



**Fig 6. AHB multilayer matrix master and slave connections**

## 7.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The ARM Cortex-M0 co-processor has its own NVIC with 32 vectored interrupts. Most peripheral interrupts are shared between the Cortex-M0 and Cortex-M4 NVICs.

### 7.6.1 Features

- ARM Cortex-M4 core:
  - Controls system exceptions and peripheral interrupts
  - Support for up to 53 vectored interrupts
  - Eight programmable interrupt priority levels with hardware priority level masking
  - Relocatable vector table
  - Non-Maskable Interrupt (NMI)
  - Software interrupt generation
- ARM Cortex-M0 core:
  - Support for up to 32 interrupts
  - Four programmable interrupt priority levels with hardware priority level masking

### 7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

## 7.7 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

**Remark:** The SysTick is not included in the ARM Cortex-M0 core implementation.

## 7.8 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts.
- C_CAN0/1 and QEI interrupts.
- Ethernet, USB0, USB1 signals.
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3).

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

#### 7.20.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

### 7.20.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

### 7.20.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

#### 7.20.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.

### 7.23.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

### 7.23.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC435x/3x/2x/1x.

### 7.23.9 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC435x/3x/2x/1x support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
   a. Deep-sleep mode
   b. Power-down mode
   c. Deep power-down mode

Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

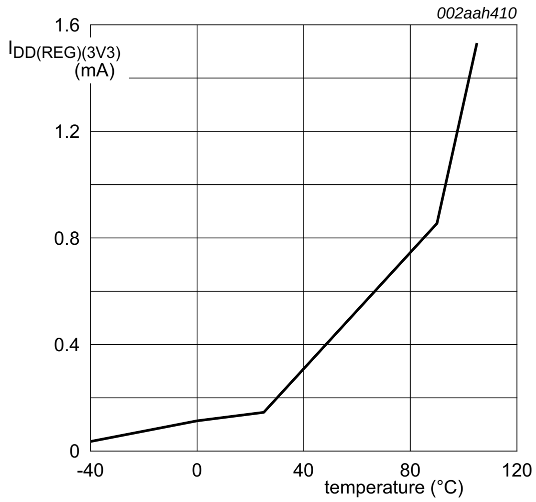
Wake-up from sleep mode is caused by an interrupt or event in the core's NVIC. The interrupt is captured in the NVIC and an event is captured in the Event router. Both cores can wake up from sleep mode independently of each other.

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot.

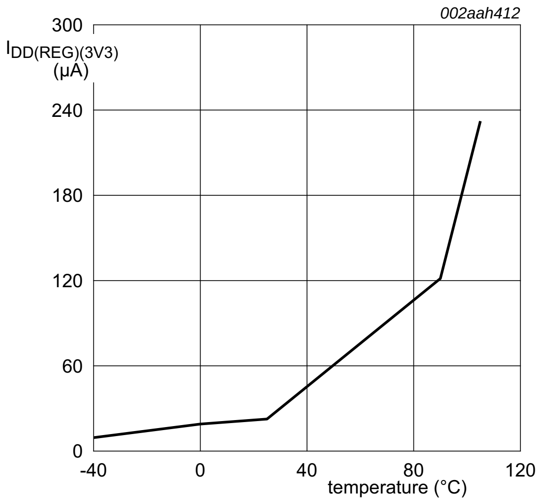
### 7.23.10 Power control

The LPC435x/3x/2x/1x feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.



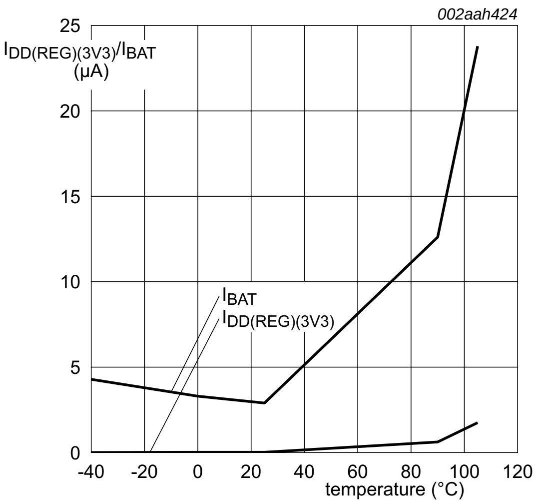

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

**Fig 15. Typical supply current versus temperature in Deep-sleep mode**



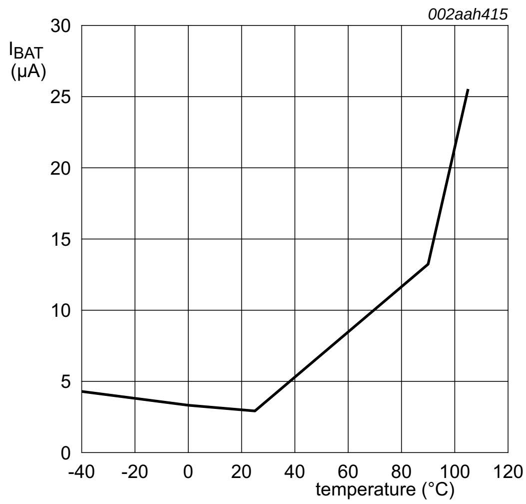

Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

**Fig 16. Typical supply current versus temperature in Power-down mode**




Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V. $V_{BAT} = V_{DD(REG)(3V3)} + 0.4$ V.

**Fig 17. Typical supply current versus temperature in Deep power-down mode**




Conditions: $V_{BAT} = 3.6$ V. $V_{DD(REG)(3V3)}$ not present.

**Fig 18. Typical battery supply current versus temperature**

## 11.2 Wake-up times

**Table 17. Dynamic characteristic: Wake-up from Deep-sleep, Power-down, and Deep power-down modes**

*$T_{amb}$ = −40 °C to +105 °C*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{wake}$ | wake-up time | from Sleep mode | [2] | 3 × $T_{cy(clk)}$ | 5 × $T_{cy(clk)}$ | - | ns |
| | | from Deep-sleep and Power-down mode | | 12 | 51 | - | μs |
| | | from Deep power-down mode | | - | 200 | - | μs |
| | | after reset | | - | 200 | - | μs |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{cy(clk)}$ = 1/CCLK with CCLK = CPU clock frequency.

## 11.3 External clock for oscillator in slave mode

**Remark:** The input voltage on the XTAL1/2 pins must be ≤ 1.2 V (see Table 11). For connecting the oscillator to the XTAL pins, also see Section 13.2 and Section 13.4.

**Table 18. Dynamic characteristic: external clock**

*$T_{amb}$ = −40 °C to +105 °C; $V_{DD(IO)}$ over specified ranges.[1]*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | | | 1 | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | | | 40 | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | | | $T_{cy(clk)}$ × 0.4 | $T_{cy(clk)}$ × 0.6 | ns |
| $t_{CLCX}$ | clock LOW time | | | $T_{cy(clk)}$ × 0.4 | $T_{cy(clk)}$ × 0.6 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

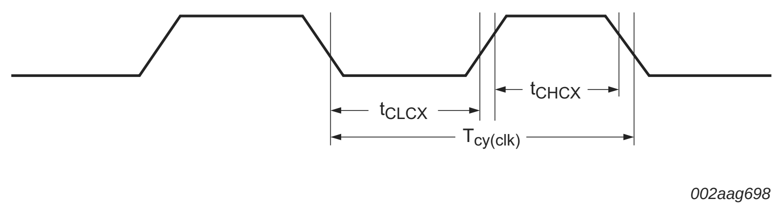



**Fig 26. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

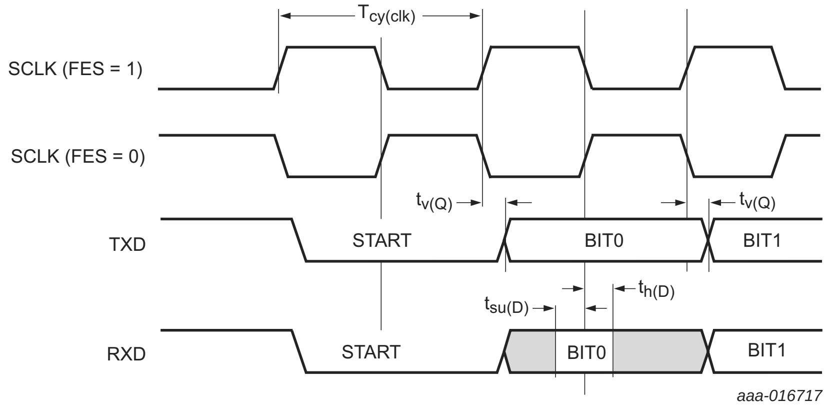



**Fig 30. USART timing**

**Table 27. Dynamic characteristics: SSP pins in SPI mode**
*$T_{amb}$ = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; $C_L$ = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{lag}$ | lag time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | 0.5 x $T_{cy(clk)}$ + 1.5 | - | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | $T_{cy(clk)}$ + 1.5 | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | 0.5 × $T_{cy(clk)}$ + 1.5 | - | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | $T_{cy(clk)}$ + 1.5 | - | - | ns |
| | | synchronous serial frame mode | | $T_{cy(clk)}$ + 1.5 | - | - | ns |
| | | microwire frame format | | 0.5 × $T_{cy(clk)}$ | - | - | ns |
| $t_d$ | delay time | continuous transfer mode<br>SPI mode; CPOL = 0; CPHA = 0 | | - | 0.5 × $T_{cy(clk)}$ | - | ns |
| | | SPI mode; CPOL = 0; CPHA = 1 | | - | n/a | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 0 | | - | 0.5 × $T_{cy(clk)}$ | - | ns |
| | | SPI mode; CPOL = 1; CPHA = 1 | | - | n/a | - | ns |
| | | synchronous serial frame mode | | - | $T_{cy(clk)}$ | - | ns |
| | | microwire frame format | | - | n/a | - | ns |

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / $f_{main}$. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency $f_{main}$, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

## 11.17 External memory interface

**Table 31. Dynamic characteristics: Static asynchronous external memory interface**

*$C_L$ = 22 pF for EMC_Dn $C_L$ = 20 pF for all others; $T_{amb}$ = –40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; values guaranteed by design; the values in the table have been calculated with WAITTURN = 0x0 in STATICWAITTURN register. Timing parameters are given for single memory access cycles. In a normal read operation, the EMC changes the address while CS is asserted which results in multiple memory accesses.*

| Symbol | Parameter[1] | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Read cycle parameters** | | | | | | | |
| $t_{CSLAV}$ | $\overline{\text{CS}}$ LOW to address valid time | | | –3.1 | - | 1.6 | ns |
| $t_{CSLOEL}$ | $\overline{\text{CS}}$ LOW to $\overline{\text{OE}}$ LOW time | | [2] [2] | –0.6 + $T_{cy(clk)}$ × WAITOEN | - | 1.3 + $T_{cy(clk)}$ × WAITOEN | ns |
| $t_{CSLBLSL}$ | $\overline{\text{CS}}$ LOW to $\overline{\text{BLS}}$ LOW time | PB = 1 | | –0.7 | - | 1.8 | ns |
| $t_{OELOEH}$ | $\overline{\text{OE}}$ LOW to $\overline{\text{OE}}$ HIGH time | | [2] | –0.6 + (WAITRD – WAITOEN + 1) × $T_{cy(clk)}$ | - | –0.4 + (WAITRD – WAITOEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{am}$ | memory access time | | | - | - | –16 + (WAITRD – WAITOEN +1) × $T_{cy(clk)}$ | ns |
| $t_{h(D)}$ | data input hold time | | | –16 | - | - | ns |
| $t_{CSHBLSH}$ | $\overline{\text{CS}}$ HIGH to $\overline{\text{BLS}}$ HIGH time | PB = 1 | | –0.4 | - | 1.9 | ns |
| $t_{CSHOEH}$ | CS HIGH to $\overline{\text{OE}}$ HIGH time | | | –0.4 | - | 1.4 | ns |
| $t_{OEHANV}$ | $\overline{\text{OE}}$ HIGH to address invalid | PB = 1 | | –2.0 | - | 2.6 | ns |
| $t_{CSHEOR}$ | $\overline{\text{CS}}$ HIGH to end of read time | | [3] | –2.0 | - | 0 | ns |
| $t_{CSLSOR}$ | $\overline{\text{CS}}$ LOW to start of read time | | [4] | 0 | - | 1.8 | ns |
| **Write cycle parameters** | | | | | | | |
| $t_{CSLAV}$ | $\overline{\text{CS}}$ LOW to address valid time | | | –3.1 | - | 1.6 | ns |
| $t_{CSLDV}$ | $\overline{\text{CS}}$ LOW to data valid time | | | –3.1 | - | 1.5 | ns |
| $t_{CSLWEL}$ | $\overline{\text{CS}}$ LOW to $\overline{\text{WE}}$ LOW time | PB = 1 | | –1.5 + (WAITWEN + 1) × $T_{cy(clk)}$ | - | 0.2 + (WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{CSLBLSL}$ | $\overline{\text{CS}}$ LOW to $\overline{\text{BLS}}$ LOW time | PB = 1 | | –0.7 | - | 1.8 | ns |
| $t_{WELWEH}$ | $\overline{\text{WE}}$ LOW to $\overline{\text{WE}}$ HIGH time | PB = 1 | [2] | –0.6 + (WAITWR – WAITWEN + 1) × $T_{cy(clk)}$ | - | –0.4 + (WAITWR – WAITWEN + 1) × $T_{cy(clk)}$ | ns |
| $t_{WEHDNV}$ | $\overline{\text{WE}}$ HIGH to data invalid time | PB = 1 | [2] | –0.9 + $T_{cy(clk)}$ | - | 2.3 + $T_{cy(clk)}$ | ns |
| $t_{WEHEOW}$ | $\overline{\text{WE}}$ HIGH to end of write time | PB = 1 | [2] [5] | –0.4 + $T_{cy(clk)}$ | - | –0.3 + $T_{cy(clk)}$ | ns |
| $t_{CSLBLSL}$ | $\overline{\text{CS}}$ LOW to $\overline{\text{BLS}}$ LOW | PB = 0 | | –0.7 + (WAITWEN + 1) × $T_{cy(clk)}$ | - | 1.8 + (WAITWEN + 1) × $T_{cy(clk)}$ | ns |

**Table 42. LCD panel connections for STN dual panel mode**

| External pin | 4-bit mono STN dual panel | | 8-bit mono STN dual panel | | Color STN dual panel | |
|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD2 | P4_3 | UD[2] | P4_3 | UD[2] | P4_3 | UD[2] |
| LCD_VD1 | P4_4 | UD[1] | P4_4 | UD[1] | P4_4 | UD[1] |
| LCD_VD0 | P4_1 | UD[0] | P4_1 | UD[0] | P4_1 | UD[0] |
| LCD_LP | P7_6 | LCDLP | P7_6 | LCDLP | P7_6 | LCDLP |
| LCD_ENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM | P4_6 | LCDENAB/ LCDM |
| LCD_FP | P4_5 | LCDFP | P4_5 | LCDFP | P4_5 | LCDFP |
| LCD_DCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK | P4_7 | LCDDCLK |
| LCD_LE | P7_0 | LCDLE | P7_0 | LCDLE | P7_0 | LCDLE |
| LCD_PWR | P7_7 | LCDPWR | P7_7 | LCDPWR | P7_7 | LCDPWR |
| GP_CLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN | PF_4 | LCDCLKIN |

**Table 43. LCD panel connections for TFT panels**

| External pin | TFT 12 bit (4:4:4 mode) | | TFT 16 bit (5:6:5 mode) | | TFT 16 bit (1:5:5:5 mode) | | TFT 24 bit | |
|---|---|---|---|---|---|---|---|---|
| | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function | LPC43xx pin used | LCD function |
| LCD_VD23 | PB_0 | BLUE3 | PB_0 | BLUE4 | PB_0 | BLUE4 | PB_0 | BLUE7 |
| LCD_VD22 | PB_1 | BLUE2 | PB_1 | BLUE3 | PB_1 | BLUE3 | PB_1 | BLUE6 |
| LCD_VD21 | PB_2 | BLUE1 | PB_2 | BLUE2 | PB_2 | BLUE2 | PB_2 | BLUE5 |
| LCD_VD20 | PB_3 | BLUE0 | PB_3 | BLUE1 | PB_3 | BLUE1 | PB_3 | BLUE4 |
| LCD_VD19 | - | - | P7_1 | BLUE0 | P7_1 | BLUE0 | P7_1 | BLUE3 |
| LCD_VD18 | - | - | - | - | P7_2 | intensity | P7_2 | BLUE2 |
| LCD_VD17 | - | - | - | - | - | - | P7_3 | BLUE1 |
| LCD_VD16 | - | - | - | - | - | - | P7_4 | BLUE0 |
| LCD_VD15 | PB_4 | GREEN3 | PB_4 | GREEN5 | PB_4 | GREEN4 | PB_4 | GREEN7 |
| LCD_VD14 | PB_5 | GREEN2 | PB_5 | GREEN4 | PB_5 | GREEN3 | PB_5 | GREEN6 |
| LCD_VD13 | PB_6 | GREEN1 | PB_6 | GREEN3 | PB_6 | GREEN2 | PB_6 | GREEN5 |
| LCD_VD12 | P8_3 | GREEN0 | P8_3 | GREEN2 | P8_3 | GREEN1 | P8_3 | GREEN4 |
| LCD_VD11 | - | - | P4_9 | GREEN1 | P4_9 | GREEN0 | P4_9 | GREEN3 |
| LCD_VD10 | - | - | P4_10 | GREEN0 | P4_10 | intensity | P4_10 | GREEN2 |
| LCD_VD9 | - | - | - | - | - | - | P4_8 | GREEN1 |
| LCD_VD8 | - | - | - | - | - | - | P7_5 | GREEN0 |
| LCD_VD7 | P8_4 | RED3 | P8_4 | RED4 | P8_4 | RED4 | P8_4 | RED7 |
| LCD_VD6 | P8_5 | RED2 | P8_5 | RED3 | P8_5 | RED3 | P8_5 | RED6 |
| LCD_VD5 | P8_6 | RED1 | P8_6 | RED2 | P8_6 | RED2 | P8_6 | RED5 |
| LCD_VD4 | P8_7 | RED0 | P8_7 | RED1 | P8_7 | RED1 | P8_7 | RED4 |
| LCD_VD3 | - | - | P4_2 | RED0 | P4_2 | RED0 | P4_2 | RED3 |
| LCD_VD2 | - | - | - | - | P4_3 | intensity | P4_3 | RED2 |
| LCD_VD1 | - | - | - | - | - | - | P4_4 | RED1 |

On the LPC435x/3x/2x/1x, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 49.

**Remark:** Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

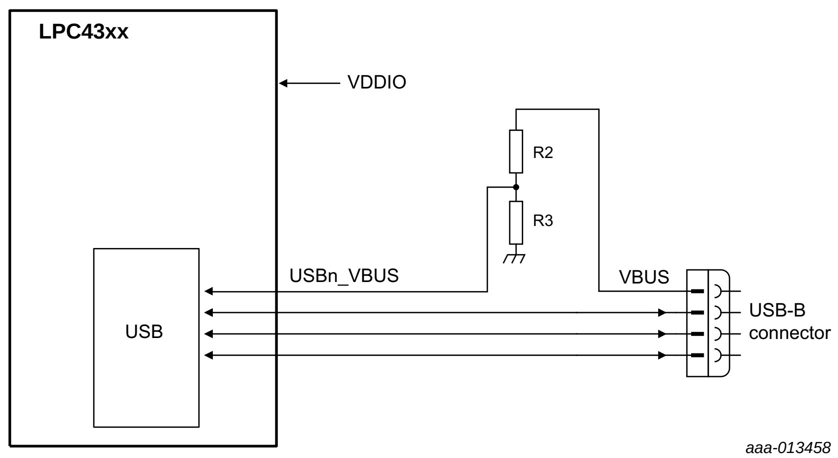



**Fig 48. USB interface on a self-powered device where USBn_VBUS = 5 V**