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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4315jbd144e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4357FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4357JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4357JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4353FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4353JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4353JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4337FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4337JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4337JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4337JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4333FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4333JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4333JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4333JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4327JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4327JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4325JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4325JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4323JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4323JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4322JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4322JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4317JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4317JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4315JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4315JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4313JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4313JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4312JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4312JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P4_0	D5	-	1	1	[2]	N; PU	I/O	**GPIO2[0] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							I	**NMI —** External interrupt input to NMI.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD13 —** LCD data.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							-	**R —** Function reserved.
P4_1	A1	-	3	3	[5]	N; PU	I/O	**GPIO2[1] —** General purpose digital input/output pin.
							O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
							O	**LCD_VD0 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD19 —** LCD data.
							O	**U3_TXD —** Transmitter output for USART3.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							AI	**ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_2	D3	-	12	8	[2]	N; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
							O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
							O	**LCD_VD3 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	-	10	7	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
							O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
							O	**LCD_VD2 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD21 —** LCD data.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							AI	**ADC0_0 —** DAC, ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_7	J13	-	123	85	[2]	N; PU	-	**R —** Function reserved.
							I/O	**EMC_A15 —** External memory address line 15.
							I/O	**SGPIO6 —** General purpose digital input/output pin.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[15] —** General purpose digital input/output pin.
							O	**T2_MAT0 —** Match output 0 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_8	H13	-	125	86	[2]	N; PU	-	**R —** Function reserved.
							I/O	**EMC_A14 —** External memory address line 14.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[16] —** General purpose digital input/output pin.
							O	**T2_MAT1 —** Match output 1 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_9	J15	F8	139	97	[2]	N; PU	I/O	**GPIO3[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_DYCS0}}$ —** SDRAM chip select 0.
							-	**R —** Function reserved.
							O	**T2_MAT2 —** Match output 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_10	H15	-	142	100	[2]	N; PU	I/O	**GPIO3[6] —** General purpose digital input/output pin.
							O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PA_2	K15	-	136	-	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_3	H11	-	147	-	[3]	N; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
							I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_4	G13	-	151	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A23 —** External memory address line 23.
							I/O	**GPIO5[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_0	B15	-	164	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
							O	**LCD_VD23 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[20] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

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Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PC_14	N1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							-	**R —** Function reserved.
							I/O	**GPIO6[13] —** General purpose digital input/output pin.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							I/O	**SD_DAT7 —** SD/MMC data bus line 7.
PD_0	N2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
							O	**EMC_DQMOUT2 —** Data mask 2 used with SDRAM and static devices.
							-	**R —** Function reserved.
							I/O	**GPIO6[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
PD_1	P1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT2 —** SDRAM clock enable 2.
							-	**R —** Function reserved.
							I/O	**GPIO6[15] —** General purpose digital input/output pin.
							O	**SD_POW —** SD/MMC power monitor output.
							-	**R —** Function reserved.
							I/O	**SGPIO5 —** General purpose digital input/output pin.
PD_2	R1	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
							I/O	**EMC_D16 —** External memory data line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[16] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO6 —** General purpose digital input/output pin.

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After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.18.2.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
- Supports DMA access.

7.18.3 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- MultiMedia Cards (MMC version 4.4)

7.18.4 External Memory Controller (EMC)

Remark: The EMC is available on all LPC435x/3x/2x/1x parts. The following memory bus widths are supported:

- LBGA256 packages: 32 bit
- TFBGA100 packages: 16 bit
- LQFP208 packages: 16 bit
- LQFP144 packages: 16 bit

The LPC435x/3x/2x/1x EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

Table 6. EMC pinout for different packages

Function	LBGA256	TFBGA100	LQFP208	LQFP144
A	EMC_A[23:0]	EMC_A[13:0]	EMC_A[23:0]	EMC_A[15:0]
D	EMC_D[31:0]	EMC_D[7:0]	EMC_D[15:0]	EMC_D[15:0]
$\overline{\text{BLS}}$	$\overline{\text{EMC\_BLS[3:0]}}$	$\overline{\text{EMC\_BLS0}}$	$\overline{\text{EMC\_BLS[1:0]}}$	$\overline{\text{EMC\_BLS[1:0]}}$
$\overline{\text{CS}}$	$\overline{\text{EMC\_CS[3:0]}}$	$\overline{\text{EMC\_CS0}}$	$\overline{\text{EMC\_CS[3:0]}}$	$\overline{\text{EMC\_CS[1:0]}}$

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7.23.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.23.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC435x/3x/2x/1x.

7.23.9 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC435x/3x/2x/1x support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
   a. Deep-sleep mode
   b. Power-down mode
   c. Deep power-down mode

Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

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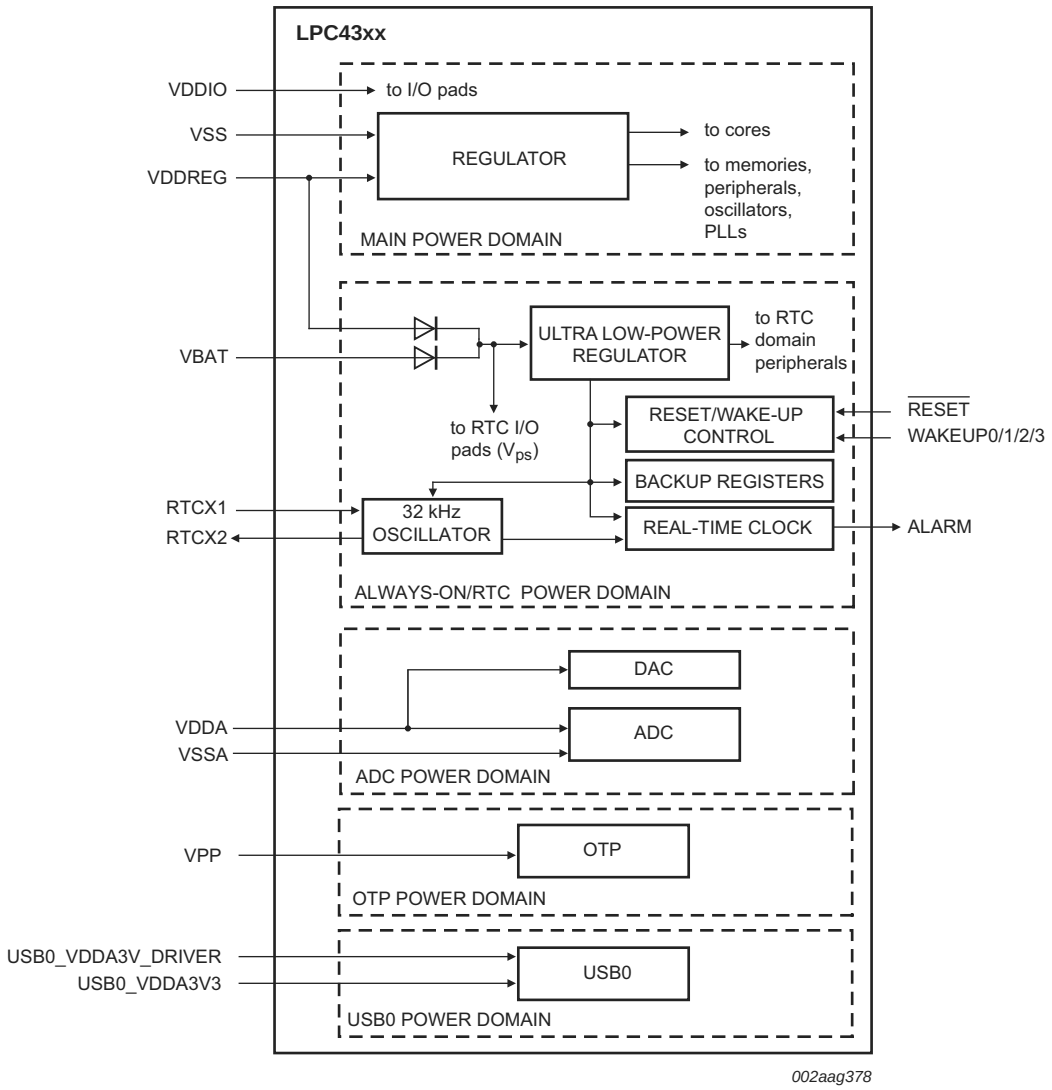

Fig 9. Power domains

7.23.11 Code security (Code Read Protection - CRP)

CRP enables different levels of security so that access to the on-chip flash and use of the JTAG and ISP can be restricted. CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by CRP.

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8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)	on pin VDDREG		−0.5	3.6	V
$V_{DD(IO)}$	input/output supply voltage	on pin VDDIO		−0.5	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		−0.5	3.6	V
V_{BAT}	battery supply voltage	on pin VBAT		−0.5	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP		−0.5	3.6	V
V_I	input voltage	when $V_{DD(IO)} \geq 2.4$ V 5 V tolerant digital I/O pins	[2]	−0.5	5.5	V
		ADC/DAC pins and digital I/O pins configured for an analog function		−0.5	$V_{DDA(3V3)}$	V
		USB0 pins USB0_DP; USB0_DM;USB0_VBUS		−0.3	5.25	V
		USB0 pins USB0_ID; USB0_RREF		−0.3	3.6	V
		USB1 pins USB1_DP and USB1_DM		−0.3	5.25	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature		[3]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	-	2000	V

[1] The following applies to the limiting values:

a) Absolute maximum ratings state the extreme limits that the product can withstand without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device. Conditions for functional operation of the part are shown in Table 11 "Static characteristics".

b) This product includes circuitry designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Dependent on package type.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −6 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−6	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		6	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86.5	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76.5	mA
I_{pd}	pull-down current	V_I = 5 V	[13] [14] [15]	-	93	-	μA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	μA
R_S	series resistance	on I/O pins with analog function; analog function enabled			200		Ω
I/O pins - high drive strength							
C_I	input capacitance			-	-	5.2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.4$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V

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Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76	mA
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[13] [14] [15]	-	62	-	μA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	0	-	μA
Open-drain I^2C0-bus pins							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			−0.5	0.14	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[12]	-	4.5	-	μA
		V_I = 5 V		-	-	10	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	-	1.2	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	-	1.2	V
C_{io}	input/output capacitance		[16]	-	-	0.8	pF
USB0 pins[17]							
V_I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		$V_{DD(IO)} \geq 2.4$ V		0	-	5.25	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
R_{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ

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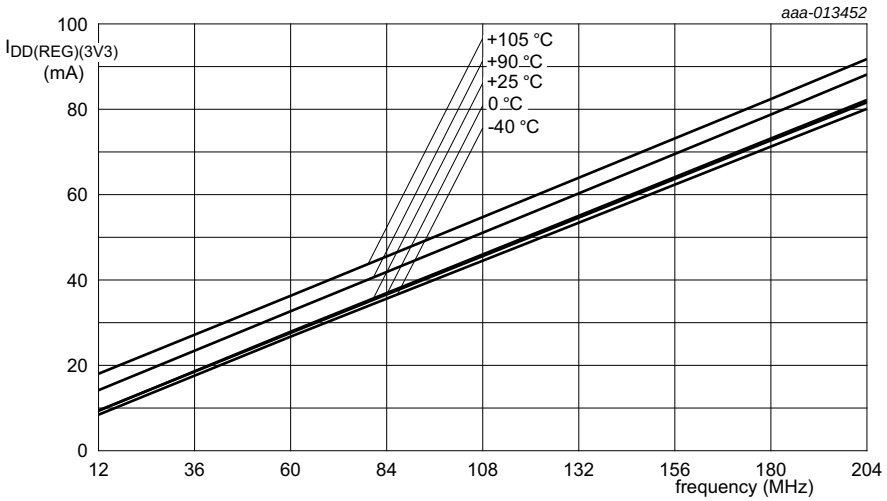
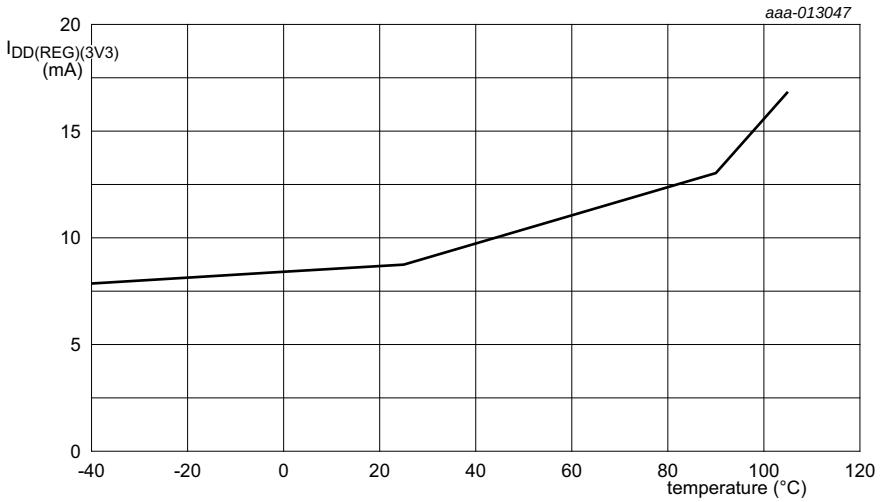


Conditions: active mode entered executing code while (1){} from SRAM; M0 core in reset; $V_{DD(REG)(3V3)}$ = 3.3 V; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 13. Typical supply current versus core frequency in active mode; code executed from SRAM



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; internal pull-up resistors disabled; M0 core in reset; system PLL disabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled. CCLK = 12 MHz.

Fig 14. Typical supply current versus temperature in sleep mode

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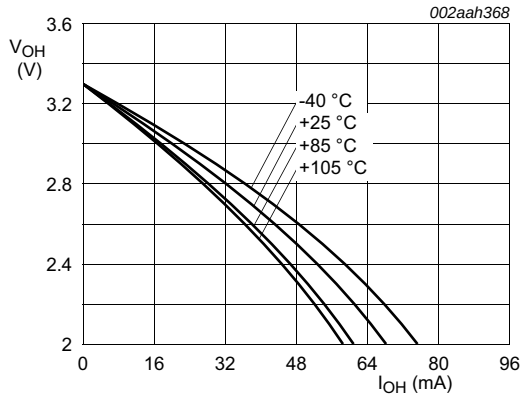
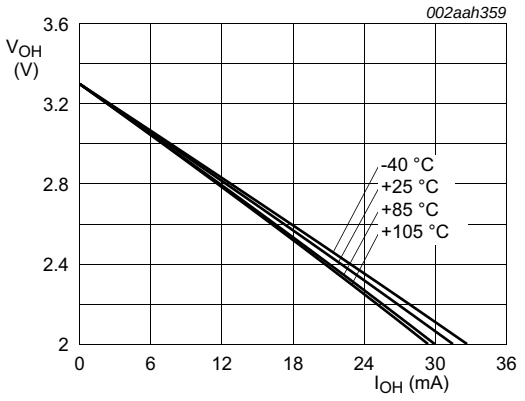
10.3 Electrical pin characteristics



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 20. Standard I/O pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V.

Fig 21. Standard I/O pins; typical HIGH level output voltage V_{OH} versus HIGH level output current I_{OH}

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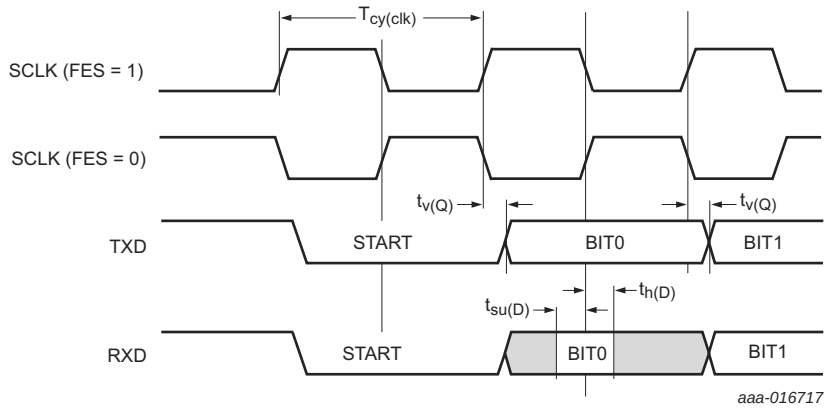

Fig 30. USART timing

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Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	$0.5 \times T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns
SSP slave							
PCLK	Peripheral clock frequency			-	-	204	MHz
$T_{cy(clk)}$	clock cycle time		[2]	$1/(11 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		1.5	-	-	ns
t_{DH}	data hold time	in SPI mode		2	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	[4 × (1/PCLK)] + 1	ns
$t_{h(Q)}$	data output hold time	in SPI mode		4.5	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$	-	-	ns
		microwire frame format		$T_{cy(clk)}$	-	-	ns

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Table 30. Dynamic characteristics: SGPIO

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D)}$	data input set-up time			2	-	-	ns
$t_{h(D)}$	data input hold time		[1]	T_{SGPIO} + 2	-	-	ns
$t_{su(D)}$	data input set-up time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{h(D)}$	data input hold time	sampled by SGPIO_CLOCK	[1]	T_{SGPIO} + 2	-	-	ns
$t_{v(Q)}$	data output valid time		[1]	-	-	2 × T_{SGPIO}	ns
$t_{h(Q)}$	data output hold time		[1]	T_{SGPIO}	-		ns
$t_{v(Q)}$	data output valid time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns
$t_{h(Q)}$	data output hold time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns

[1] SGPIO_CLOCK is the internally generated SGPIO clock. $T_{SGPIO} = 1/f_{SGPIO\_CLOCK}$.

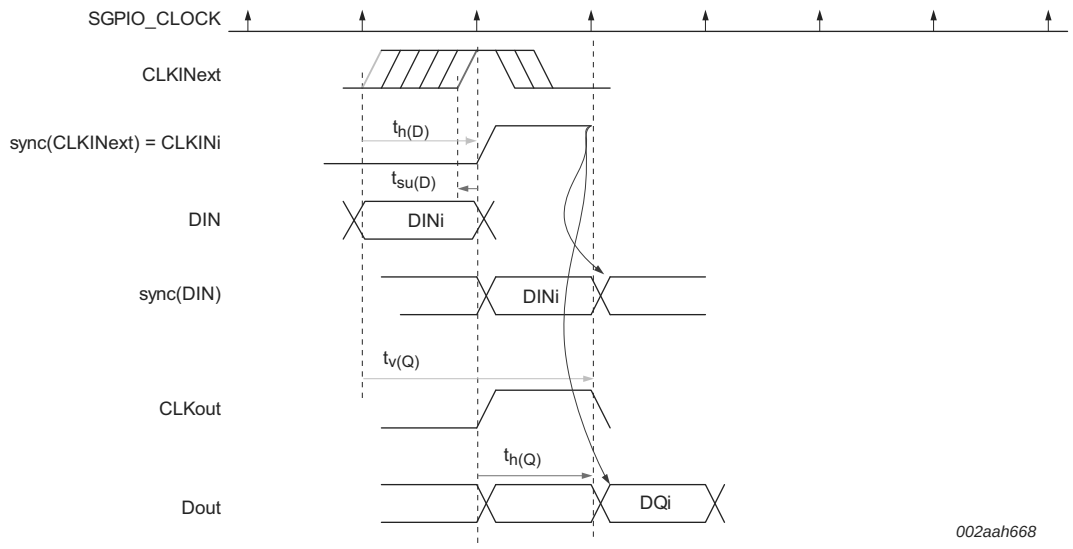

Fig 34. SGPIO timing

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Table 32. Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for $\overline{EMC\_DYCSn}$, $\overline{EMC\_RAS}$, $\overline{EMC\_CAS}$, $\overline{EMC\_WE}$, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ = 3.3 V ± 10 %; RD = 1 (see LPC43xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	dynamic chip select valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DYCS)}$	dynamic chip select hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	4.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	0.5 + 0.5 × $T_{cy(clk)}$	1.1 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	2.9 + 0.5 × $T_{cy(clk)}$	4.6 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	write enable valid delay time	-	3.2 + 0.5 × $T_{cy(clk)}$	5.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(WE)}$	write enable hold time	1.3 + 0.5 × $T_{cy(clk)}$	1.4 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	DQMOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.0 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	DQMOUT hold time	0.2 + 0.5 × $T_{cy(clk)}$	0.8 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.3 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	CKEOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	CKEOUT hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	2.2	0.8	-	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.2 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns

Table 33. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 105 °C; $V_{DD(IO)}$ = 3.3 V ± 10 %; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	delay value	[1]				
		CLKn_DELAY = 0		0.0	0.0	0.0	ns
		CLKn_DELAY = 1	[1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2	[1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3	[1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4	[1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5	[1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6	[1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7	[1]	2.5	3.6	5.8	ns

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC43xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.

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Table 35. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.19 Ethernet

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

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Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC4357_53_37_33 v.2	20120711	Preliminary data sheet	-	LPC4357_53 v.1
Modifications:	• Data sheet status changed to preliminary. • Parts LPC4337 and LPC4333 added. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”, “USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Section 10.2 added. • Table 8 “Thermal resistance (LQFP packages)” and Table 9 “Thermal resistance value (BGA packages)” added. • AES removed. Available on parts LPC43Sxx only. • Dynamic characteristics of the SD/MMC controller updated in Table 30. • Dynamic characteristics of the LCD controller updated in Table 31. • Dynamic characteristics of the SSP controller updated in Table 23. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 10.			
LPC4357_53 v.1	20120604	Objective data sheet	-	-

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19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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