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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, WDT
Number of I/O	49
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4315jet100e

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4357FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4357JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4357JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4353FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4353JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4353JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4337FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4337JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4337JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4337JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4333FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4333JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4333JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4333JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4327JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4327JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4325JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4325JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4323JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4323JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4322JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4322JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4317JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4317JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4315JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4315JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4313JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4313JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4312JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4312JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	Motor control PWM	QEI	ADC channels	Temperature range ^[1]	GPIO
LPC4357FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC4357JET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC4357JBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC4353FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC4353JET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC4353JBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC4337FET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC4337JET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC4337JBD144	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC4337JET100	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC4333FET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC4333JET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC4333JBD144	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC4333JET100	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC4327JBD144	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4327JET100	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC4325JBD144	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4325JET100	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC4323JBD144	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4323JET100	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC4322JBD144	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4322JET100	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC4317JBD144	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC4317JET100	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC4315JBD144	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC4315JET100	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC4313JBD144	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC4313JET100	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	no	no	4	J	49
LPC4312JBD144	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC4312JET100	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	no	no	4	J	49

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_3	P15	-	113	79	[2]	N; PU	I/O	GPIO3[2] — General purpose digital input/output pin.
							O	USB0_PPWR — VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	SGPIO4 — General purpose digital input/output pin.
							O	EMC_CS1 — LOW active Chip Select 1 signal.
							-	R — Function reserved.
							I	T2_CAP2 — Capture input 2 of timer 2.
							-	R — Function reserved.
							-	R — Function reserved.
P6_4	R16	F6	114	80	[2]	N; PU	I/O	GPIO3[3] — General purpose digital input/output pin.
							I	CTIN_6 — SCT input 6. Capture input 1 of timer 3.
							O	U0_TXD — Transmitter output for USART0.
							O	EMC_CAS — LOW active SDRAM Column Address Strobe.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P6_5	P16	F9	117	82	[2]	N; PU	I/O	GPIO3[4] — General purpose digital input/output pin.
							O	CTOUT_6 — SCT output 6. Match output 2 of timer 1.
							I	U0_RXD — Receiver input for USART0.
							O	EMC_RAS — LOW active SDRAM Row Address Strobe.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P6_6	L14	-	119	83	[2]	N; PU	I/O	GPIO0[5] — General purpose digital input/output pin.
							O	EMC_BLS1 — LOW active Byte Lane select signal 1.
							I/O	SGPIO5 — General purpose digital input/output pin.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	R — Function reserved.
							I	T2_CAP3 — Capture input 3 of timer 2.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PC_2	F6	-	13	-	[2]	N; PU	I/O	USB1_ULPI_D6 — ULPI link bidirectional data line 6.
							-	R — Function reserved.
							I	U1_CTS — Clear to Send input for UART 1.
							O	ENET_TXD2 — Ethernet transmit data 2 (MII interface).
							I/O	GPIO6[1] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							O	SD_RST — SD/MMC reset signal for MMC4.4 card.
PC_3	F5	-	11	-	[5]	N; PU	I/O	USB1_ULPI_D5 — ULPI link bidirectional data line 5.
							-	R — Function reserved.
							O	U1_RTS — Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							O	ENET_TXD3 — Ethernet transmit data 3 (MII interface).
							I/O	GPIO6[2] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
							O	SD_VOLT1 — SD/MMC bus voltage select output 1.
PC_4	F4	-	16	-	[2]	N; PU	AI	ADC1_0 — DAC, ADC1 and ADC0, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							-	R — Function reserved.
							I/O	USB1_ULPI_D4 — ULPI link bidirectional data line 4.
							-	R — Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	GPIO6[3] — General purpose digital input/output pin.
							-	R — Function reserved.
							I	T3_CAP1 — Capture input 1 of timer 3.
PC_5	G4	-	20	-	[2]	N; PU	I/O	SD_DAT0 — SD/MMC data bus line 0.
							-	R — Function reserved.
							I/O	USB1_ULPI_D3 — ULPI link bidirectional data line 3.
							-	R — Function reserved.
							O	ENET_TX_ER — Ethernet Transmit Error (MII interface).
							I/O	GPIO6[4] — General purpose digital input/output pin.
							-	R — Function reserved.
							I	T3_CAP2 — Capture input 2 of timer 3.
PC_5	G4	-	20	-	[2]	N; PU	I/O	SD_DAT1 — SD/MMC data bus line 1.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PC_10	M5	-	-	-	[2]	N; PU	-	R — Function reserved.
							O	USB1_ULPI_STP — ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
							I	U1_DSR — Data Set Ready input for UART 1.
							-	R — Function reserved.
							I/O	GPIO6[9] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT3 — Match output 3 of timer 3.
							I/O	SD_CMD — SD/MMC command signal.
PC_11	L5	-	-	-	[2]	N; PU	-	R — Function reserved.
							I	USB1_ULPI_DIR — ULPI link DIR signal. Controls the ULPI data line direction.
							I	U1_DCD — Data Carrier Detect input for UART 1.
							-	R — Function reserved.
							I/O	GPIO6[10] — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
PC_12	L6	-	-	-	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							O	U1_DTR — Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							-	R — Function reserved.
							I/O	GPIO6[11] — General purpose digital input/output pin.
							I/O	SGPIO11 — General purpose digital input/output pin.
							I/O	I2S0_TX_SDA — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I ² S-bus specification.
							I/O	SD_DAT5 — SD/MMC data bus line 5.
PC_13	M1	-	-	-	[2]	N; PU	-	R — Function reserved.
							-	R — Function reserved.
							O	U1_TXD — Transmitter output for UART 1.
							-	R — Function reserved.
							I/O	GPIO6[12] — General purpose digital input/output pin.
							I/O	SGPIO12 — General purpose digital input/output pin.
							I/O	I2S0_TX_WS — Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the I ² S-bus specification.
							I/O	SD_DAT6 — SD/MMC data bus line 6.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
WAKEUP0	A9	A4	187	130	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 0 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP1	A10	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 1 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP2	C9	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 2 of the event monitor. This pin does not have an internal pull-up.
WAKEUP3	D8	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. This pin does not have an internal pull-up.
ADC pins								
ADC0_0/ ADC1_0/DAC	E3	A2	8	6	[8]	I; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	A1	4	2	[8]	I; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	206	143	[8]	I; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	A3	200	139	[8]	I; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	-	199	138	[8]	I; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	-	208	144	[8]	I; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	-	204	142	[8]	I; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	-	197	136	[8]	I; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC								
RTC_ALARM	A11	C3	186	129	[11]	-	O	RTC controlled output.
RTCX1	A8	A5	182	125	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B5	183	126	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
SAMPLE	B9	-	-	-	[11]	O	O	Event monitor sample output.
Crystal oscillator pins								

The LCD controller provides all of the necessary control signals to interface directly to various color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024×768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512 byte color palette allows reducing bus utilization (that is, memory size of the displayed data) while still supporting many colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time required to operate the display.

7.18.7.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320×200 , 320×240 , 640×200 , 640×240 , 640×480 , 800×600 , and 1024×768 .
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128×32 -bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.18.8 Ethernet

Remark: The ethernet controller is available on parts LPC435x and LPC433x. Ethernet is not available on parts LPC432x and LPC431x.

7.18.8.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection

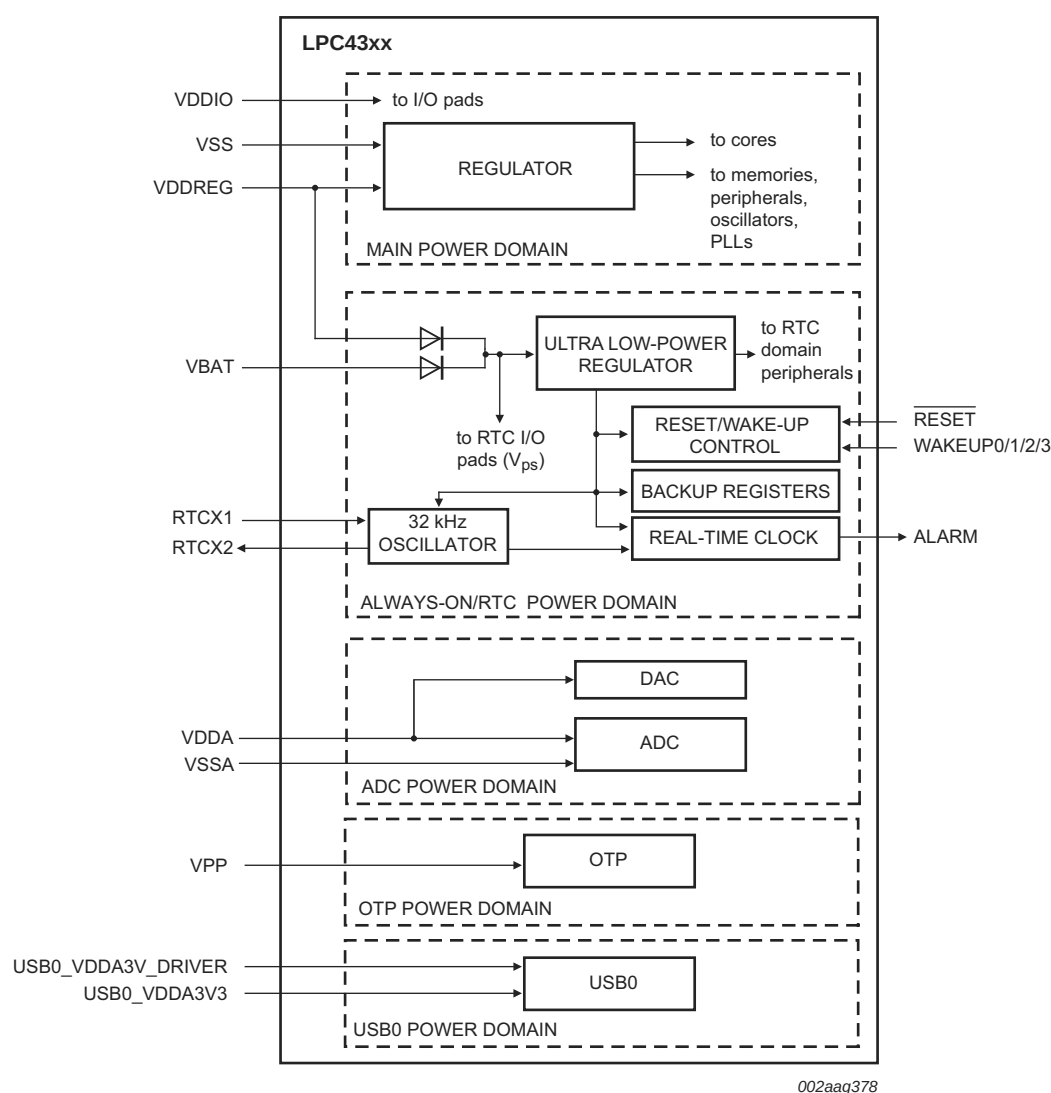


Fig 9. Power domains

7.23.11 Code security (Code Read Protection - CRP)

CRP enables different levels of security so that access to the on-chip flash and use of the JTAG and ISP can be restricted. CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by CRP.

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.
- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0. See [Table 5](#).

CAUTION



If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.24 Serial Wire Debug/JTAG

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

Remark: Serial Wire Debug is supported for the ARM Cortex-M4 only,

The ARM Cortex-M0 coprocessor supports JTAG debug. A standard ARM Cortex-compliant debugger can debug the ARM Cortex-M4 and the ARM Cortex-M0 cores separately or both cores simultaneously.

Remark: In order to debug the ARM Cortex-M0, release the M0 reset by software in the RGU block.

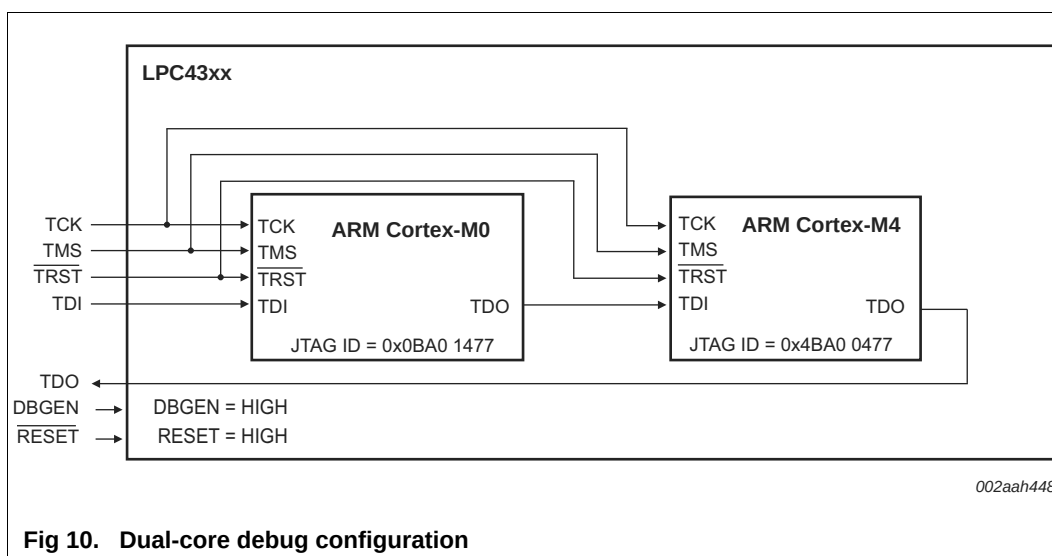
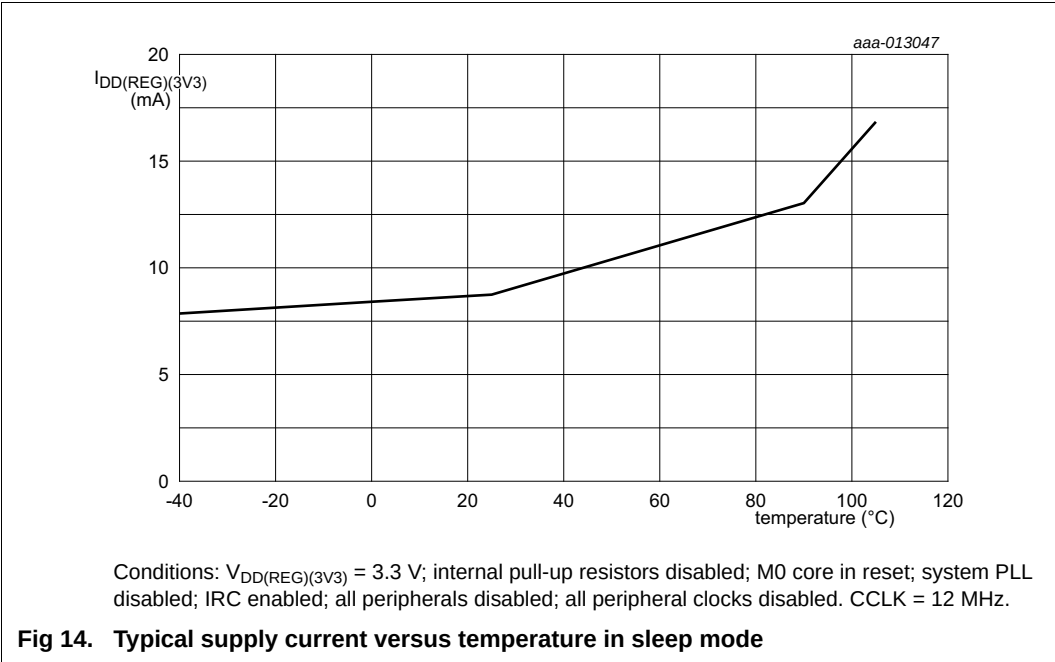
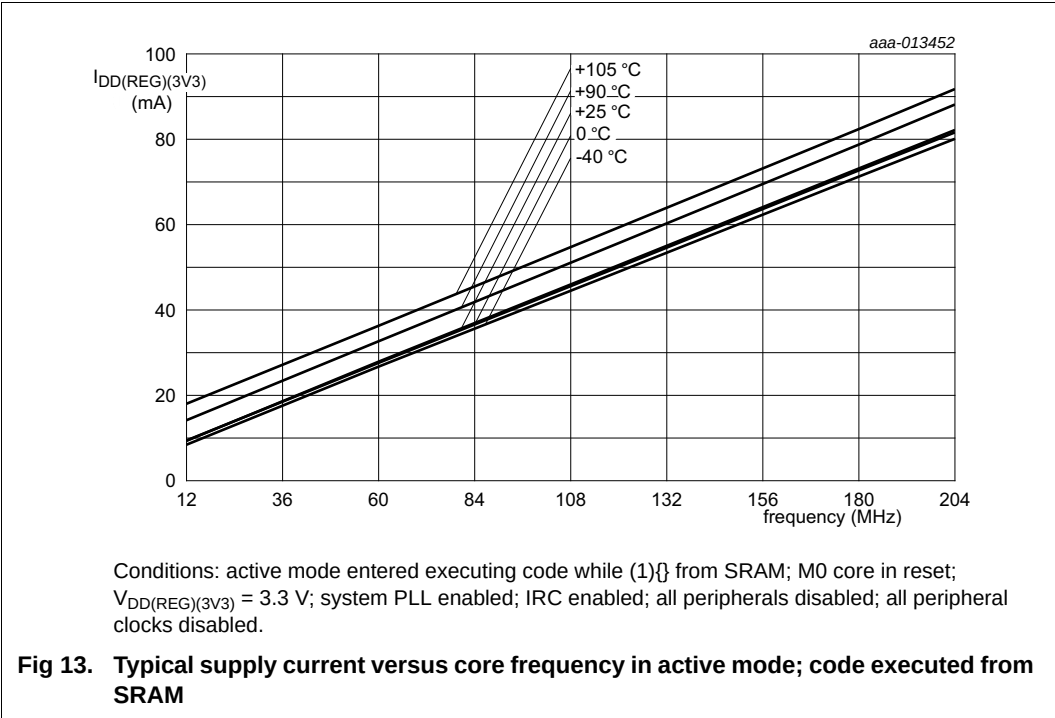
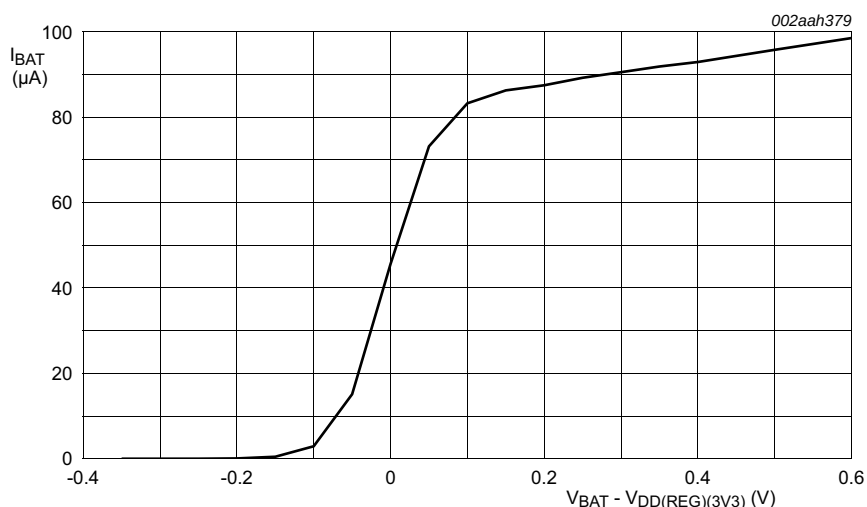


Fig 10. Dual-core debug configuration

Table 11. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
V _{OH}	HIGH-level output voltage	I _{OH} = −8 mA		V _{DD(I/O)} − 0.4	-	-	V
V _{OL}	LOW-level output voltage	I _{OL} = 8 mA		-	-	0.4	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD(I/O)} − 0.4 V		−8	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V		8	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86	mA
I _{OLS}	LOW-level short-circuit output current	drive LOW; connected to V _{DD(I/O)}	[11]	-	-	76	mA
I _{pd}	pull-down current	V _I = V _{DD(I/O)}	[13] [14] [15]	-	62	-	μA
I _{pu}	pull-up current	V _I = 0 V	[13] [14] [15]	-	−62	-	μA
		V _{DD(I/O)} < V _I ≤ 5 V		-	0	-	μA
Open-drain I ² C0-bus pins							
V _{IH}	HIGH-level input voltage			0.7 × V _{DD(I/O)}	-	-	V
V _{IL}	LOW-level input voltage			−0.5	0.14	0.3 × V _{DD(I/O)}	V
V _{hys}	hysteresis voltage			0.1 × V _{DD(I/O)}	-	-	V
V _{OL}	LOW-level output voltage	I _{OLS} = 3 mA		-	-	0.4	V
I _{LI}	input leakage current	V _I = V _{DD(I/O)}	[12]	-	4.5	-	μA
		V _I = 5 V		-	-	10	μA
Oscillator pins							
V _{i(XTAL1)}	input voltage on pin XTAL1			−0.5	-	1.2	V
V _{o(XTAL2)}	output voltage on pin XTAL2			−0.5	-	1.2	V
C _{io}	input/output capacitance		[16]	-	-	0.8	pF
USB0 pins ^[17]							
V _I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		V _{DD(I/O)} ≥ 2.4 V		0	-	5.25	V
		V _{DD(I/O)} = 0 V		0	-	3.6	V
R _{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ





Conditions: $V_{DD(REG)(3V3)} = 3.0$ V; $V_{BAT} = 2.6$ V to 3.6 V; CCLK = 12 MHz.

Remark: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V.

Fig 19. Typical battery supply current in Active mode

10.2 Peripheral power consumption

The typical power consumption at $T = 25$ °C for each individual peripheral is measured as follows:

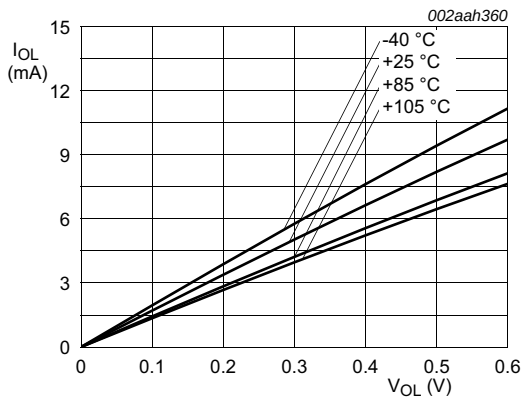
1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

Table 12. Peripheral power consumption

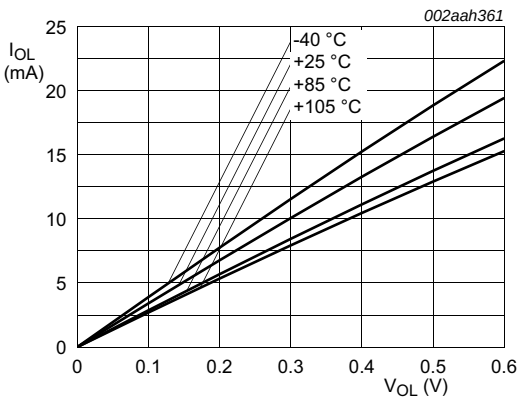
Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
M0 core	CLK_M4_M0APP	3.3	6.6
I2C1	CLK_APB3_I2C1	0.01	0.01
I2C0	CLK_APB1_I2C0	< 0.01	0.02
DAC	CLK_APB3_DAC	0.01	0.02
ADC0	CLK_APB3_ADC0	0.07	0.07
ADC1	CLK_APB3_ADC1	0.07	0.07
CAN0	CLK_APB3_CAN0	0.17	0.17
CAN1	CLK_APB1_CAN1	0.16	0.15
MOTOCON	CLK_APB1_MOTOCON	0.04	0.04
I2S	CLK_APB1_I2S	0.09	0.08
SPIFI	CLK_SPIFI, CLK_M4_SPIFI	1.14	2.29

Table 12. Peripheral power consumption

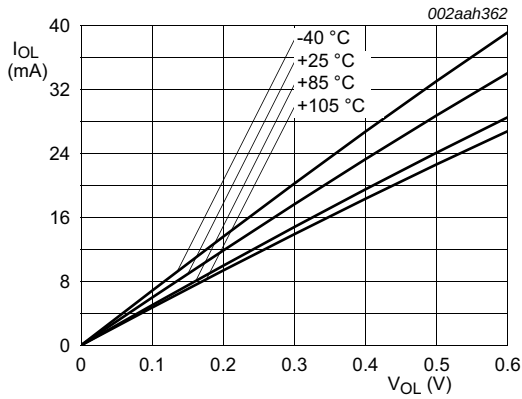
Peripheral	Branch clock	I _{DD(REG)(3V3)} in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
GPIO	CLK_M4_GPIO	0.72	1.43
LCD	CLK_M4_LCD	0.91	1.82
ETHERNET	CLK_M4_ETHERNET	1.06	2.15
UART0	CLK_M4_UART0, CLK_APB0_UART0	0.24	0.43
UART1	CLK_M4_UART1, CLK_APB0_UART1	0.24	0.43
UART2	CLK_M4_UART2, CLK_APB2_UART2	0.26	0.5
UART3	CLK_M4_USART3, CLK_APB2_UART3	0.27	0.45
TIMER0	CLK_M4_TIMER0	0.08	0.15
TIMER1	CLK_M4_TIMER1	0.09	0.15
TIMER2	CLK_M4_TIMER2	0.1	0.19
TIMER3	CLK_M4_TIMER3	0.08	0.16
SDIO	CLK_M4_SDIO, CLK_SDIO	0.66	1.17
SCTimer/PWM	CLK_M4_SCT	0.66	1.3
SSP0	CLK_M4_SSP0, CLK_APB0_SSP0	0.13	0.23
SSP1	CLK_M4_SSP1, CLK_APB2_SSP1	0.14	0.27
DMA	CLK_M4_DMA	1.81	3.61
WWDT	CLK_M4_WWDT	0.03	0.09
QEI	CLK_M4_QEI	0.28	0.55
USB0	CLK_M4_USB0, CLK_USB0	1.9	3.9
USB1	CLK_M4_USB1, CLK_USB1	3.02	5.69
RITIMER	CLK_M4_RITIMER	0.05	0.1
EMC	CLK_M4 EMC, CLK_M4 EMC_DIV	3.94	7.95
SCU	CLK_M4_SCU	0.1	0.21
CREG	CLK_M4_CREG	0.35	0.7
Flash bank A	CLK_M4_FLASHA	1.47	2.97
Flash bank B	CLK_M4_FLASHB	1.4	2.84
SGPIO	CLK_PERIPH_SGPIO	0.1	0.17
SPI	CLK_SPI	0.07	0.11



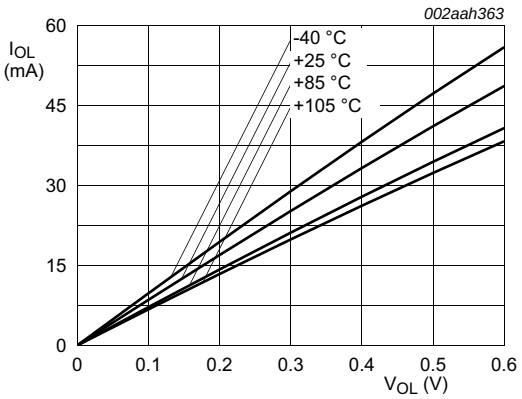
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3\text{ V}$; ultra high-drive; EHD = 0x3.

Fig 22. High-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}

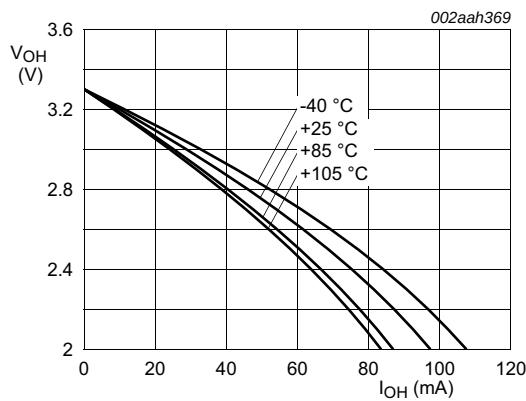
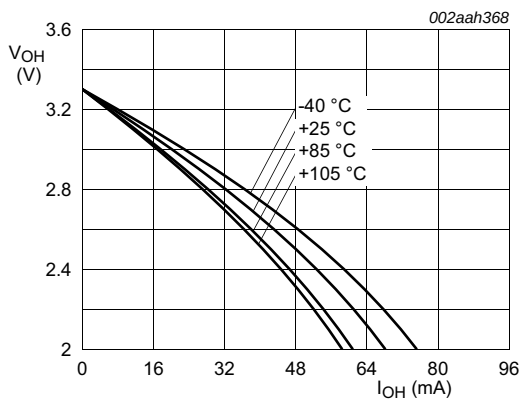
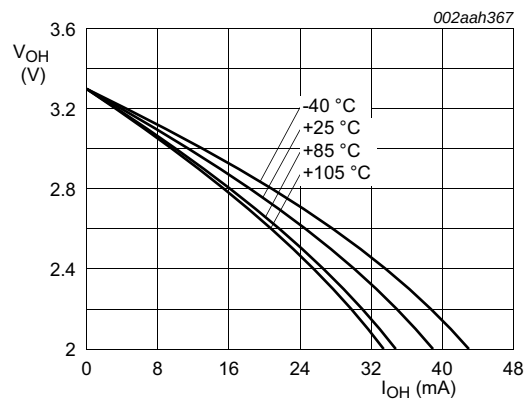
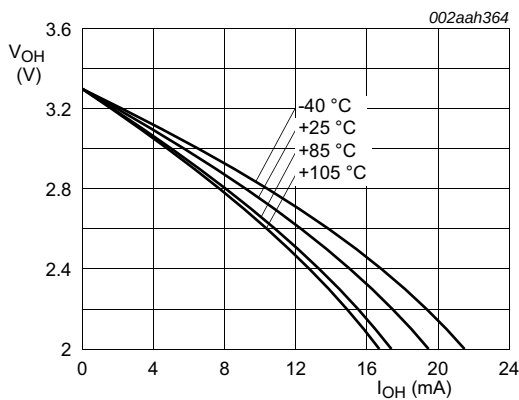


Fig 23. High-drive pins; typical HIGH level output voltage V_{OH} versus HIGH level output current I_{OH}

Table 36. Dynamic characteristics: Ethernet

$T_{amb} = -40\text{ }^{\circ}\text{C to }105\text{ }^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$; $2.7\text{ V} \leq V_{DD(IO)} \leq 3.6\text{ V}$. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load $\geq 25\text{ pF}$ accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

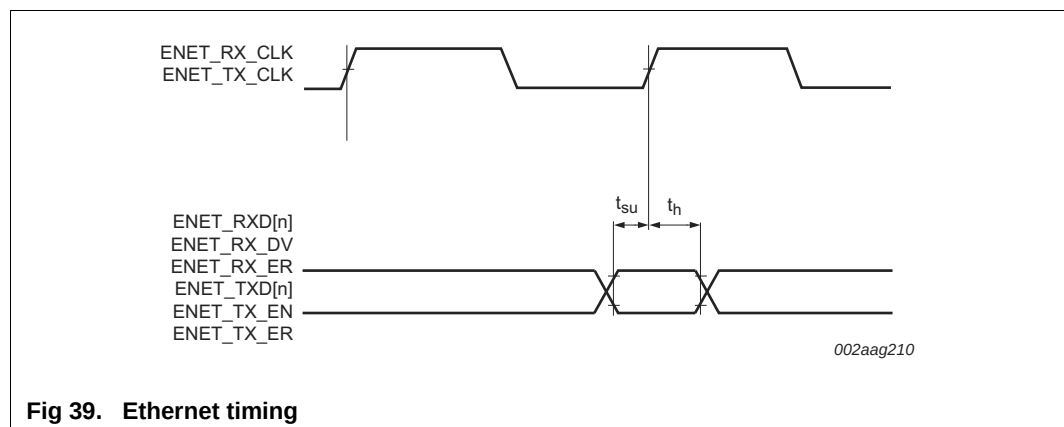
**Fig 39. Ethernet timing**

Table 42. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 43. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4	PB_0	BLUE7
LCD_VD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3	PB_1	BLUE6
LCD_VD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2	PB_2	BLUE5
LCD_VD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1	PB_3	BLUE4
LCD_VD19	-	-	P7_1	BLUE0	P7_1	BLUE0	P7_1	BLUE3
LCD_VD18	-	-	-	-	P7_2	intensity	P7_2	BLUE2
LCD_VD17	-	-	-	-	-	-	P7_3	BLUE1
LCD_VD16	-	-	-	-	-	-	P7_4	BLUE0
LCD_VD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCD_VD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCD_VD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCD_VD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCD_VD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCD_VD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCD_VD9	-	-	-	-	-	-	P4_8	GREEN1
LCD_VD8	-	-	-	-	-	-	P7_5	GREEN0
LCD_VD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCD_VD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCD_VD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCD_VD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4
LCD_VD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCD_VD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCD_VD1	-	-	-	-	-	-	P4_4	RED1

On the LPC435x/3x/2x/1x, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

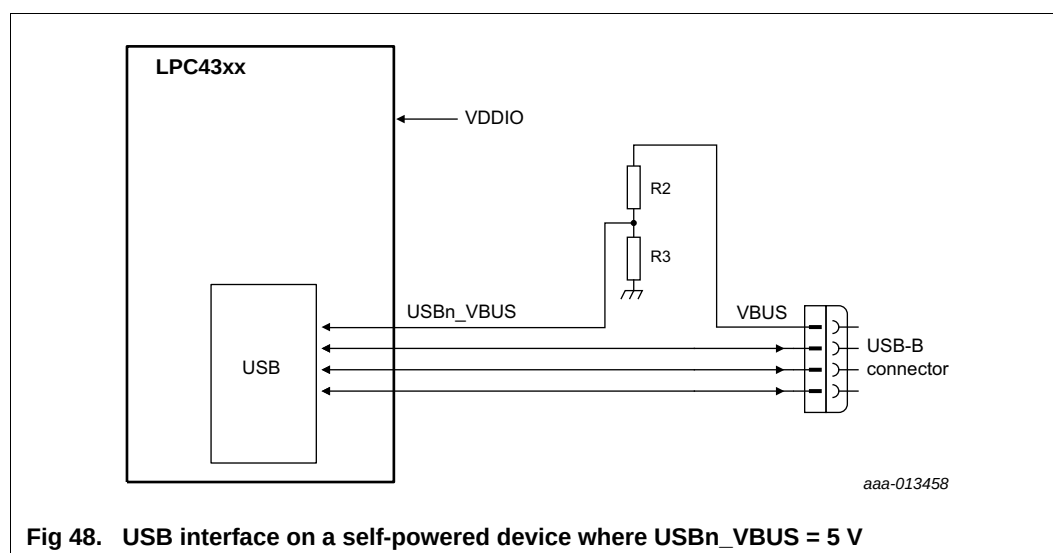
$$VBUS_{\max} = 5.25 \text{ V}$$

$$VDDIO = 3.6 \text{ V},$$

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See [Figure 49](#).

Remark: Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.



14. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm

SOT740-2

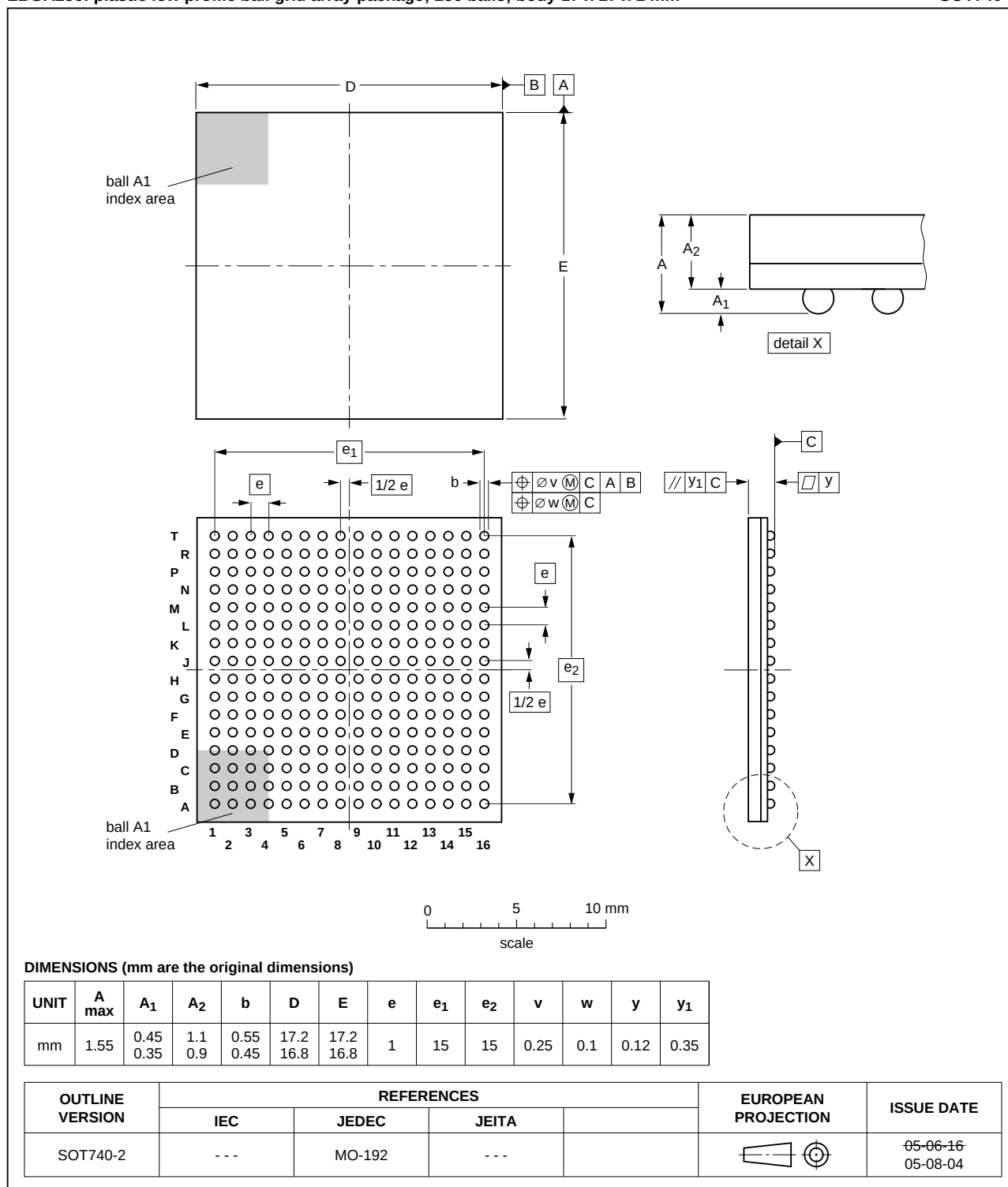


Fig 51. Package outline LBGA256 package

Table 47. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	- SD/MMC timing data updated. See Table 35 "Dynamic characteristics: SD/MMC". - IEEE standard 802.3 compliance added to Section 11.18. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals. - SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 "SSP in SPI mode and SPI master timing". - Parameters t_{lead}, t_{lag}, and t_d added in Table 25 "Dynamic characteristics: SSP pins in SPI mode". - Parameter t_{CSLWEL} with condition $PB = 1$ corrected: $(WAITWEN + 1) \times T_{cy(clk)}$ added. See Table 29 "Dynamic characteristics: Static asynchronous external memory interface". - Parameter t_{CSLBSL} with condition $PB = 0$ corrected: $(WAITWEN + 1) \times T_{cy(clk)}$ added. See Table 29 "Dynamic characteristics: Static asynchronous external memory interface". - Removed restriction on C_CAN bus usage. See CAN.1 errata in Ref. 2. - General-purpose OTP size corrected.			
LPC435X_3X_2X_1X v.3	20121206	Preliminary data sheet	-	LPC4357_53_37_33 v.2.1
Modifications:	- TFBGA180 packages removed. - Part LPC432x and LPC431x added. - SCT dither engine added and SCT bi-directional event enable features added. - Figure 10 "Dual-core debug configuration" added. $T = 105\text{ }^{\circ}\text{C}$ data added in Figure 20 to Figure 23. - Change symbol names and parameter names in Table 21. - Parameter I_{LH} updated for condition $V_I = 5\text{ V}$ and $T_{amb} = 25\text{ }^{\circ}\text{C}/105\text{ }^{\circ}\text{C}$ in Table 11. - Power consumption data added in Section 10.1. - SPIFI dynamic characteristics added in Section 11.16. - IRC accuracy corrected to $\pm 2\%$ for $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $0\text{ }^{\circ}\text{C}$ and $T_{amb} = 85\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$. - Pull-up and Pull-down current data (Figure 24 and Figure 25) updated with data for $T_{amb} = 105\text{ }^{\circ}\text{C}$. - SPIFI maximum data rate changed to 52 MB per second. - Recommendation for V_{BAT} use added: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2\text{ V}$. - Table 14 "Band gap characteristics" added. - Section 7.23.9 "Power Management Controller (PMC)" added. - Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. - OTP memory size changed to 64 bit. - Use of C_CAN peripheral restricted in Section 2. - ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.			
LPC4357_53_37_33 v.2.1	20120904	Preliminary data sheet	-	LPC4357_53_37_33 v.2
Modifications:	- SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. - SWD removed for ARM Cortex-M0. - BOD de-assertion levels added in Table 13. - Peripheral power consumption data added in Table 12. - Minimum value for all supply voltages changed to -0.5 V in Table 7.			