Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4317jbd144e

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_20	M10	K10	100	70	[2]	N; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							I	**T0_CAP2 —** Capture input 2 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							I/O	**EMC_D11 —** External memory data line 11.
P2_0	T16	G10	108	75	[2]	N; PU	I/O	**SGPIO4 —** General purpose digital input/output pin.
							O	**U0_TXD —** Transmitter output for USART0. See Table 4 for ISP mode.
							I/O	**EMC_A13 —** External memory address line 13.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	**GPIO5[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
P2_1	N15	G7	116	81	[2]	N; PU	I/O	**SGPIO5 —** General purpose digital input/output pin.
							I	**U0_RXD —** Receiver input for USART0. See Table 4 for ISP mode.
							I/O	**EMC_A12 —** External memory address line 12.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**GPIO5[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P3_5	C12	B7	173	121	[2]	N; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**LCD_VD12 —** LCD data.
P3_6	B13	C7	174	122	[2]	N; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
							I/O	**SPI_MISO —** Master In Slave Out for SPI.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_7	C11	D7	176	123	[2]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_MOSI —** Master Out Slave In for SPI.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							I/O	**SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0.
							I/O	**GPIO5[10] —** General purpose digital input/output pin.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_8	C10	E7	179	124	[2]	N; PU	-	**R —** Function reserved.
							I	**SPI_SSEL —** Slave Select for SPI. Note that this pin in an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							I/O	**SPIFI_CS —** SPIFI serial flash chip select.
							I/O	**GPIO5[11] —** General purpose digital input/output pin.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P5_4	P9	-	80	57	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART 1.
							O	**T1_MAT0 —** Match output 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_5	P10	-	81	58	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							I/O	**EMC_D9 —** External memory data line 9.
							-	**R —** Function reserved.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							O	**T1_MAT1 —** Match output 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_6	T13	-	89	63	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I/O	**EMC_D10 —** External memory data line 10.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							O	**T1_MAT2 —** Match output 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_7	R12	-	91	65	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
							O	**MCOA2 —** Motor control PWM channel 2, output A.
							I/O	**EMC_D11 —** External memory data line 11.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							O	**T1_MAT3 —** Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_3	P15	-	113	79	[2]	N; PU	I/O	**GPIO3[2] —** General purpose digital input/output pin.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
							O	**EMC_CS1 —** LOW active Chip Select 1 signal.
							-	**R —** Function reserved.
							I	**T2_CAP2 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_4	R16	F6	114	80	[2]	N; PU	I/O	**GPIO3[3] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
							O	**U0_TXD —** Transmitter output for USART0.
							O	**EMC_CAS —** LOW active SDRAM Column Address Strobe.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_5	P16	F9	117	82	[2]	N; PU	I/O	**GPIO3[4] —** General purpose digital input/output pin.
							O	**CTOUT_6 —** SCT output 6. Match output 2 of timer 1.
							I	**U0_RXD —** Receiver input for USART0.
							O	**EMC_RAS —** LOW active SDRAM Row Address Strobe.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_6	L14	-	119	83	[2]	N; PU	I/O	**GPIO0[5] —** General purpose digital input/output pin.
							O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
							I/O	**SGPIO5 —** General purpose digital input/output pin.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**T2_CAP3 —** Capture input 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P8_2	K4	-	36	-	[3]	N; PU	I/O	**GPIO4[2] —** General purpose digital input/output pin.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							-	**R —** Function reserved.
							I	**MCI0 —** Motor control PWM channel 0, input.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT2 —** Match output 2 of timer 0.
P8_3	J3	-	37	-	[2]	N; PU	I/O	**GPIO4[3] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							O	**LCD_VD19 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT3 —** Match output 3 of timer 0.
P8_4	J2	-	39	-	[2]	N; PU	I/O	**GPIO4[4] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
							-	**R —** Function reserved.
							O	**LCD_VD7 —** LCD data.
							O	**LCD_VD16 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
P8_5	J1	-	40	-	[2]	N; PU	I/O	**GPIO4[5] —** General purpose digital input/output pin.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							-	**R —** Function reserved.
							O	**LCD_VD6 —** LCD data.
							O	**LCD_VD8 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP1 —** Capture input 1 of timer 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PD_15	T15	-	101	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A17 —** External memory address line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[29] —** General purpose digital input/output pin.
							I	**SD_WP —** SD/MMC card write protect input.
							O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
PD_16	R14	-	104	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A16 —** External memory address line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[30] —** General purpose digital input/output pin.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
PE_0	P14	-	106	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A18 —** External memory address line 18.
							I/O	**GPIO7[0] —** General purpose digital input/output pin.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_1	N14	-	112	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A19 —** External memory address line 19.
							I/O	**GPIO7[1] —** General purpose digital input/output pin.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PE_6	M16	-	124	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
							I	**U1_RI —** Ring Indicator input for UART 1.
							I/O	**EMC_D25 —** External memory data line 25.
							I/O	**GPIO7[6] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_7	F15	-	149	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_5 —** SCT output 5. Match output 3 of timer 3.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**EMC_D26 —** External memory data line 26.
							I/O	**GPIO7[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_8	F14	-	150	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
							I	**U1_DSR —** Data Set Ready input for UART 1.
							I/O	**EMC_D27 —** External memory data line 27.
							I/O	**GPIO7[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_9	E16	-	152	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							I/O	**EMC_D28 —** External memory data line 28.
							I/O	**GPIO7[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
WAKEUP0	A9	A4	187	130	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 0 of the event monitor.No internal pull-up is enabled when this pin is configured as input.
WAKEUP1	A10	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 1 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP2	C9	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 2 of the event monitor. This pin does not have an internal pull-up.
WAKEUP3	D8	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. This pin does not have an internal pull-up.
ADC pins								
ADC0_0/ ADC1_0/DAC	E3	A2	8	6	[8]	I; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	A1	4	2	[8]	I; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	206	143	[8]	I; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	A3	200	139	[8]	I; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	-	199	138	[8]	I; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	-	208	144	[8]	I; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	-	204	142	[8]	I; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	-	197	136	[8]	I; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC								
RTC_ALARM	A11	C3	186	129	[11]	-	O	RTC controlled output.
RTCX1	A8	A5	182	125	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B5	183	126	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
$\overline{\text{SAMPLE}}$	B9	-	-	-	[11]	O	O	Event monitor sample output.
Crystal oscillator pins								

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.20.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event can also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.20.2 Motor control PWM

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input causes the PWM to release all motor drive outputs immediately . At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

7.20.3 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user code can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.20.3.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.

- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).

7.20.4 Repetitive Interrupt (RI) timer

The repetitive interrupt timer provides a free-running 32-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare function can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.20.4.1 Features

- 32-bit counter. Counter can be free-running or be reset by a generated interrupt.
- 32-bit compare value.
- 32-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This mechanism allows for combinations not possible with a simple compare.

7.20.5 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.20.5.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the IRC as the clock source.

7.21 Analog peripherals

7.21.1 Analog-to-Digital Converter (ADC0/1)

Remark: The LPC435x/3x/2x/1x contain two 10-bit ADCs.

7.21.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.21.2 Digital-to-Analog Converter (DAC)

7.21.2.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

7.22 Peripherals in the RTC power domain

7.22.1 RTC

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.22.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.

7.23.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.23.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC435x/3x/2x/1x.

7.23.9 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC435x/3x/2x/1x support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
   a. Deep-sleep mode
   b. Power-down mode
   c. Deep power-down mode

Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature	-	-	-	125	°C

Table 9. Thermal resistance (LQFP packages)

Symbol	Parameter	Conditions	Thermal resistance in °C/W ±15 %	
			LQFP144	LQFP208
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	38	31
		Single-layer (4.5 in × 3 in); still air	50	39
$R_{th(j-c)}$	thermal resistance from junction to case	-	11	10

Table 10. Thermal resistance value (BGA packages)

Symbol	Parameter	Conditions	Thermal resistance in °C/W ±15 %	
			LBGA256	TFBGA100
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	29	46
		8-layer (4.5 in × 3 in); still air	24	37
$R_{th(j-c)}$	thermal resistance from junction to case		14	11

10. Static characteristics

Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage		[17]	2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_ DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; ARM Cortex-M0 core in reset; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
		CCLK = 204 MHz	[4]	-	83	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled; ARM Cortex-M0 core in reset					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-		0.1	nA

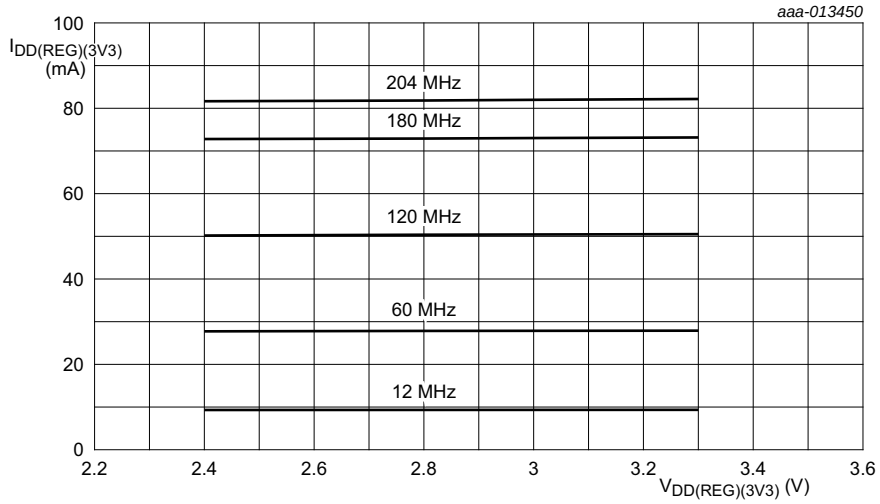
[16] The parameter value specified is a simulated value excluding bond capacitance.

[17] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[18] $V_{DD(IO)}$ present.

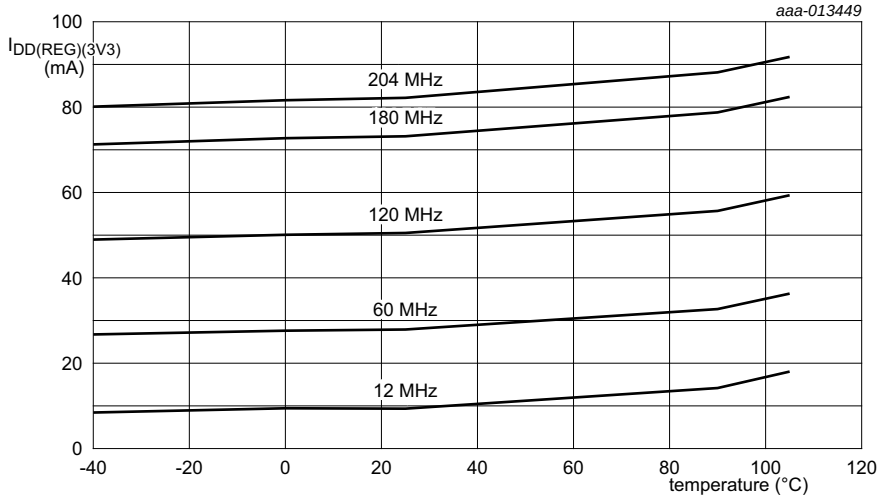
[19] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

10.1 Power consumption



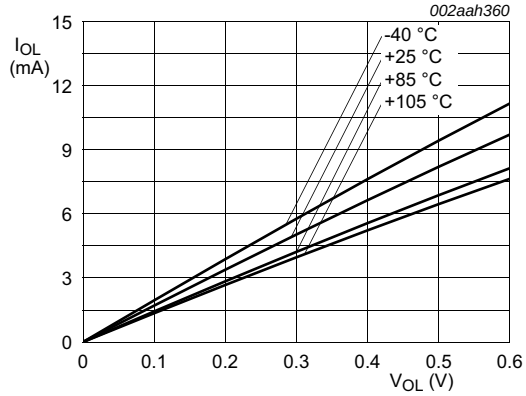
Conditions: T_{amb} = 25 °C; executing code while (1){} from SRAM; M0 core in reset; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus regulator supply voltage $V_{DD(REEG)(3V3)}$ in active mode

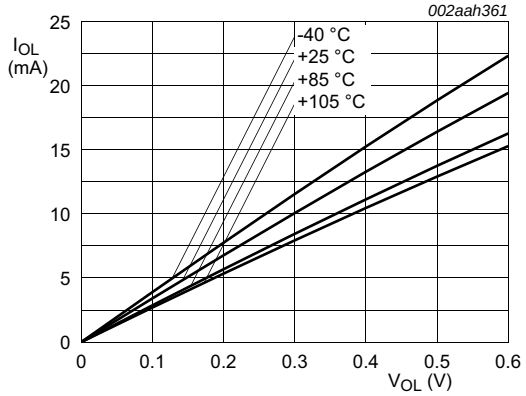


Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; M0 core in reset; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

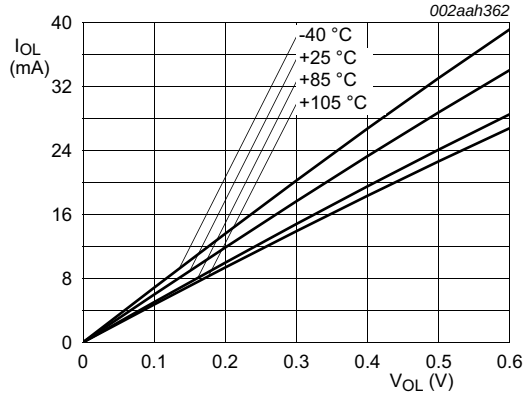
Fig 12. Typical supply current versus temperature in active mode



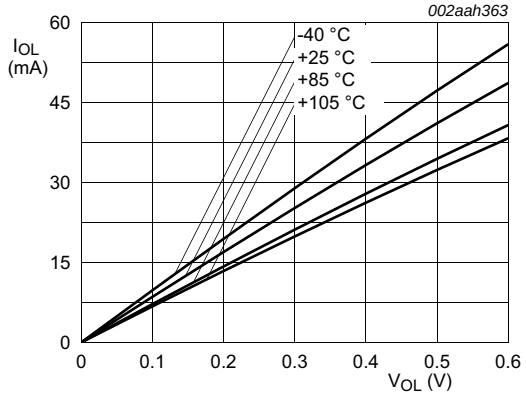
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 22. High-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}

11.7 GPCLKIN

Table 22. Dynamic characteristic: GPCLKIN

T_{amb} = 25 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V

Symbol	Parameter	Min	Typ	Max	Unit
GP_CLKIN	input frequency	-	-	25	MHz

11.8 I/O pins

Table 23. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	1.0	-	2.5	ns
t_f	fall time	pin configured as output; EHS = 1	[2][3]	0.9	-	2.5	ns
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.3	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.9	-	4.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high drive strength							
t_r	rise time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.3	-	7.9	ns
t_f	fall time	pin configured as output; standard drive mode (EHD = 0x0)	[2][5]	4.7	-	8.7	ns
t_r	rise time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.7	ns
t_f	fall time	pin configured as output; medium drive mode (EHD = 0x1)	[2][5]	3.2	-	5.5	ns
t_r	rise time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.9	-	4.9	ns
t_f	fall time	pin configured as output; high drive mode (EHD = 0x2)	[2][5]	2.5	-	3.9	ns
t_r	rise time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.8	-	4.7	ns
t_f	fall time	pin configured as output; ultra-high drive mode (EHD = 0x3)	[2][5]	2.4	-	3.4	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns
I/O pins - high-speed							
t_r	rise time	pin configured as output; EHS = 1	[2][3]	350	-	670	ps
t_f	fall time	pin configured as output; EHS = 1	[2][3]	450	-	730	ps
t_r	rise time	pin configured as output; EHS = 0	[2][3]	1.0	-	1.9	ns
t_f	fall time	pin configured as output; EHS = 0	[2][3]	1.0	-	2.0	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

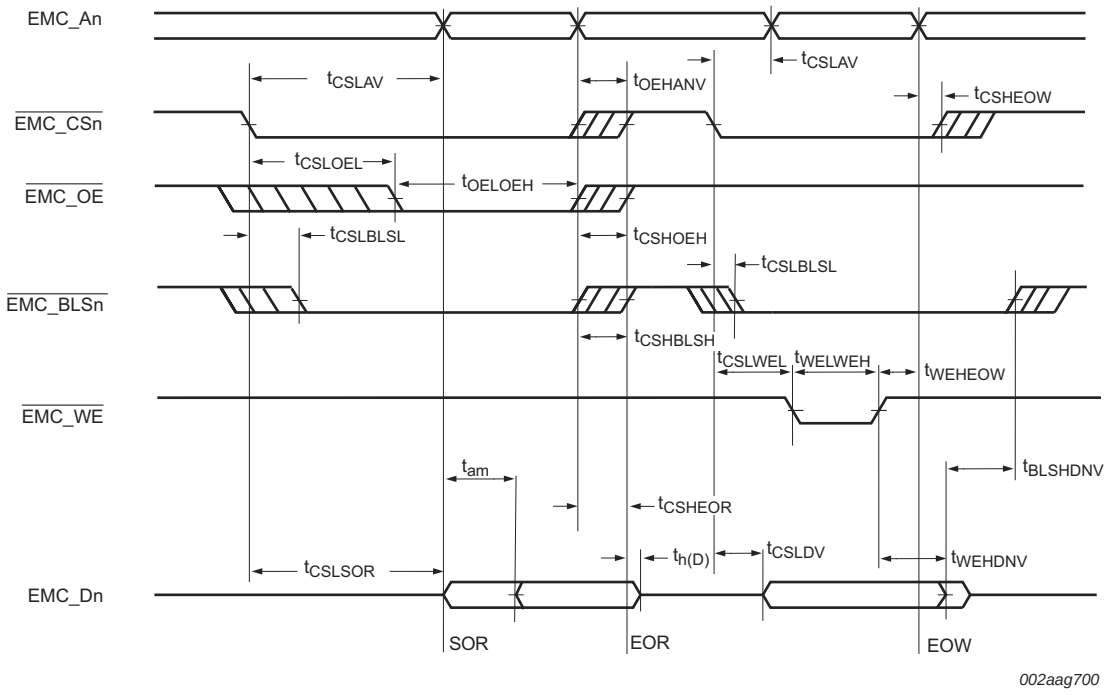
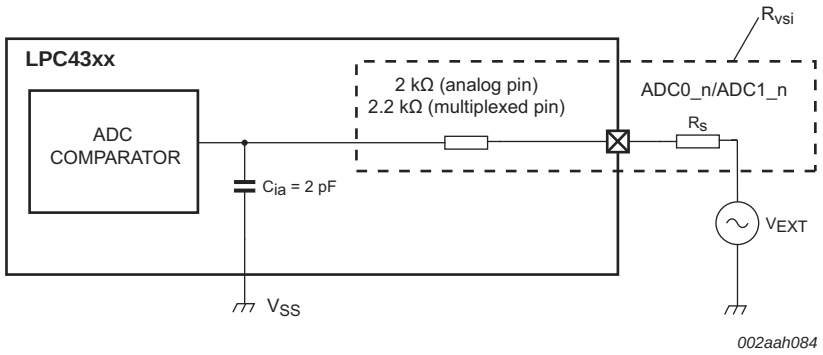


Fig 36. External static memory read/write access (PB = 1)



$Rs < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 42. ADC interface to pins

Table 40. DAC characteristics

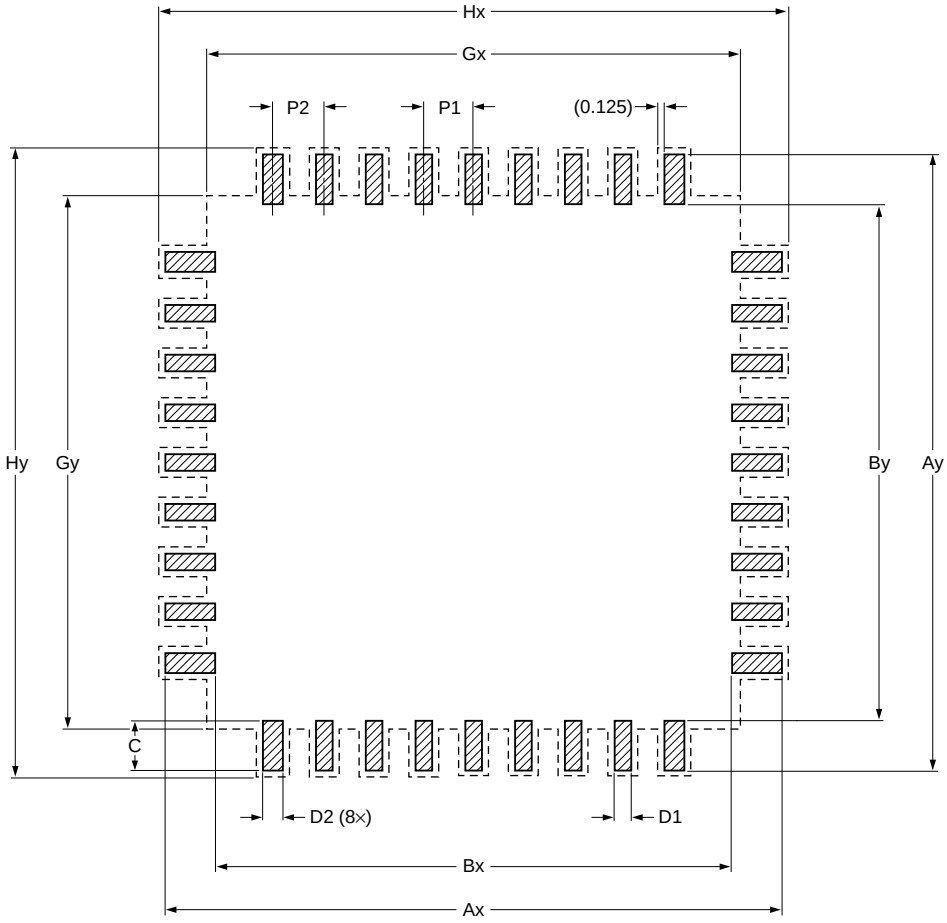
$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.8	-	LSB
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 $2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±1.0	-	LSB
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.5	-	LSB
E_O	offset error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.8	-	LSB
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
E_G	gain error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.3	-	%
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[2]		0.4		μσ

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC43xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 56. Reflow soldering of the LQFP208 package