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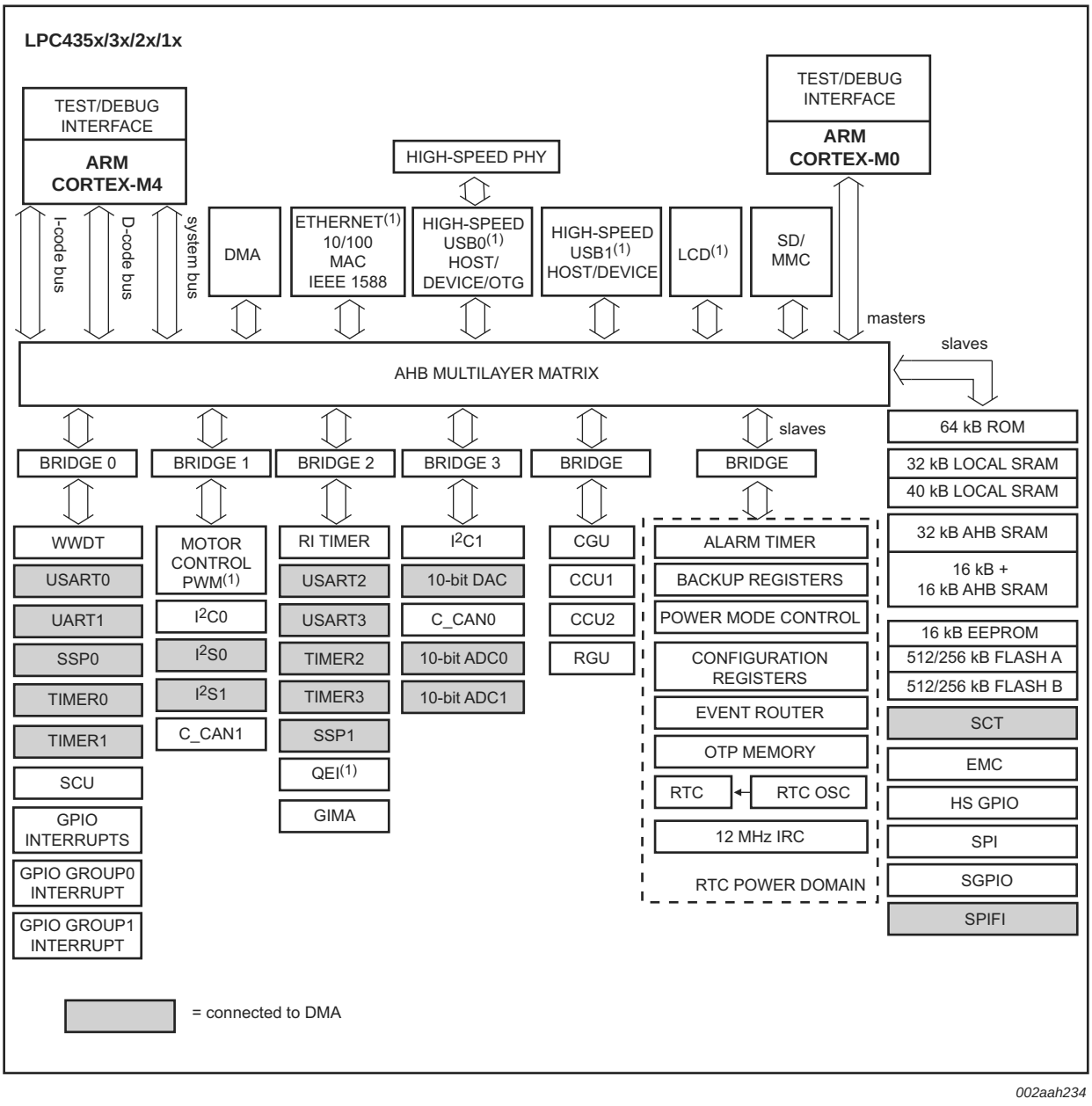
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4322jbd144e

5. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. LPC435x/3x/2x/1x Block diagram

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_12	R9	K7	78	56	[2]	N; PU	I/O	**GPIO1[5] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D5 —** External memory data line 5.
							I	**T0_CAP1 —** Capture input 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
P1_13	R10	H8	83	60	[2]	N; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D6 —** External memory data line 6.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							I	**SD_CD —** SD/MMC card detect input.
P1_14	R11	J8	85	61	[2]	N; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D7 —** External memory data line 7.
							O	**T0_MAT2 —** Match output 2 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P1_15	T12	K8	87	62	[2]	N; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**SGPIO2 —** General purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1 —** Match output 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P3_2	F11	G6	166	116	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	A7	169	118	[4]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_SCK —** Serial clock for SPI.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification.
P3_4	A15	B8	171	119	[2]	N; PU	I/O	**GPIO1[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD13 —** LCD data.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P4_0	D5	-	1	1	[2]	N; PU	I/O	**GPIO2[0] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							I	**NMI —** External interrupt input to NMI.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD13 —** LCD data.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							-	**R —** Function reserved.
P4_1	A1	-	3	3	[5]	N; PU	I/O	**GPIO2[1] —** General purpose digital input/output pin.
							O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
							O	**LCD_VD0 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD19 —** LCD data.
							O	**U3_TXD —** Transmitter output for USART3.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							AI	**ADC0_1 —** ADC0 and ADC1, input channel 1. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P4_2	D3	-	12	8	[2]	N; PU	I/O	**GPIO2[2] —** General purpose digital input/output pin.
							O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
							O	**LCD_VD3 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD12 —** LCD data.
							I	**U3_RXD —** Receiver input for USART3.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
P4_3	C2	-	10	7	[5]	N; PU	I/O	**GPIO2[3] —** General purpose digital input/output pin.
							O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
							O	**LCD_VD2 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD21 —** LCD data.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							AI	**ADC0_0 —** DAC, ADC0 and ADC1, input channel 0. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P5_4	P9	-	80	57	[2]	N; PU	I/O	**GPIO2[13] —** General purpose digital input/output pin.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.
							I	**U1_CTS —** Clear to Send input for UART 1.
							O	**T1_MAT0 —** Match output 0 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_5	P10	-	81	58	[2]	N; PU	I/O	**GPIO2[14] —** General purpose digital input/output pin.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							I/O	**EMC_D9 —** External memory data line 9.
							-	**R —** Function reserved.
							I	**U1_DCD —** Data Carrier Detect input for UART 1.
							O	**T1_MAT1 —** Match output 1 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_6	T13	-	89	63	[2]	N; PU	I/O	**GPIO2[15] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I/O	**EMC_D10 —** External memory data line 10.
							-	**R —** Function reserved.
							O	**U1_TXD —** Transmitter output for UART 1.
							O	**T1_MAT2 —** Match output 2 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P5_7	R12	-	91	65	[2]	N; PU	I/O	**GPIO2[7] —** General purpose digital input/output pin.
							O	**MCOA2 —** Motor control PWM channel 2, output A.
							I/O	**EMC_D11 —** External memory data line 11.
							-	**R —** Function reserved.
							I	**U1_RXD —** Receiver input for UART 1.
							O	**T1_MAT3 —** Match output 3 of timer 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P7_6	C7	-	194	134	[2]	N; PU	I/O	**GPIO3[14] —** General purpose digital input/output pin.
							O	**CTOUT_11 —** SCT output 1. Match output 3 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_7	B6	-	201	140	[5]	N; PU	I/O	**GPIO3[15] —** General purpose digital input/output pin.
							O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
							AI	**ADC1_6 —** ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P8_0	E5	-	2	-	[3]	N; PU	I/O	**GPIO4[0] —** General purpose digital input/output pin.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							I	**MCI2 —** Motor control PWM channel 2, input.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT0 —** Match output 0 of timer 0.
P8_1	H5	-	34	-	[3]	N; PU	I/O	**GPIO4[1] —** General purpose digital input/output pin.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							-	**R —** Function reserved.
							I	**MCI1 —** Motor control PWM channel 1, input.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T0_MAT1 —** Match output 1 of timer 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P8_6	K3	-	43	-	[2]	N; PU	I/O	**GPIO4[6] —** General purpose digital input/output pin.
							I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
							-	**R —** Function reserved.
							O	**LCD_VD5 —** LCD data.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP2 —** Capture input 2 of timer 0.
P8_7	K1	-	45	-	[2]	N; PU	I/O	**GPIO4[7] —** General purpose digital input/output pin.
							O	**USB1_ULPI_STP —** ULPI link STP signal. Asserted to end or interrupt transfers to the PHY.
							-	**R —** Function reserved.
							O	**LCD_VD4 —** LCD data.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**T0_CAP3 —** Capture input 3 of timer 0.
P8_8	L1	-	49	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CGU_OUT0 —** CGU spare clock output 0.
							O	**I2S1_TX_MCLK —** I2S1 transmit master clock.
P9_0	T1	-	59	-	[2]	N; PU	I/O	**GPIO4[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
							I/O	**SGPIO0 —** General purpose digital input/output pin.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PA_2	K15	-	136	-	[3]	N; PU	I/O	**GPIO4[9] —** General purpose digital input/output pin.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_3	H11	-	147	-	[3]	N; PU	I/O	**GPIO4[10] —** General purpose digital input/output pin.
							I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PA_4	G13	-	151	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A23 —** External memory address line 23.
							I/O	**GPIO5[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PB_0	B15	-	164	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
							O	**LCD_VD23 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[20] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PD_7	T6	-	72	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
							I/O	**EMC_D21 —** External memory data line 21.
							-	**R —** Function reserved.
							I/O	**GPIO6[21] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
PD_8	P8	-	74	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
							I/O	**EMC_D22 —** External memory data line 22.
							-	**R —** Function reserved.
							I/O	**GPIO6[22] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
PD_9	T11	-	84	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_13 —** SCT output 13. Match output 3 of timer 3.
							I/O	**EMC_D23 —** External memory data line 23.
							-	**R —** Function reserved.
							I/O	**GPIO6[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
PD_10	P11	-	86	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							O	**$\overline{\text{EMC\_BLS3}}$ —** LOW active Byte Lane select signal 3.
							-	**R —** Function reserved.
							I/O	**GPIO6[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PF_9	D6	-	203	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**GPIO7[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO3 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	205	-	[5]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**SD_WP —** SD/MMC card write protect input.
							-	**R —** Function reserved.
							AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	207	-	[5]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[25] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							-	**R —** Function reserved.
							AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

7.5 AHB multilayer matrix

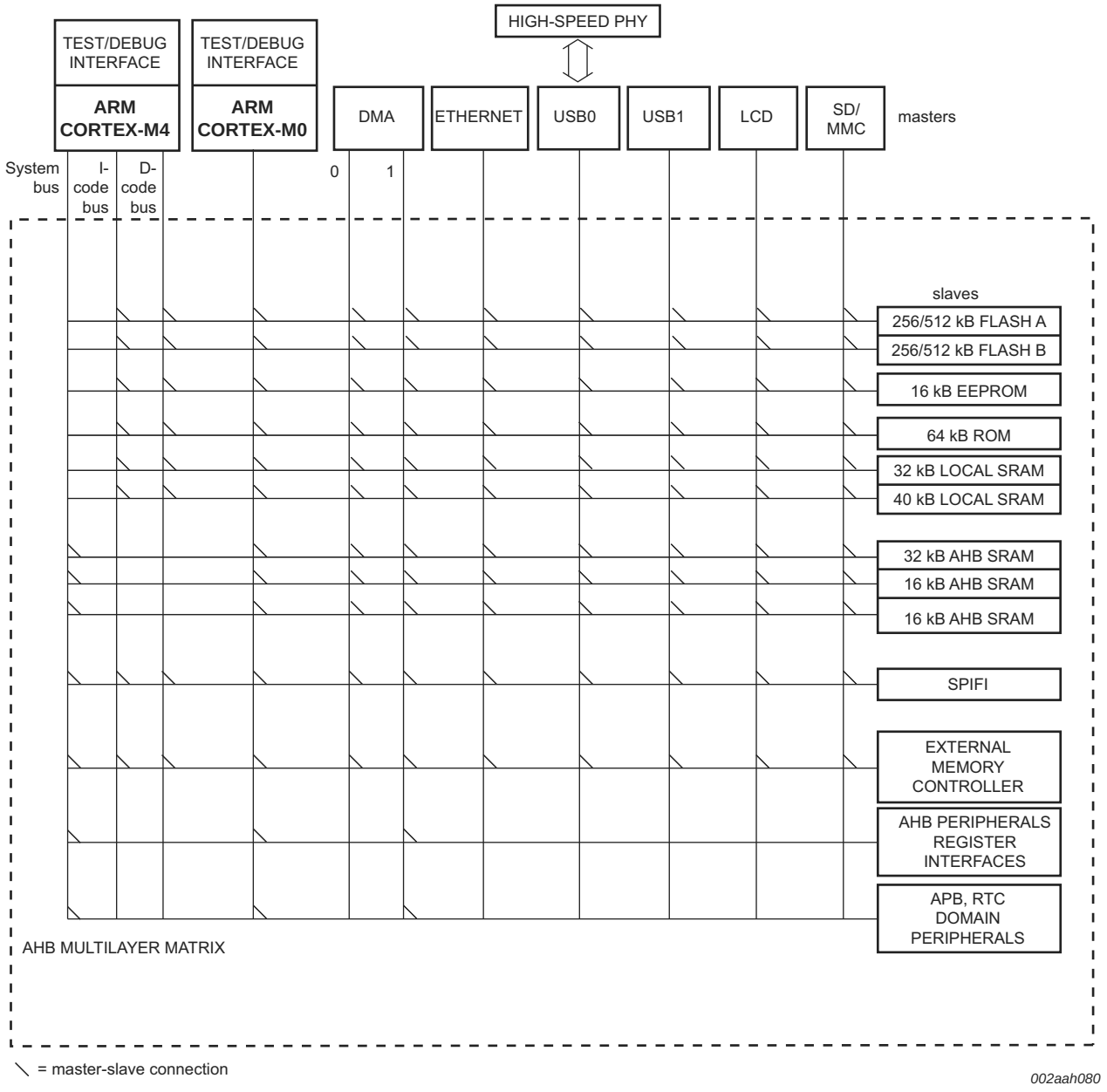


Fig 6. AHB multilayer matrix master and slave connections

7.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The ARM Cortex-M0 co-processor has its own NVIC with 32 vectored interrupts. Most peripheral interrupts are shared between the Cortex-M0 and Cortex-M4 NVICs.

- Each slice has a 32-bit pattern match filter.

7.18 AHB peripherals

7.18.1 General Purpose DMA

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.18.1.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.18.2 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.

Table 6. EMC pinout for different packages

Function	LBGA256	TFBGA100	LQFP208	LQFP144
$\overline{OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$
$\overline{WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$
CKEOUT	EMC_ CKEOUT[3:0]	EMC_ CKEOUT[1:0]	EMC_ CKEOUT[1:0]	EMC_ CKEOUT[1:0]
CLK	EMC_CLK[3:0]; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23
DQMOUT	EMC_ DQMOUT[3:0]	-	EMC_ DQMOUT[1:0]	EMC_ DQMOUT[1:0]
$\overline{DYCS}$	$\overline{EMC\_DYCS[3:0]}$	$\overline{EMC\_DYCS[1:0]}$	$\overline{EMC\_DYCS[2:0]}$	$\overline{EMC\_DYCS[1:0]}$
$\overline{CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$
$\overline{RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$

7.18.4.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

7.19.5 I²C-bus interface

Remark: The LPC435x/3x/2x/1x each contain two I²C-bus interfaces.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.19.5.1 Features

- I²C0 is a standard I²C compliant bus interface with open-drain pins. I²C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I²C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I²C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- All I²C-bus controllers support multiple address recognition and a bus monitor mode.

7.19.6 I²S interface

Remark: The LPC435x/3x/2x/1x each contain two I²S-bus interfaces.

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

There are three levels of the Code Read Protection:

- In level CRP1, access to the chip via the JTAG is disabled. Partial flash updates are allowed (excluding flash sector 0) using a limited set of the ISP commands. This level is useful when CRP is required and flash field updates are needed. CRP1 does prevent the user code from erasing all sectors.
- In level CRP2, access to the chip via the JTAG is disabled. Only a full flash erase and update using a reduced set of the ISP commands is allowed.
- In level CRP3, any access to the chip via the JTAG pins or the ISP is disabled. This mode also disables the ISP override using P2_7 pin. If necessary, the application code must provide a flash update mechanism using the IAP calls or using the reinvoke ISP command to enable flash update via USART0. See Table 5.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.24 Serial Wire Debug/JTAG

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

Remark: Serial Wire Debug is supported for the ARM Cortex-M4 only,

The ARM Cortex-M0 coprocessor supports JTAG debug. A standard ARM Cortex-compliant debugger can debug the ARM Cortex-M4 and the ARM Cortex-M0 cores separately or both cores simultaneously.

Remark: In order to debug the ARM Cortex-M0, release the M0 reset by software in the RGU block.

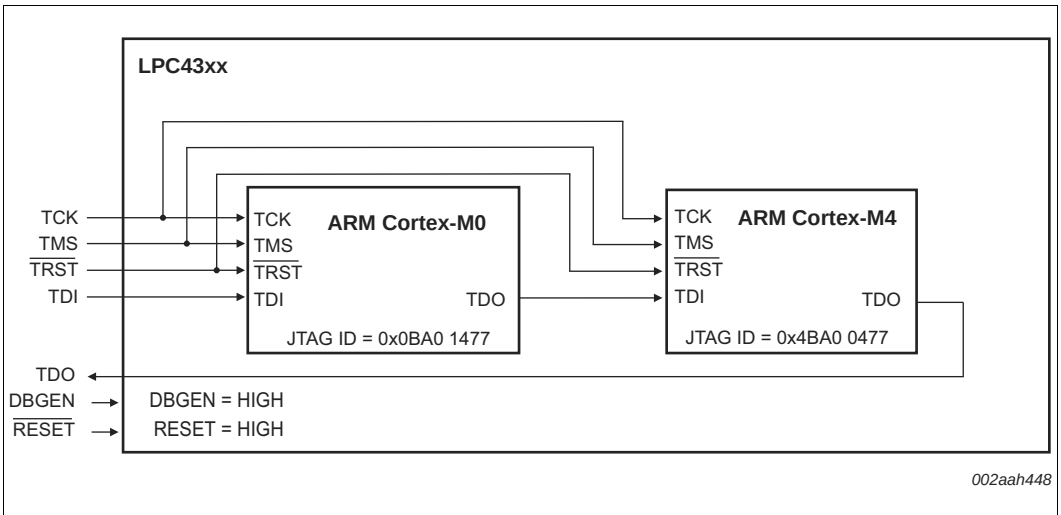
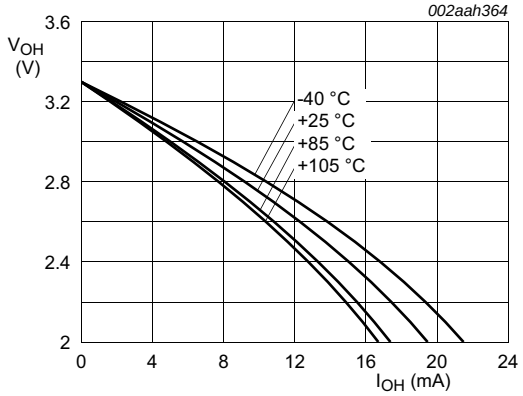
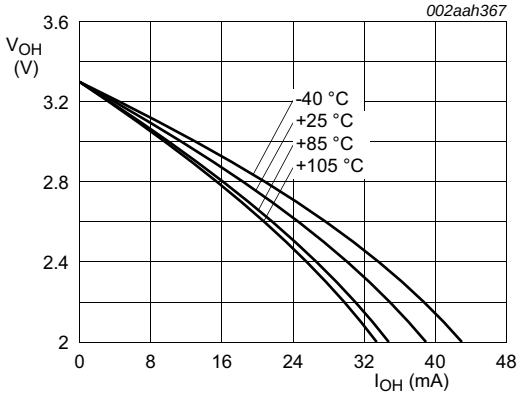


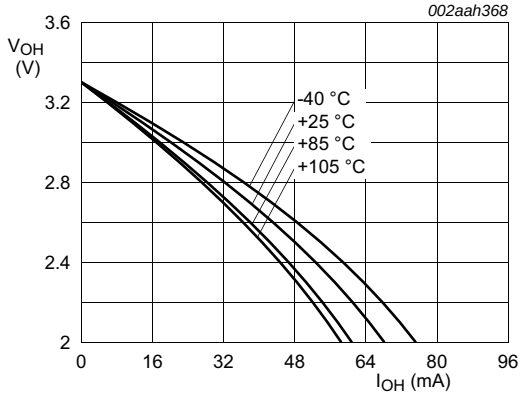
Fig 10. Dual-core debug configuration



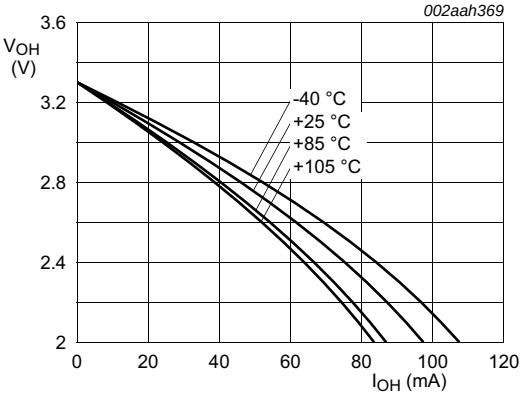
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 23. High-drive pins; typical HIGH level output voltage V_{OH} versus HGH level output current I_{OH}

[9] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

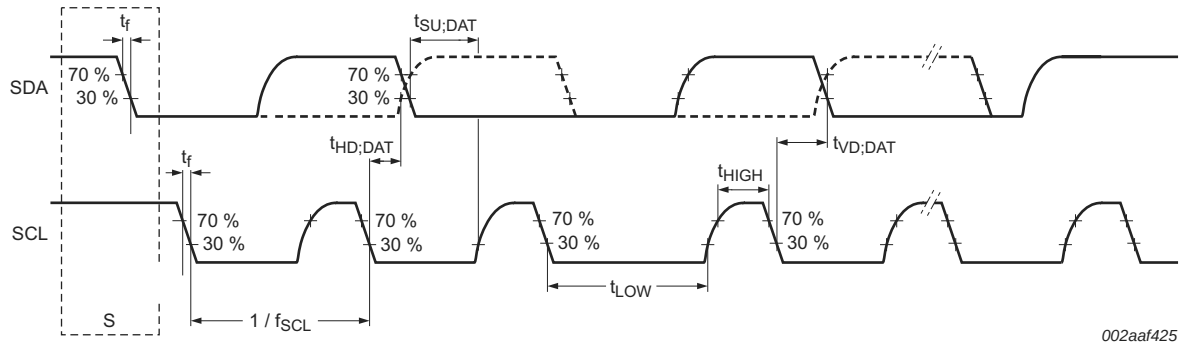


Fig 27. I^2C-bus pins clock timing

11.10 I^2S-bus interface

Table 25. Dynamic characteristics: I^2S-bus interface pins

T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF. Conditions and data refer to I2S0 and I2S1 pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
common to input and output							
t_r	rise time			-	4	-	ns
t_f	fall time			-	4	-	ns
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK		36	-	-	ns
output							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[1]	-	4.4	-	ns
		on pin I2Sx_TX_WS		-	4.3	-	ns
input							
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[1]	-	0	-	ns
		on pin I2Sx_RX_WS			0.20		ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[1]	-	3.7	-	ns
		on pin I2Sx_RX_WS		-	3.9	-	ns

[1] Clock to the I^2S-bus interface BASE_APB1_CLK = 150 MHz; peripheral clock to the I^2S-bus interface PCLK = BASE_APB1_CLK / 12. I^2S clock cycle time $T_{cy(clk)}$ = 79.2 ns, corresponds to the SCK signal in the *I^2S-bus specification*.

13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{RTCX1} and C_{RTCX2} need to be connected externally. Typical capacitance values for C_{RTCX1} and C_{RTCX2} are $C_{RTCX1/2}$ = 20 (typical) $\pm$ 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

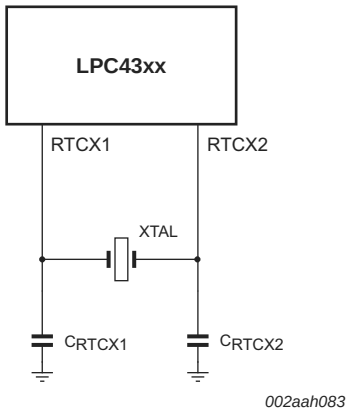


Fig 45. RTC 32 kHz oscillator circuit

13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. Also connect the external components to the ground plain. To keep the noise coupled in via the PCB as small as possible, make loops and parasitics as small as possible. Choose smaller values of C_{X1} and C_{X2} if parasitics increase in the PCB layout.

Ensure that no high-speed or high-drive signals are near the RTCX1/2 signals.

13.5 Standard I/O pin configuration

Figure 46 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input buffer enabled/disabled
- Analog input

The default configuration for standard I/O pins is input buffer disabled and pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

16. Abbreviations

Table 46. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
BOD	BrownOut Detection
CAN	Controller Area Network
CMAC	Cipher-based Message Authentication Code
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DAC	Digital-to-Analog Converter
DC-DC	Direct Current-to-Direct Current
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MAC	Media Access Control
MCU	MicroController Unit
MIIM	Media Independent Interface Management
n.c.	not connected
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PMC	Power Mode Control
PWM	Pulse Width Modulator
RIT	Repetitive Interrupt Timer
RMII	Reduced Media Independent Interface
SDRAM	Synchronous Dynamic Random Access Memory
SIMD	Single Instruction Multiple Data
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USART	Universal Synchronous Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
UTMI	USB2.0 Transceiver Macrocell Interface

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• SD/MMC timing data updated. See Table 35 “Dynamic characteristics: SD/MMC”. • IEEE standard 802.3 compliance added to Section 11.18. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals. • SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 “SSP in SPI mode and SPI master timing”. • Parameters t_{lead}, t_{lag}, and t_d added in Table 25 “Dynamic characteristics: SSP pins in SPI mode”. • Parameter t_{CSLWEL} with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 29 “Dynamic characteristics: Static asynchronous external memory interface”. • Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 29 “Dynamic characteristics: Static asynchronous external memory interface”. • Removed restriction on C_CAN bus usage. See CAN.1 errata in Ref. 2. • General-purpose OTP size corrected.			
LPC435X_3X_2X_1X v.3	20121206	Preliminary data sheet	-	LPC4357_53_37_33 v.2.1
Modifications:	• TFBGA180 packages removed. • Part LPC432x and LPC431x added. • SCT dither engine added and SCT bi-directional event enable features added. • Figure 10 “Dual-core debug configuration” added. • T = 105 °C data added in Figure 20 to Figure 23. • Change symbol names and parameter names in Table 21. • Parameter I_{LH} updated for condition V_I = 5 V and T_{amb} = 25 °C/105 °C in Table 11. • Power consumption data added in Section 10.1. • SPIFI dynamic characteristics added in Section 11.16. • IRC accuracy corrected to ± 2 % for T_{amb} = -40 °C to 0 °C and T_{amb} = 85 °C to 105 °C. • Pull-up and Pull-down current data (Figure 24 and Figure 25) updated with data for T_{amb} = 105 °C. • SPIFI maximum data rate changed to 52 MB per second. • Recommendation for V_{BAT} use added: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT}$ + 0.2 V. • Table 14 “Band gap characteristics” added. • Section 7.23.9 “Power Management Controller (PMC)” added. • Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. • OTP memory size changed to 64 bit. • Use of C_CAN peripheral restricted in Section 2. • ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.			
LPC4357_53_37_33 v.2.1	20120904	Preliminary data sheet	-	LPC4357_53_37_33 v.2
Modifications:	• SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • SWD removed for ARM Cortex-M0. • BOD de-assertion levels added in Table 13. • Peripheral power consumption data added in Table 12. • Minimum value for all supply voltages changed to -0.5 V in Table 7.			