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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	104K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4323jbd144e

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_16	M7	H9	90	64	[2]	N; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**SGPIO3 —** General purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
							O	**T0_MAT0 —** Match output 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D9 —** External memory data line 9.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
P1_17	M8	H10	93	66	[3]	N; PU	I/O	**GPIO0[12] —** General purpose digital input/output pin.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.
							-	**R —** Function reserved.
							I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
							I	**T0_CAP3 —** Capture input 3 of timer 0.
							O	**CAN1_TD —** CAN1 transmitter output.
							I/O	**SGPIO11 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P1_18	N12	J10	95	67	[2]	N; PU	I/O	**GPIO0[13] —** General purpose digital input/output pin.
							I/O	**U2_DIR —** RS-485/EIA-485 output enable/direction control for USART2.
							-	**R —** Function reserved.
							O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
							O	**T0_MAT3 —** Match output 3 of timer 0.
							I	**CAN1_RD —** CAN1 receiver input.
							I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**EMC_D10 —** External memory data line 10.
P1_19	M11	K9	96	68	[2]	N; PU	I	**ENET_TX_CLK (ENET_REF_CLK) —** Ethernet Transmit Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**CLKOUT —** Clock output pin.
							-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I2S receive master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I^2S-bus specification.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P2_2	M15	F5	121	84	[2]	N; PU	I/O	**SGPIO6 —** General purpose digital input/output pin.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**EMC_A11 —** External memory address line 11.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[2] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							O	**$\overline{\text{EMC\_CS1}}$ —** LOW active Chip Select 1 signal.
P2_3	J12	D8	127	87	[3]	N; PU	I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**U3_TXD —** Transmitter output for USART3. See Table 4 for ISP mode.
							I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	**GPIO5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
P2_4	K11	D9	128	88	[3]	N; PU	I/O	**SGPIO13 —** General purpose digital input/output pin.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							I	**U3_RXD —** Receiver input for USART3. See Table 4 for ISP mode.
							I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	**GPIO5[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_7	J13	-	123	85	[2]	N; PU	-	**R —** Function reserved.
							I/O	**EMC_A15 —** External memory address line 15.
							I/O	**SGPIO6 —** General purpose digital input/output pin.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[15] —** General purpose digital input/output pin.
							O	**T2_MAT0 —** Match output 0 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_8	H13	-	125	86	[2]	N; PU	-	**R —** Function reserved.
							I/O	**EMC_A14 —** External memory address line 14.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[16] —** General purpose digital input/output pin.
							O	**T2_MAT1 —** Match output 1 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_9	J15	F8	139	97	[2]	N; PU	I/O	**GPIO3[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_DYCS0}}$ —** SDRAM chip select 0.
							-	**R —** Function reserved.
							O	**T2_MAT2 —** Match output 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_10	H15	-	142	100	[2]	N; PU	I/O	**GPIO3[6] —** General purpose digital input/output pin.
							O	**$\overline{\text{MCABORT}}$ —** Motor control PWM, LOW-active fast abort.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT1 —** Data mask 1 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P7_2	A16	-	165	115	[2]	N; PU	I/O	**GPIO3[10] —** General purpose digital input/output pin.
							I	**CTIN_4 —** SCT input 4. Capture input 2 of timer 1.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD18 —** LCD data.
							O	**LCD_VD6 —** LCD data.
							-	**R —** Function reserved.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**SGPIO6 —** General purpose digital input/output pin.
P7_3	C13	-	167	117	[2]	N; PU	I/O	**GPIO3[11] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
							-	**R —** Function reserved.
							O	**LCD_VD17 —** LCD data.
							O	**LCD_VD5 —** LCD data.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_4	C8	-	189	132	[5]	N; PU	I/O	**GPIO3[12] —** General purpose digital input/output pin.
							O	**CTOUT_13 —** SCT output 13. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD16 —** LCD data.
							O	**LCD_VD4 —** LCD data.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_4 —** ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
P7_5	A7	-	191	133	[5]	N; PU	I/O	**GPIO3[13] —** General purpose digital input/output pin.
							O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_VD8 —** LCD data.
							O	**LCD_VD23 —** LCD data.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							AI	**ADC0_3 —** ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PB_5	A12	-	181	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D4 —** ULPI link bidirectional data line 4.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[25] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCT input 7.
							O	**LCD_PWR —** LCD panel power enable.
							-	**R —** Function reserved.
PB_6	A6	-	-	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D3 —** ULPI link bidirectional data line 3.
							O	**LCD_VD13 —** LCD data.
							-	**R —** Function reserved.
							I/O	**GPIO5[26] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
							O	**LCD_VD19 —** LCD data.
							-	**R —** Function reserved.
							AI	**ADC0_6 —** ADC0 and ADC1, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PC_0	D4	-	7	-	[5]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_CLK —** ULPI link CLK signal. 60 MHz clock generated by the PHY.
							-	**R —** Function reserved.
							I/O	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface).
							O	**LCD_DCLK —** LCD panel clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SD_CLK —** SD/MMC card clock.
							AI	**ADC1_1 —** ADC1 and ADC0, input channel 1. Configure the pin as input (USB_ULPI_CLK) and use the ADC function select register in the SCU to select the ADC.
PC_1	E4	-	9	-	[2]	N; PU	I/O	**USB1_ULPI_D7 —** ULPI link bidirectional data line 7.
							-	**R —** Function reserved.
							I	**U1_RI —** Ring Indicator input for UART 1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							I/O	**GPIO6[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**SD_VOLT0 —** SD/MMC bus voltage select output 0.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PD_3	P4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_6 —** SCT output 7. Match output 2 of timer 1.
							I/O	**EMC_D17 —** External memory data line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
PD_4	T2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
							I/O	**EMC_D18 —** External memory data line 18.
							-	**R —** Function reserved.
							I/O	**GPIO6[18] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
PD_5	P6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
							I/O	**EMC_D19 —** External memory data line 19.
							-	**R —** Function reserved.
							I/O	**GPIO6[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
PD_6	R6	-	68	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
							I/O	**EMC_D20 —** External memory data line 20.
							-	**R —** Function reserved.
							I/O	**GPIO6[20] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO10 —** General purpose digital input/output pin.

7.6.1 Features

- ARM Cortex-M4 core:
  - Controls system exceptions and peripheral interrupts
  - Support for up to 53 vectored interrupts
  - Eight programmable interrupt priority levels with hardware priority level masking
  - Relocatable vector table
  - Non-Maskable Interrupt (NMI)
  - Software interrupt generation
- ARM Cortex-M0 core:
  - Support for up to 32 interrupts
  - Four programmable interrupt priority levels with hardware priority level masking

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.7 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

Remark: The SysTick is not included in the ARM Cortex-M0 core implementation.

7.8 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts.
- C_CAN0/1 and QEI interrupts.
- Ethernet, USB0, USB1 signals.
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3).

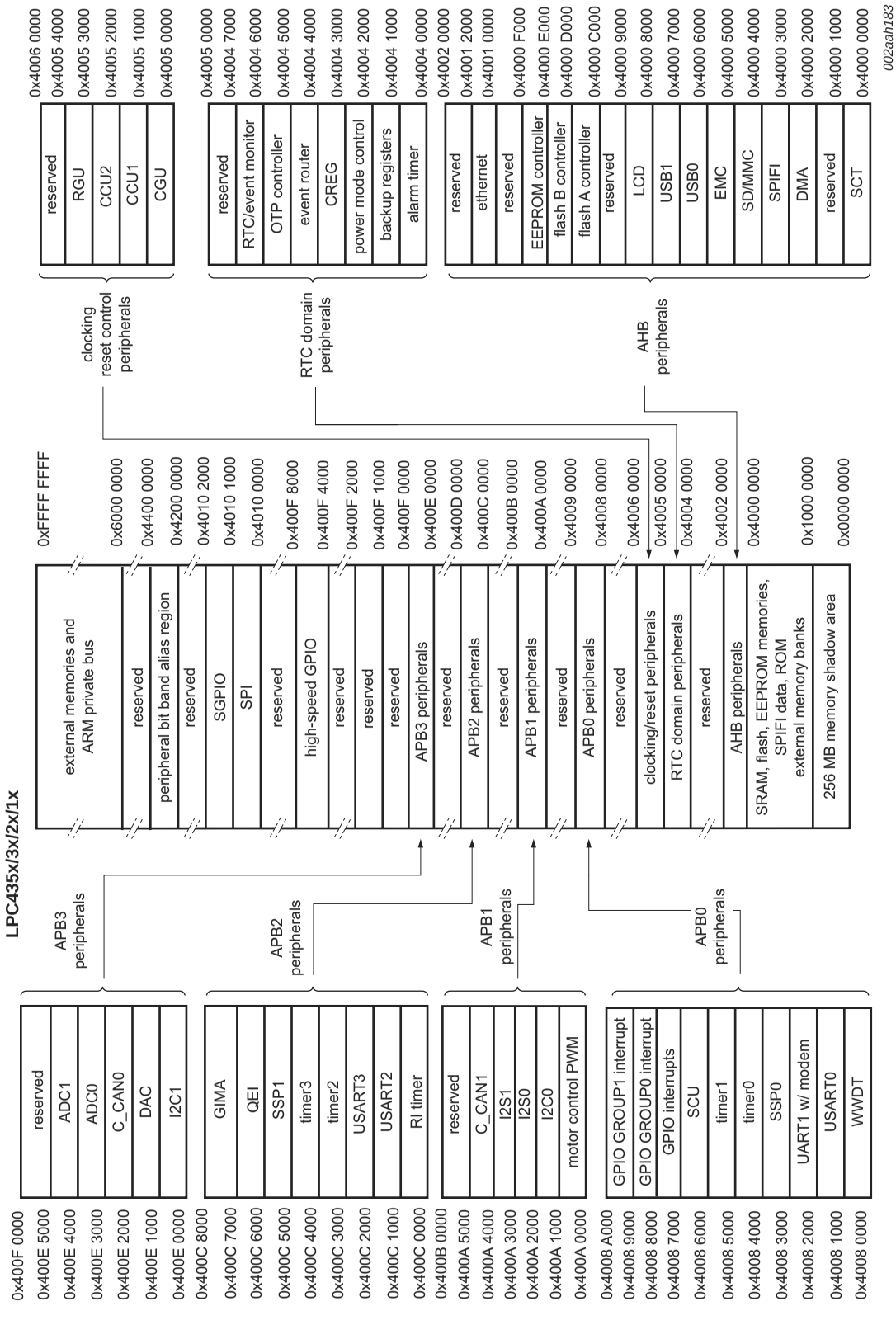


Fig 8. LPC435x/3x/2x/1x Memory mapping (peripherals)

- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.19 Digital serial peripherals

7.19.1 UART1

Remark: The LPC435x/3x/2x/1x contain one UART with standard transmit and receive data lines.

UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

UART1 includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.19.1.1 Features

- Maximum UART data bit rate of 8 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Equipped with standard modem interface signals. This module also provides full support for hardware flow control.
- Support for RS-485/9-bit/EIA-485 mode (UART1).
- DMA support.

7.19.2 USART0/2/3

Remark: The LPC435x/3x/2x/1x contain three USARTs. In addition to standard transmit and receive data lines, the USARTs support a synchronous mode.

The USARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −6 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−6	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		6	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86.5	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76.5	mA
I_{pd}	pull-down current	V_I = 5 V	[13] [14] [15]	-	93	-	μA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	μA
R_S	series resistance	on I/O pins with analog function; analog function enabled			200		Ω
I/O pins - high drive strength							
C_I	input capacitance			-	-	5.2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.4$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V

Table 11. Static characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[13] [14] [15]	-	62	-	µA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	µA
		$V_{DD(IO)} < V_I \leq$ 5 V		-	10	-	µA
I/O pins - high drive strength: standard drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	65	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	32	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	32	mA
I/O pins - high drive strength: medium drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.7	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	70	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	65	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	63	mA
I/O pins - high drive strength: high drive mode							
I_{LH}	HIGH-level leakage current	$V_I = V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	63	-	nA
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−14	-	-	mA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		14	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	113	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	110	mA
I/O pins - high drive strength: ultra-high drive mode							
I_{LH}	HIGH-level leakage current	V_I = $V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.6	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	63	-	nA
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(IO)}$ − 0.4 V		−20	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		20	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	165	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	156	mA
I/O pins - high-speed							
C_I	input capacitance			-	-	2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{LH}	HIGH-level leakage current	V_I = $V_{DD(IO)}$; on-chip pull-down resistor disabled		-	3	-	nA
		V_I = 5 V; T_{amb} = 25 °C		-	0.5	-	nA
		V_I = 5 V; T_{amb} = 105 °C		-	40	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function;					
		$V_{DD(IO)} \geq$ 2.4 V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V

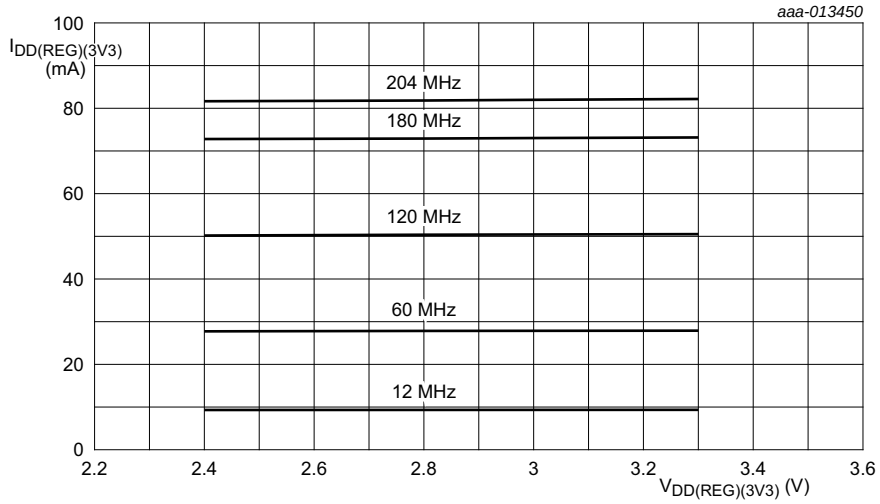
[16] The parameter value specified is a simulated value excluding bond capacitance.

[17] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[18] $V_{DD(IO)}$ present.

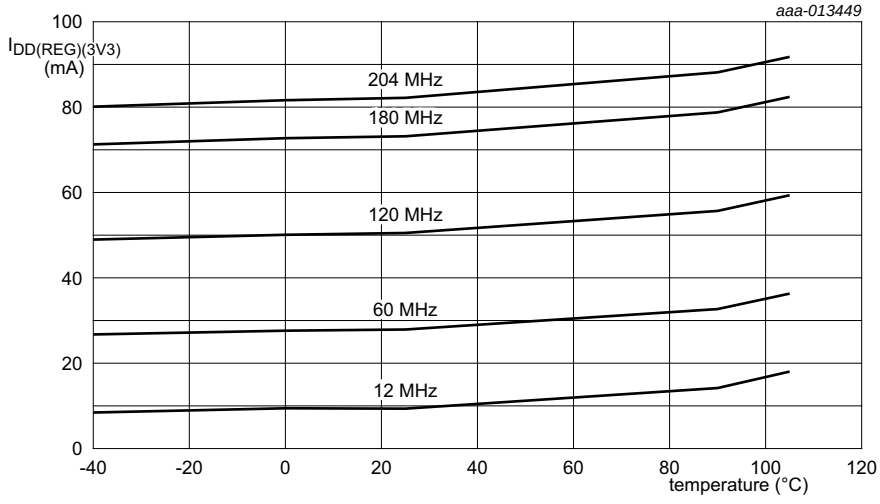
[19] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

10.1 Power consumption



Conditions: T_{amb} = 25 °C; executing code while (1){} from SRAM; M0 core in reset; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus regulator supply voltage $V_{DD(REEG)(3V3)}$ in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; M0 core in reset; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 12. Typical supply current versus temperature in active mode

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		0.5 x $T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		0.5 × $T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$ + 1.5	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$ + 1.5	-	-	ns
		microwire frame format		0.5 × $T_{cy(clk)}$	-	-	ns
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

11.14 SSP/SPI timing diagrams

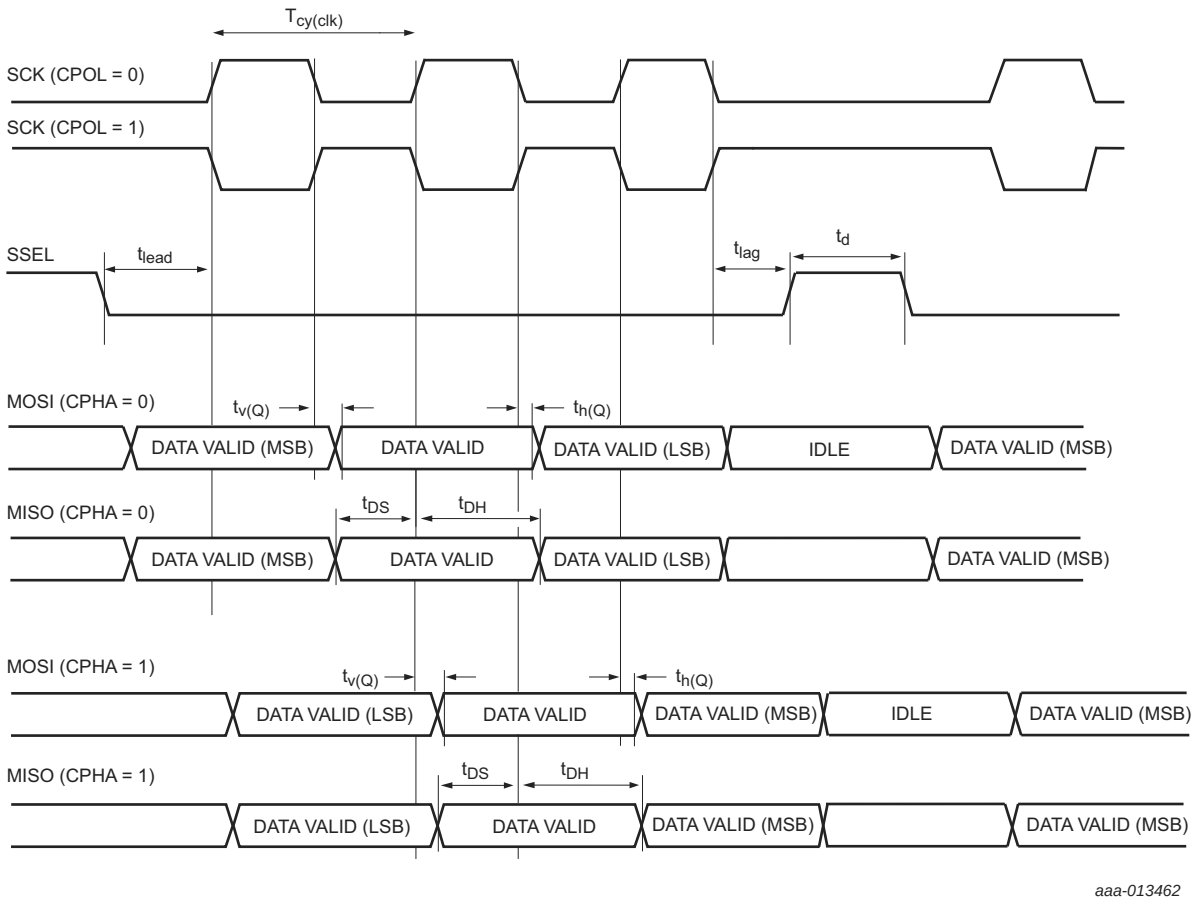


Fig 31. SSP in SPI mode and SPI master timing

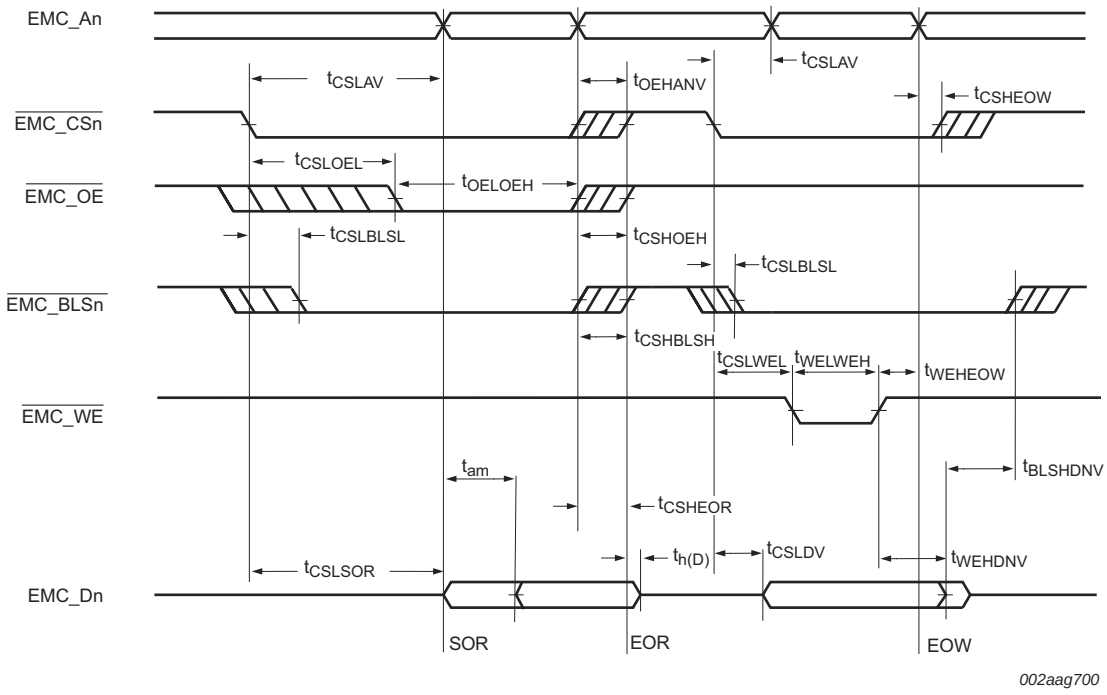


Fig 36. External static memory read/write access (PB = 1)

Table 44. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
12 MHz	< 160 Ω	18 pF, 18 pF
	< 160 Ω	39 pF, 39 pF
16 MHz	< 120 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF
20 MHz	< 100 Ω	18 pF, 18 pF
	< 80 Ω	33 pF, 33 pF

Table 45. Recommended values for $C_{X1/X2}$ in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz	< 80 Ω	18 pF, 18 pF
20 MHz	< 80 Ω	39 pF, 39 pF
	< 100 Ω	47 pF, 47 pF

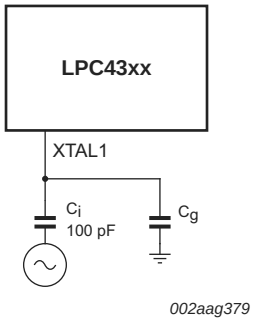


Fig 43. Slave mode operation of the on-chip oscillator

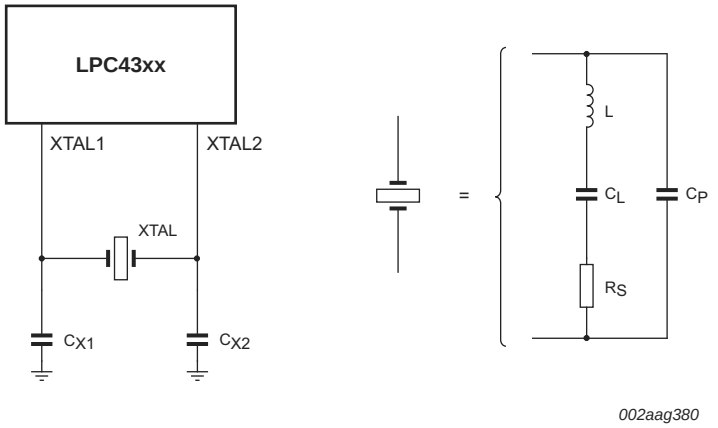
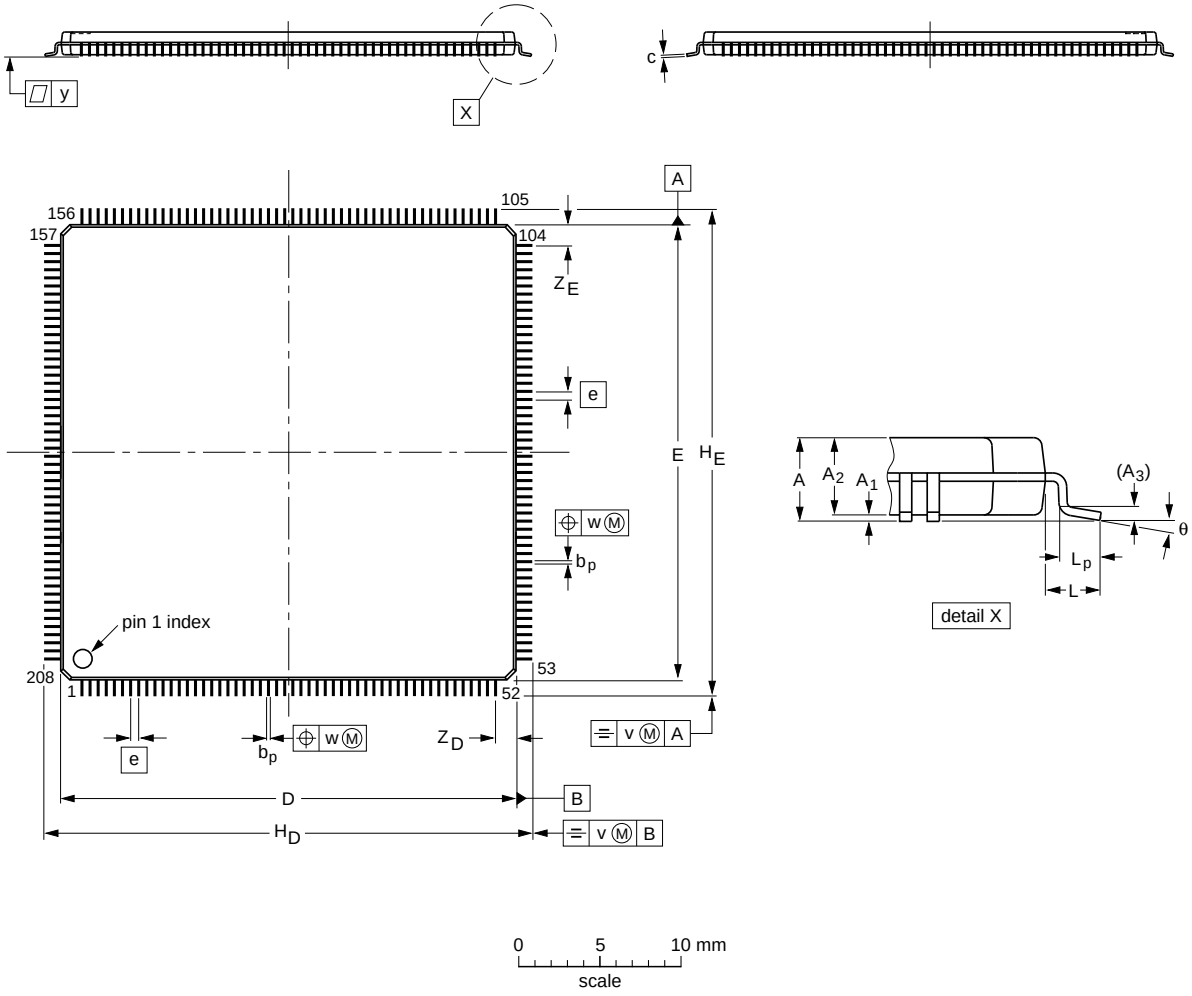


Fig 44. Oscillator modes with external crystal model used for C_{X1}/C_{X2} evaluation

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 52. Package outline of the LQFP208 package

17. References

[1] LPC43xx User manual UM10503:
http://www.nxp.com/documents/user_manual/UM10503.pdf

[2] LPC43xx Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC43XX.pdf

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC4357_53_37_33 v.2	20120711	Preliminary data sheet	-	LPC4357_53 v.1
Modifications:	• Data sheet status changed to preliminary. • Parts LPC4337 and LPC4333 added. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”, “USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Section 10.2 added. • Table 8 “Thermal resistance (LQFP packages)” and Table 9 “Thermal resistance value (BGA packages)” added. • AES removed. Available on parts LPC43Sxx only. • Dynamic characteristics of the SD/MMC controller updated in Table 30. • Dynamic characteristics of the LCD controller updated in Table 31. • Dynamic characteristics of the SSP controller updated in Table 23. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 10.			
LPC4357_53 v.1	20120604	Objective data sheet	-	-