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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	49
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4325jet100e

4.1 Ordering options

Table 2. Ordering options

Type number	Flash total	Flash bank A	Flash bank B	Total SRAM	LCD	Ethernet	USB0 (Host, Device, OTG)	USB1 (Host, Device)/ ULPI interface	Motor control PWM	QEI	ADC channels	Temperature range[1]	GPIO
LPC4357FET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC4357JET256	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC4357JBD208	1 MB	512 kB	512 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC4353FET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	F	164
LPC4353JET256	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	164
LPC4353JBD208	512 kB	256 kB	256 kB	136 kB	yes	yes	yes	yes/yes	yes	yes	8	J	142
LPC4337FET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC4337JET256	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC4337JBD144	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC4337JET100	1 MB	512 kB	512 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC4333FET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	F	164
LPC4333JET256	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	yes	8	J	164
LPC4333JBD144	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/yes	yes	no	8	J	83
LPC4333JET100	512 kB	256 kB	256 kB	136 kB	no	yes	yes	yes/no	no	no	4	J	49
LPC4327JBD144	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4327JET100	1 MB	512 kB	512 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC4325JBD144	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4325JET100	768 kB	384 kB	384 kB	136 kB	no	no	yes	no/no	no	no	4	J	49
LPC4323JBD144	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4323JET100	512 kB	256 kB	256 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC4322JBD144	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	yes	no	8	J	83
LPC4322JET100	512 kB	512 kB	0 kB	104 kB	no	no	yes	no/no	no	no	4	J	49
LPC4317JBD144	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC4317JET100	1 MB	512 kB	512 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC4315JBD144	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	yes	no	8	J	83
LPC4315JET100	768 kB	384 kB	384 kB	136 kB	no	no	no	no/no	no	no	4	J	49
LPC4313JBD144	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC4313JET100	512 kB	256 kB	256 kB	104 kB	no	no	no	no/no	no	no	4	J	49
LPC4312JBD144	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	yes	no	8	J	83
LPC4312JET100	512 kB	512 kB	0 kB	104 kB	no	no	no	no/no	no	no	4	J	49

[1] J = -40 °C to +105 °C; F = -40 °C to +85 °C.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_5	R5	J4	65	48	[2]	N; PU	I/O	**GPIO1[8] —** General purpose digital input/output pin.
							O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_CS0}}$ —** LOW active Chip Select 0 signal.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							I/O	**SGPIO15 —** General purpose digital input/output pin.
							O	**SD_POW —** SD/MMC power monitor output.
P1_6	T4	K4	67	49	[2]	N; PU	I/O	**GPIO1[9] —** General purpose digital input/output pin.
							I	**CTIN_5 —** SCT input 5. Capture input 2 of timer 2.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
							I/O	**SGPIO14 —** General purpose digital input/output pin.
							I/O	**SD_CMD —** SD/MMC command signal.
P1_7	T5	G4	69	50	[2]	N; PU	I/O	**GPIO1[0] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**CTOUT_13 —** SCT output 13. Match output 3 of timer 3.
							I/O	**EMC_D0 —** External memory data line 0.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P2_2	M15	F5	121	84	[2]	N; PU	I/O	**SGPIO6 —** General purpose digital input/output pin.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**EMC_A11 —** External memory address line 11.
							O	**USB0_IND1 —** USB0 port indicator LED control output 1.
							I/O	**GPIO5[2] —** General purpose digital input/output pin.
							I	**CTIN_6 —** SCT input 6. Capture input 1 of timer 3.
							I	**T3_CAP2 —** Capture input 2 of timer 3.
							O	**$\overline{\text{EMC\_CS1}}$ —** LOW active Chip Select 1 signal.
P2_3	J12	D8	127	87	[3]	N; PU	I/O	**SGPIO12 —** General purpose digital input/output pin.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**U3_TXD —** Transmitter output for USART3. See Table 4 for ISP mode.
							I	**CTIN_1 —** SCT input 1. Capture input 1 of timer 0. Capture input 1 of timer 2.
							I/O	**GPIO5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
P2_4	K11	D9	128	88	[3]	N; PU	I/O	**SGPIO13 —** General purpose digital input/output pin.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							I	**U3_RXD —** Receiver input for USART3. See Table 4 for ISP mode.
							I	**CTIN_0 —** SCT input 0. Capture input 0 of timer 0, 1, 2, 3.
							I/O	**GPIO5[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P3_2	F11	G6	166	116	[2]	OL; PU	I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							I/O	**I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**CAN0_TD —** CAN transmitter output.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							I/O	**GPIO5[9] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**LCD_VD14 —** LCD data.
							-	**R —** Function reserved.
P3_3	B14	A7	169	118	[4]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_SCK —** Serial clock for SPI.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**SPIFI_SCK —** Serial clock for SPIFI.
							O	**CGU_OUT1 —** CGU spare clock output 1.
							-	**R —** Function reserved.
							O	**I2S0_TX_MCLK —** I2S transmit master clock.
							I/O	**I2S1_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I²S-bus specification.
P3_4	A15	B8	171	119	[2]	N; PU	I/O	**GPIO1[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO3 —** I/O lane 3 for SPIFI.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							I/O	**I2S1_RX_SDA —** I2S1 Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							O	**LCD_VD13 —** LCD data.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PC_6	H6	-	22	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D2 —** ULPI link bidirectional data line 2.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							I/O	**GPIO6[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							I/O	**SD_DAT2 —** SD/MMC data bus line 2.
PC_7	G5	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D1 —** ULPI link bidirectional data line 1.
							-	**R —** Function reserved.
							I	**ENET_RXD3 —** Ethernet receive data 3 (MII interface).
							I/O	**GPIO6[6] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output 0 of timer 3.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
PC_8	N4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I/O	**USB1_ULPI_D0 —** ULPI link bidirectional data line 0.
							-	**R —** Function reserved.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).
							I/O	**GPIO6[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output 1 of timer 3.
							I	**SD_CD —** SD/MMC card detect input.
PC_9	K2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							I	**USB1_ULPI_NXT —** ULPI link NXT signal. Data flow control signal from the PHY.
							-	**R —** Function reserved.
							I	**ENET_RX_ER —** Ethernet receive error (MII interface).
							I/O	**GPIO6[8] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**SD_POW —** SD/MMC power monitor output.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PD_15	T15	-	101	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A17 —** External memory address line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[29] —** General purpose digital input/output pin.
							I	**SD_WP —** SD/MMC card write protect input.
							O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
							-	**R —** Function reserved.
PD_16	R14	-	104	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A16 —** External memory address line 16.
							-	**R —** Function reserved.
							I/O	**GPIO6[30] —** General purpose digital input/output pin.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
							-	**R —** Function reserved.
PE_0	P14	-	106	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A18 —** External memory address line 18.
							I/O	**GPIO7[0] —** General purpose digital input/output pin.
							O	**CAN1_TD —** CAN1 transmitter output.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_1	N14	-	112	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**EMC_A19 —** External memory address line 19.
							I/O	**GPIO7[1] —** General purpose digital input/output pin.
							I	**CAN1_RD —** CAN1 receiver input.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PF_9	D6	-	203	-	[5]	N; PU	-	**R —** Function reserved.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**GPIO7[23] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I/O	**SGPIO3 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							AI	**ADC1_2 —** ADC1 and ADC0, input channel 2. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_10	A3	-	205	-	[5]	N; PU	-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[24] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**SD_WP —** SD/MMC card write protect input.
							-	**R —** Function reserved.
							AI	**ADC0_5 —** ADC0 and ADC1, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
PF_11	A2	-	207	-	[5]	N; PU	-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**GPIO7[25] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**SD_VOLT2 —** SD/MMC bus voltage select output 2.
							-	**R —** Function reserved.
							AI	**ADC1_5 —** ADC1 and ADC0, input channel 5. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Remark: Any interrupt can wake up the ARM Cortex-M4 from sleep mode if enabled in the NVIC.

7.9 Global Input Multiplexer Array (GIMA)

The GIMA allows to route signals to event-driven peripheral targets like the SCTimer/PWM, timers, event router, or the ADCs.

7.9.1 Features

- Single selection of a source.
- Signal inversion.
- Can capture a pulse if the input event source is faster than the target clock.
- Synchronization of input event and target clock.
- Single-cycle pulse generation for target.

7.10 On-chip static RAM

The LPC435x/3x/2x/1x support up to 136 kB SRAM with separate bus master access for higher throughput and individual power control for low power operation.

7.11 On-chip flash memory

The LPC435x/3x/2x/1x contain up to 1 MB of dual-bank flash program memory. With dual-bank flash memory, the user code can write or erase one flash bank while reading the other flash bank without interruption. A two-port flash accelerator maximizes the flash performance.

In-System Programming (ISP) and In-Application Programming (IAP) routines for programming the flash memory are provided in the Boot ROM.

7.12 EEPROM

The LPC435x/3x/2x/1x contain 16 kB of on-chip byte-erasable and byte-programmable EEPROM memory.

The EEPROM memory is divided into 128 pages. The user can access pages 1 through 127. Page 128 is protected.

7.13 Boot ROM

The internal ROM memory is used to store the boot code of the LPC435x/3x/2x/1x. After a reset, the ARM processor will start its code execution from this memory.

The boot ROM memory includes the following features:

- The ROM memory size is 64 kB.
- Supports booting from external static memory such as NOR flash, SPI flash, quad SPI flash, USB0, and USB1.
- Includes API for OTP programming.
- Includes a flexible USB device stack that supports Human Interface Device (HID), Mass Storage Class (MSC), and Device Firmware Upgrade (DFU) drivers.

Table 6. EMC pinout for different packages

Function	LBGA256	TFBGA100	LQFP208	LQFP144
$\overline{OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$	$\overline{EMC\_OE}$
$\overline{WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$	$\overline{EMC\_WE}$
CKEOUT	EMC_ CKEOUT[3:0]	EMC_ CKEOUT[1:0]	EMC_ CKEOUT[1:0]	EMC_ CKEOUT[1:0]
CLK	EMC_CLK[3:0]; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23	EMC_CLK0, EMC_CLK3; EMC_CLK01, EMC_CLK23
DQMOUT	EMC_ DQMOUT[3:0]	-	EMC_ DQMOUT[1:0]	EMC_ DQMOUT[1:0]
$\overline{DYCS}$	$\overline{EMC\_DYCS[3:0]}$	$\overline{EMC\_DYCS[1:0]}$	$\overline{EMC\_DYCS[2:0]}$	$\overline{EMC\_DYCS[1:0]}$
$\overline{CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$	$\overline{EMC\_CAS}$
$\overline{RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$	$\overline{EMC\_RAS}$

7.18.4.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and NOR flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 24 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable Wait States
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK signals to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. Those are typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- SDRAM clock can run at full or half the Cortex-M4 core frequency.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- DMA transfers supported by GPDMA

7.19.5 I²C-bus interface

Remark: The LPC435x/3x/2x/1x each contain two I²C-bus interfaces.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (for example an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.19.5.1 Features

- I²C0 is a standard I²C compliant bus interface with open-drain pins. I²C0 also supports Fast mode plus with bit rates up to 1 Mbit/s.
- I²C1 uses standard I/O pins with bit rates of up to 400 kbit/s (Fast I²C-bus).
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- All I²C-bus controllers support multiple address recognition and a bus monitor mode.

7.19.6 I²S interface

Remark: The LPC435x/3x/2x/1x each contain two I²S-bus interfaces.

The I²S-bus provides a standard communication interface for digital audio applications.

The *I²S-bus specification* defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S-bus connection has one master, which is always the master, and one slave. The I²S-bus interface provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

Wake-up from sleep mode is caused by an interrupt or event in the core's NVIC. The interrupt is captured in the NVIC and an event is captured in the Event router. Both cores can wake up from sleep mode independently of each other.

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot.

7.23.10 Power control

The LPC435x/3x/2x/1x feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

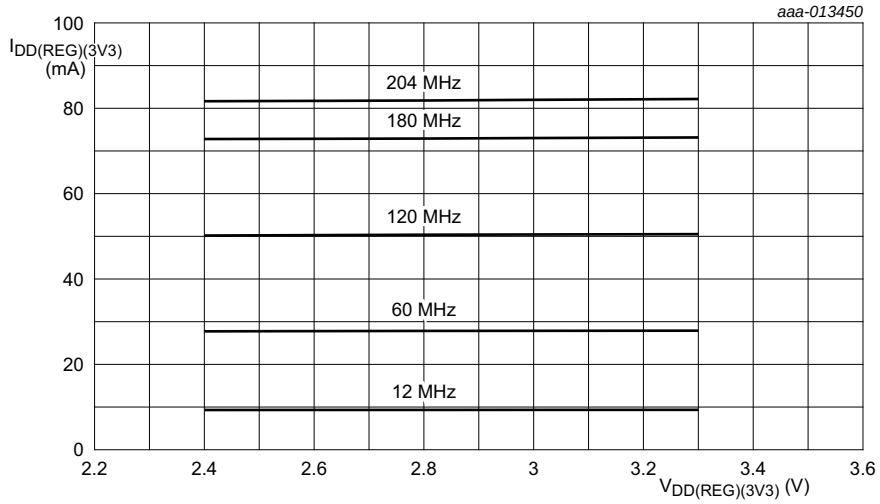
[16] The parameter value specified is a simulated value excluding bond capacitance.

[17] For USB operation 3.0 V ≤ $V_{DD((IO)}$ ≤ 3.6 V. Guaranteed by design.

[18] $V_{DD(IO)}$ present.

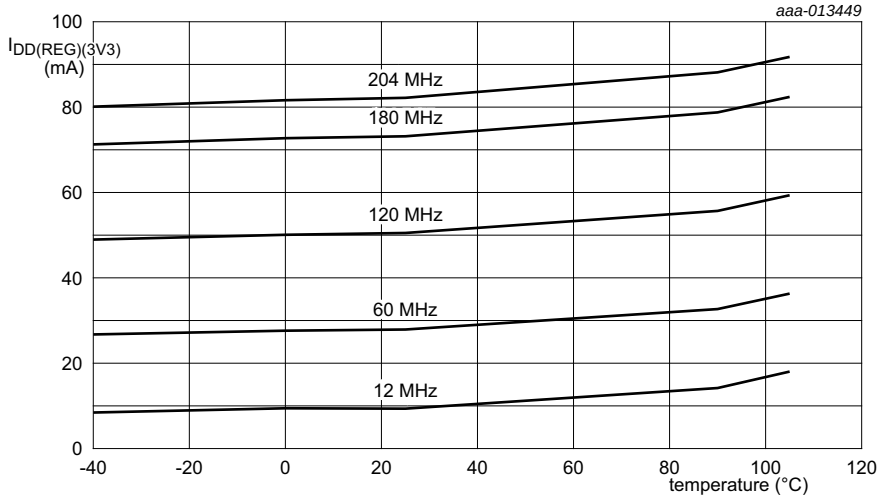
[19] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

10.1 Power consumption



Conditions: T_{amb} = 25 °C; executing code while (1){} from SRAM; M0 core in reset; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 11. Typical supply current versus regulator supply voltage $V_{DD(REEG)(3V3)}$ in active mode



Conditions: $V_{DD(REG)(3V3)}$ = 3.3 V; executing code while (1){} from SRAM; M0 core in reset; system PLL enabled; IRC enabled; all peripherals disabled; all peripheral clocks disabled.

Fig 12. Typical supply current versus temperature in active mode

11.12 SSP interface

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SSP master							
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	$1/(25.5 \times 10^6)$	-	-	s
		when only transmitting		$1/(51 \times 10^6)$	-	-	s
t_{DS}	data set-up time	in SPI mode		12.2	-	-	ns
t_{DH}	data hold time	in SPI mode		−3.6	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode		-	-	6.7	ns
$t_{h(Q)}$	data output hold time	in SPI mode		−1.7	-	-	ns
t_{lead}	lead time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 0; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 0		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
		SPI mode; CPOL = 1; CPHA = 1		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		synchronous serial frame mode		$0.5 \times T_{cy(clk)}$ + 3.3	-	$0.5 \times T_{cy(clk)}$ + 8.2	ns
		microwire frame format		$T_{cy(clk)}$ + 3.3	-	$T_{cy(clk)}$ + 8.2	ns
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		$0.5 \times T_{cy(clk)}$	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$	-	-	ns
		microwire frame format		$0.5 \times T_{cy(clk)}$	-	-	ns

Table 27. Dynamic characteristics: SSP pins in SPI mode

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V; C_L = 20 pF; sampled at 10 % and 90 % of the signal level; EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{lag}	lag time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		0.5 x $T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 0; CPHA = 1		$T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 1; CPHA = 0		0.5 × $T_{cy(clk)}$ + 1.5	-	-	ns
		SPI mode; CPOL = 1; CPHA = 1		$T_{cy(clk)}$ + 1.5	-	-	ns
		synchronous serial frame mode		$T_{cy(clk)}$ + 1.5	-	-	ns
		microwire frame format		0.5 × $T_{cy(clk)}$	-	-	ns
t_d	delay time	continuous transfer mode SPI mode; CPOL = 0; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 0; CPHA = 1		-	n/a	-	ns
		SPI mode; CPOL = 1; CPHA = 0		-	0.5 × $T_{cy(clk)}$	-	ns
		SPI mode; CPOL = 1; CPHA = 1		-	n/a	-	ns
		synchronous serial frame mode		-	$T_{cy(clk)}$	-	ns
		microwire frame format		-	n/a	-	ns

[1] $T_{cy(clk)}$ = (SSPCLKDIV × (1 + SCR) × CPSDVSR) / f_{main}. The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{cy(clk)} \geq 12 \times T_{cy(PCLK)}$.

11.14 SSP/SPI timing diagrams

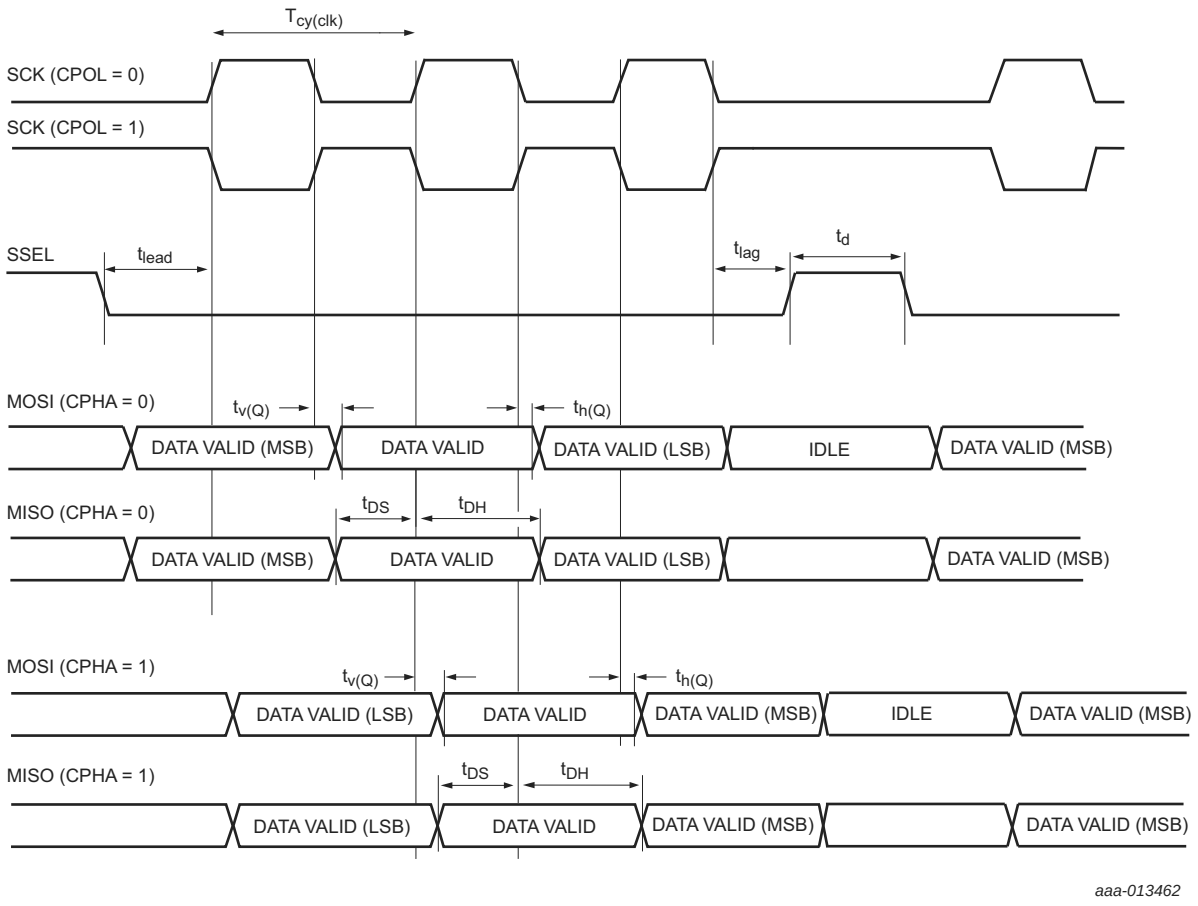


Fig 31. SSP in SPI mode and SPI master timing

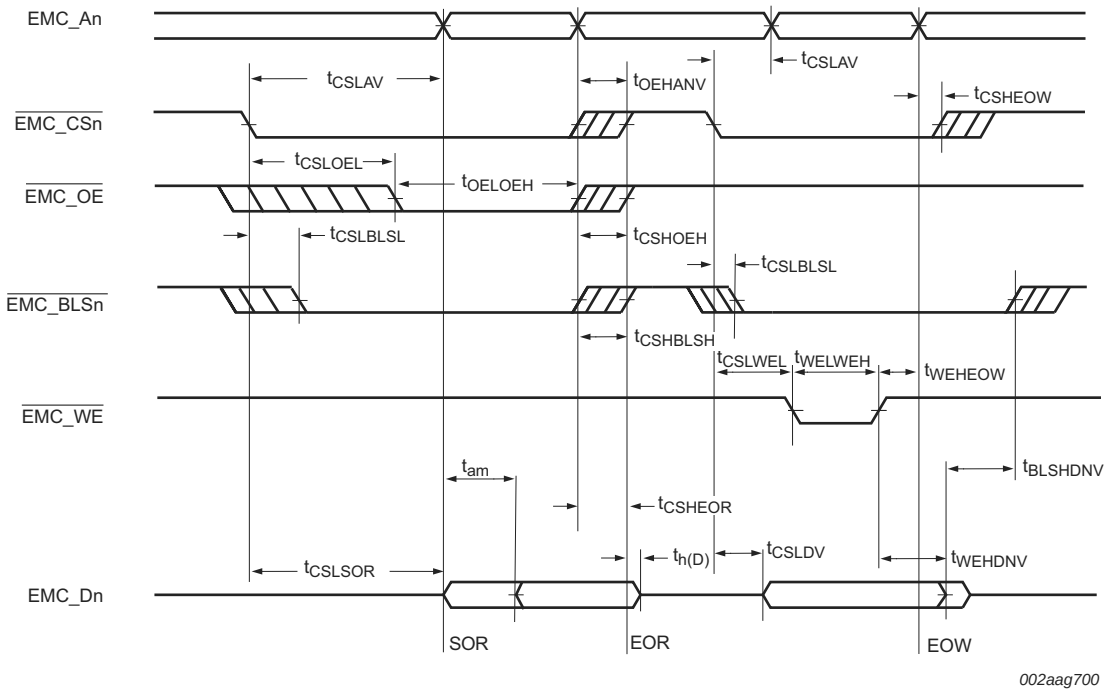


Fig 36. External static memory read/write access (PB = 1)

Table 35. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.19 Ethernet

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

13.3 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{RTCX1} and C_{RTCX2} need to be connected externally. Typical capacitance values for C_{RTCX1} and C_{RTCX2} are $C_{RTCX1/2}$ = 20 (typical) $\pm$ 4 pF.

An external clock can be connected to RTCX1 if RTCX2 is left open. The recommended amplitude of the clock signal is $V_{i(RMS)}$ = 100 mV to 200 mV with a coupling capacitance of 5 pF to 10 pF.

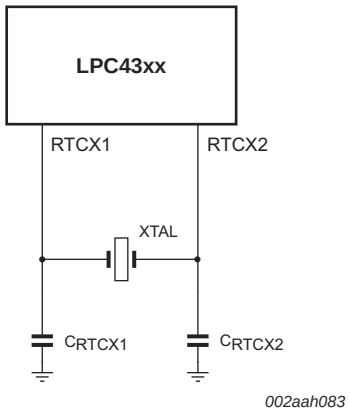


Fig 45. RTC 32 kHz oscillator circuit

13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines

Connect the crystal on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1}, C_{X2}, and C_{X3} in case of third overtone crystal usage have a common ground plane. Also connect the external components to the ground plain. To keep the noise coupled in via the PCB as small as possible, make loops and parasitics as small as possible. Choose smaller values of C_{X1} and C_{X2} if parasitics increase in the PCB layout.

Ensure that no high-speed or high-drive signals are near the RTCX1/2 signals.

13.5 Standard I/O pin configuration

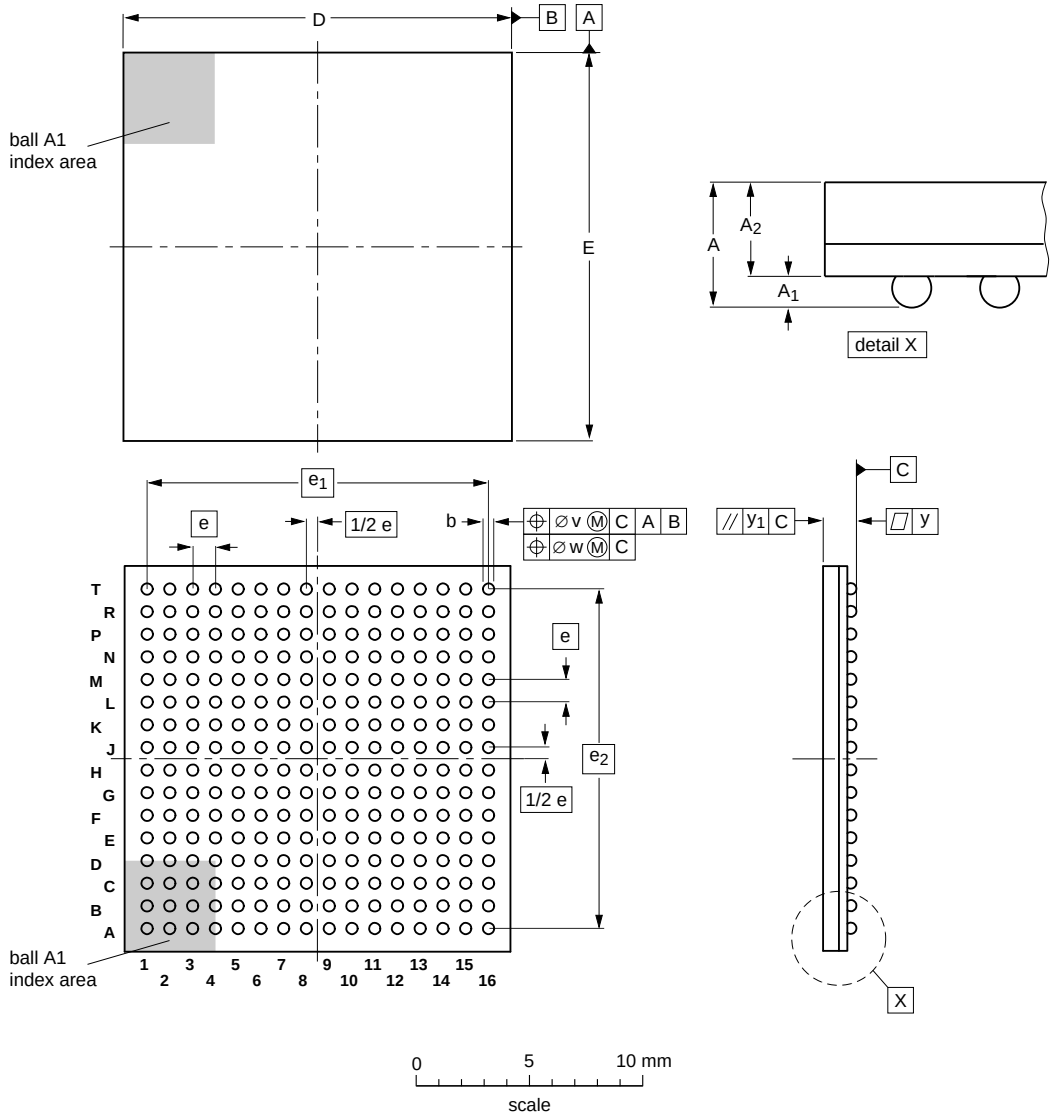
Figure 46 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver enabled/disabled
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input buffer enabled/disabled
- Analog input

The default configuration for standard I/O pins is input buffer disabled and pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

14. Package outline

LBGA256: plastic low profile ball grid array package; 256 balls; body 17 x 17 x 1 mm **SOT740-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.55	0.45 0.35	1.1 0.9	0.55 0.45	17.2 16.8	17.2 16.8	1	15	15	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT740-2	- - -	MO-192	- - -			~~05-06-16~~ 05-08-04

Fig 51. Package outline LBGA256 package

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• SD/MMC timing data updated. See Table 35 “Dynamic characteristics: SD/MMC”. • IEEE standard 802.3 compliance added to Section 11.18. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals. • SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 “SSP in SPI mode and SPI master timing”. • Parameters t_{lead}, t_{lag}, and t_d added in Table 25 “Dynamic characteristics: SSP pins in SPI mode”. • Parameter t_{CSLWEL} with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 29 “Dynamic characteristics: Static asynchronous external memory interface”. • Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 29 “Dynamic characteristics: Static asynchronous external memory interface”. • Removed restriction on C_CAN bus usage. See CAN.1 errata in Ref. 2. • General-purpose OTP size corrected.			
LPC435X_3X_2X_1X v.3	20121206	Preliminary data sheet	-	LPC4357_53_37_33 v.2.1
Modifications:	• TFBGA180 packages removed. • Part LPC432x and LPC431x added. • SCT dither engine added and SCT bi-directional event enable features added. • Figure 10 “Dual-core debug configuration” added. • T = 105 °C data added in Figure 20 to Figure 23. • Change symbol names and parameter names in Table 21. • Parameter I_{LH} updated for condition V_I = 5 V and T_{amb} = 25 °C/105 °C in Table 11. • Power consumption data added in Section 10.1. • SPIFI dynamic characteristics added in Section 11.16. • IRC accuracy corrected to ± 2 % for T_{amb} = -40 °C to 0 °C and T_{amb} = 85 °C to 105 °C. • Pull-up and Pull-down current data (Figure 24 and Figure 25) updated with data for T_{amb} = 105 °C. • SPIFI maximum data rate changed to 52 MB per second. • Recommendation for V_{BAT} use added: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT}$ + 0.2 V. • Table 14 “Band gap characteristics” added. • Section 7.23.9 “Power Management Controller (PMC)” added. • Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. • OTP memory size changed to 64 bit. • Use of C_CAN peripheral restricted in Section 2. • ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.			
LPC4357_53_37_33 v.2.1	20120904	Preliminary data sheet	-	LPC4357_53_37_33 v.2
Modifications:	• SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • SWD removed for ARM Cortex-M0. • BOD de-assertion levels added in Table 13. • Peripheral power consumption data added in Table 12. • Minimum value for all supply voltages changed to -0.5 V in Table 7.			