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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4327jet100e

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_12	R9	K7	78	56	[2]	N; PU	I/O	GPIO1[5] — General purpose digital input/output pin.
							I	U1_DCD — Data Carrier Detect input for UART1.
							-	R — Function reserved.
							I/O	EMC_D5 — External memory data line 5.
							I	T0_CAP1 — Capture input 1 of timer 0.
							-	R — Function reserved.
							I/O	SGPIO8 — General purpose digital input/output pin.
							I/O	SD_DAT3 — SD/MMC data bus line 3.
P1_13	R10	H8	83	60	[2]	N; PU	I/O	GPIO1[6] — General purpose digital input/output pin.
							O	U1_TXD — Transmitter output for UART1.
							-	R — Function reserved.
							I/O	EMC_D6 — External memory data line 6.
							I	T0_CAP0 — Capture input 0 of timer 0.
							-	R — Function reserved.
							I/O	SGPIO9 — General purpose digital input/output pin.
P1_14	R11	J8	85	61	[2]	N; PU	I/O	GPIO1[7] — General purpose digital input/output pin.
							I	U1_RXD — Receiver input for UART1.
							-	R — Function reserved.
							I/O	EMC_D7 — External memory data line 7.
							O	T0_MAT2 — Match output 2 of timer 0.
							-	R — Function reserved.
							I/O	SGPIO10 — General purpose digital input/output pin.
P1_15	T12	K8	87	62	[2]	N; PU	-	R — Function reserved.
							I/O	GPIO0[2] — General purpose digital input/output pin.
							O	U2_TXD — Transmitter output for USART2.
							I/O	SGPIO2 — General purpose digital input/output pin.
							I	ENET_RXD0 — Ethernet receive data 0 (RMII/MII interface).
							O	T0_MAT1 — Match output 1 of timer 0.
							-	R — Function reserved.
							I/O	EMC_D8 — External memory data line 8.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_3	P15	-	113	79	[2]	N; PU	I/O	GPIO3[2] — General purpose digital input/output pin.
							O	USB0_PPWR — VBUS drive signal (towards external charge pump or power management unit); indicates that the VBUS signal must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	SGPIO4 — General purpose digital input/output pin.
							O	EMC_CS1 — LOW active Chip Select 1 signal.
							-	R — Function reserved.
							I	T2_CAP2 — Capture input 2 of timer 2.
							-	R — Function reserved.
							-	R — Function reserved.
P6_4	R16	F6	114	80	[2]	N; PU	I/O	GPIO3[3] — General purpose digital input/output pin.
							I	CTIN_6 — SCT input 6. Capture input 1 of timer 3.
							O	U0_TXD — Transmitter output for USART0.
							O	EMC_CAS — LOW active SDRAM Column Address Strobe.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P6_5	P16	F9	117	82	[2]	N; PU	I/O	GPIO3[4] — General purpose digital input/output pin.
							O	CTOUT_6 — SCT output 6. Match output 2 of timer 1.
							I	U0_RXD — Receiver input for USART0.
							O	EMC_RAS — LOW active SDRAM Row Address Strobe.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P6_6	L14	-	119	83	[2]	N; PU	I/O	GPIO0[5] — General purpose digital input/output pin.
							O	EMC_BLS1 — LOW active Byte Lane select signal 1.
							I/O	SGPIO5 — General purpose digital input/output pin.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	R — Function reserved.
							I	T2_CAP3 — Capture input 3 of timer 2.
							-	R — Function reserved.
							-	R — Function reserved.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P7_2	A16	-	165	115	[2]	N; PU	I/O	GPIO3[10] — General purpose digital input/output pin.
							I	CTIN_4 — SCT input 4. Capture input 2 of timer 1.
							I/O	I2S0_TX_SDA — I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the I ² S-bus specification.
							O	LCD_VD18 — LCD data.
							O	LCD_VD6 — LCD data.
							-	R — Function reserved.
							I	U2_RXD — Receiver input for USART2.
							I/O	SGPIO6 — General purpose digital input/output pin.
P7_3	C13	-	167	117	[2]	N; PU	I/O	GPIO3[11] — General purpose digital input/output pin.
							I	CTIN_3 — SCT input 3. Capture input 1 of timer 1.
							-	R — Function reserved.
							O	LCD_VD17 — LCD data.
							O	LCD_VD5 — LCD data.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
P7_4	C8	-	189	132	[5]	N; PU	I/O	GPIO3[12] — General purpose digital input/output pin.
							O	CTOUT_13 — SCT output 13. Match output 3 of timer 3.
							-	R — Function reserved.
							O	LCD_VD16 — LCD data.
							O	LCD_VD4 — LCD data.
							O	TRACEDATA[0] — Trace data, bit 0.
							-	R — Function reserved.
							-	R — Function reserved.
P7_5	A7	-	191	133	[5]	N; PU	AI	ADC0_4 — ADC0 and ADC1, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							I/O	GPIO3[13] — General purpose digital input/output pin.
							O	CTOUT_12 — SCT output 12. Match output 3 of timer 3.
							-	R — Function reserved.
							O	LCD_VD8 — LCD data.
							O	LCD_VD23 — LCD data.
							O	TRACEDATA[1] — Trace data, bit 1.
							-	R — Function reserved.
P7_5	A7	-	191	133	[5]	N; PU	-	R — Function reserved.
							AI	ADC0_3 — ADC0 and ADC1, input channel 3. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P7_6	C7	-	194	134	[2]	N; PU	I/O	GPIO3[14] — General purpose digital input/output pin.
							O	CTOUT_11 — SCT output 1. Match output 3 of timer 2.
							-	R — Function reserved.
							O	LCD_LP — Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							-	R — Function reserved.
							O	TRACEDATA[2] — Trace data, bit 2.
							-	R — Function reserved.
							-	R — Function reserved.
P7_7	B6	-	201	140	[5]	N; PU	I/O	GPIO3[15] — General purpose digital input/output pin.
							O	CTOUT_8 — SCT output 8. Match output 0 of timer 2.
							-	R — Function reserved.
							O	LCD_PWR — LCD panel power enable.
							-	R — Function reserved.
							O	TRACEDATA[3] — Trace data, bit 3.
							O	ENET_MDC — Ethernet MIIM clock.
							I/O	SGPIO7 — General purpose digital input/output pin.
P8_0	E5	-	2	-	[3]	N; PU	AI	ADC1_6 — ADC1 and ADC0, input channel 6. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.
							I/O	GPIO4[0] — General purpose digital input/output pin.
							I	USB0_PWR_FAULT — Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							-	R — Function reserved.
							I	MC12 — Motor control PWM channel 2, input.
							I/O	SGPIO8 — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
P8_1	H5	-	34	-	[3]	N; PU	O	T0_MAT0 — Match output 0 of timer 0.
							I/O	GPIO4[1] — General purpose digital input/output pin.
							O	USB0_IND1 — USB0 port indicator LED control output 1.
							-	R — Function reserved.
							I	MC11 — Motor control PWM channel 1, input.
							I/O	SGPIO9 — General purpose digital input/output pin.
							-	R — Function reserved.
							-	R — Function reserved.
P8_1	H5	-	34	-	[3]	N; PU	O	T0_MAT1 — Match output 1 of timer 0.

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PC_6	H6	-	22	-	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D2 — ULPI link bidirectional data line 2.
							-	R — Function reserved.
							I	ENET_RXD2 — Ethernet receive data 2 (MII interface).
							I/O	GPIO6[5] — General purpose digital input/output pin.
							-	R — Function reserved.
							I	T3_CAP3 — Capture input 3 of timer 3.
I/O	SD_DAT2 — SD/MMC data bus line 2.							
PC_7	G5	-	-	-	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D1 — ULPI link bidirectional data line 1.
							-	R — Function reserved.
							I	ENET_RXD3 — Ethernet receive data 3 (MII interface).
							I/O	GPIO6[6] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT0 — Match output 0 of timer 3.
I/O	SD_DAT3 — SD/MMC data bus line 3.							
PC_8	N4	-	-	-	[2]	N; PU	-	R — Function reserved.
							I/O	USB1_ULPI_D0 — ULPI link bidirectional data line 0.
							-	R — Function reserved.
							I	ENET_RX_DV — Ethernet Receive Data Valid (RMII/MII interface).
							I/O	GPIO6[7] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT1 — Match output 1 of timer 3.
I	SD_CD — SD/MMC card detect input.							
PC_9	K2	-	-	-	[2]	N; PU	-	R — Function reserved.
							I	USB1_ULPI_NXT — ULPI link NXT signal. Data flow control signal from the PHY.
							-	R — Function reserved.
							I	ENET_RX_ER — Ethernet receive error (MII interface).
							I/O	GPIO6[8] — General purpose digital input/output pin.
							-	R — Function reserved.
							O	T3_MAT2 — Match output 2 of timer 3.
O	SD_POW — SD/MMC power monitor output.							

Table 3. Pin description ...continued

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PF_2	D11	-	168	-	[2]	N; PU	-	R — Function reserved.
							O	U3_TXD — Transmitter output for USART3.
							I/O	SSP0_MISO — Master In Slave Out for SSP0.
							-	R — Function reserved.
							I/O	GPIO7[17] — General purpose digital input/output pin.
							-	R — Function reserved.
							I/O	SGPIO1 — General purpose digital input/output pin.
							-	R — Function reserved.
PF_3	E10	-	170	-	[2]	N; PU	-	R — Function reserved.
							I	U3_RXD — Receiver input for USART3.
							I/O	SSP0_MOSI — Master Out Slave in for SSP0.
							-	R — Function reserved.
							I/O	GPIO7[18] — General purpose digital input/output pin.
							-	R — Function reserved.
							I/O	SGPIO2 — General purpose digital input/output pin.
PF_4	D10	H4	172	120	[2]	O; PU	I/O	SSP1_SCK — Serial clock for SSP1.
							I	GP_CLKIN — General purpose clock input to the CGU.
							O	TRACECLK — Trace clock.
							-	R — Function reserved.
							-	R — Function reserved.
							-	R — Function reserved.
							O	I2S0_TX_MCLK — I2S transmit master clock.
							I/O	I2S0_RX_SCK — I2S receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the I ² S-bus specification.
PF_5	E9	-	190	-	[5]	N; PU	-	R — Function reserved.
							I/O	U3_UCLK — Serial clock input/output for USART3 in synchronous mode.
							I/O	SSP1_SSEL — Slave Select for SSP1.
							O	TRACEDATA[0] — Trace data, bit 0.
							I/O	GPIO7[19] — General purpose digital input/output pin.
							-	R — Function reserved.
							I/O	SGPIO4 — General purpose digital input/output pin.
							-	R — Function reserved.
PF_5	E9	-	190	-	[5]	N; PU	AI	ADC1_4 — ADC1 and ADC0, input channel 4. Configure the pin as GPIO input and use the ADC function select register in the SCU to select the ADC.

Table 3. Pin description ...continued

Pin name	LPGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
WAKEUP0	A9	A4	187	130	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 0 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP1	A10	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 1 of the event monitor. No internal pull-up is enabled when this pin is configured as input.
WAKEUP2	C9	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. Input 2 of the event monitor. This pin does not have an internal pull-up.
WAKEUP3	D8	-	-	-	[11]	I; IA	I	External wake-up input; can raise an interrupt and can cause wake-up from any of the low power modes. A pulse with a duration of at least 45 ns wakes up the part. This pin does not have an internal pull-up.
ADC pins								
ADC0_0/ ADC1_0/DAC	E3	A2	8	6	[8]	I; IA	I	ADC input channel 0. Shared between 10-bit ADC0/1 and DAC.
ADC0_1/ ADC1_1	C3	A1	4	2	[8]	I; IA	I	ADC input channel 1. Shared between 10-bit ADC0/1.
ADC0_2/ ADC1_2	A4	B3	206	143	[8]	I; IA	I	ADC input channel 2. Shared between 10-bit ADC0/1.
ADC0_3/ ADC1_3	B5	A3	200	139	[8]	I; IA	I	ADC input channel 3. Shared between 10-bit ADC0/1.
ADC0_4/ ADC1_4	C6	-	199	138	[8]	I; IA	I	ADC input channel 4. Shared between 10-bit ADC0/1.
ADC0_5/ ADC1_5	B3	-	208	144	[8]	I; IA	I	ADC input channel 5. Shared between 10-bit ADC0/1.
ADC0_6/ ADC1_6	A5	-	204	142	[8]	I; IA	I	ADC input channel 6. Shared between 10-bit ADC0/1.
ADC0_7/ ADC1_7	C5	-	197	136	[8]	I; IA	I	ADC input channel 7. Shared between 10-bit ADC0/1.
RTC								
RTC_ALARM	A11	C3	186	129	[11]	-	O	RTC controlled output.
RTCX1	A8	A5	182	125	[8]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	B8	B5	183	126	[8]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
SAMPLE	B9	-	-	-	[11]	O	O	Event monitor sample output.
Crystal oscillator pins								

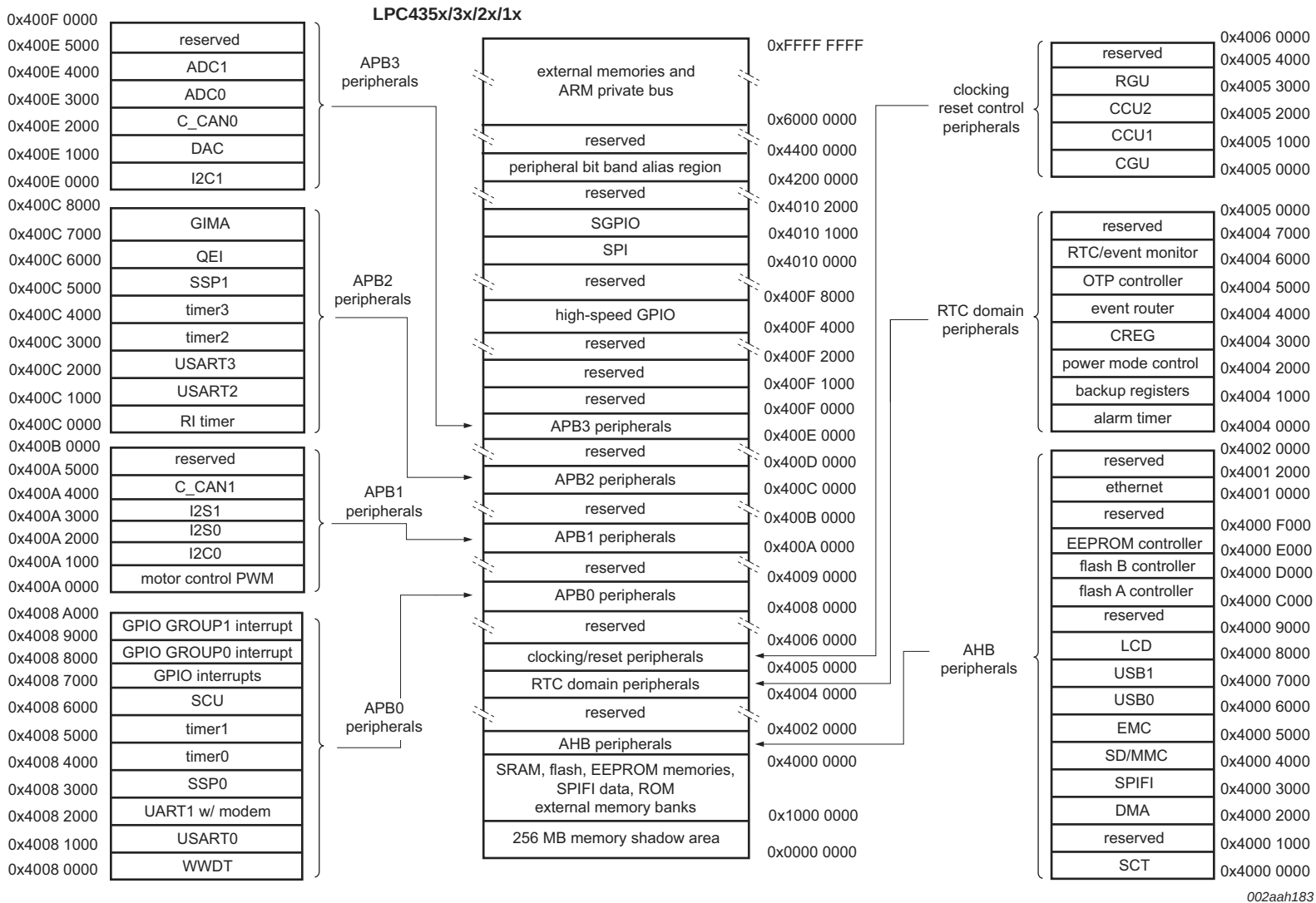


Fig 8. LPC435x/3x/2x/1x Memory mapping (peripherals)

- Each slice has a 32-bit pattern match filter.

7.18 AHB peripherals

7.18.1 General Purpose DMA

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.18.1.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.18.2 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.

7.18.5 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on the following parts: LPC435x, LPC433x, LPC432x. USB0 is not available on the LPC431x parts.

The USB OTG module allows the LPC435x/3x/2x/1x to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.18.5.1 Features

- Contains UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.6 High-speed USB Host/Device interface with ULPI (USB1)

Remark: USB1 is available on the following parts: LPC435x and LPC433x. USB1 is not available on the LPC432x and LPC431x parts.

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.18.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.7 LCD controller

Remark: The LCD controller is only available on parts LPC435x. LCD is not available on parts LPC433x, LPC432x, and LPC431x.

7.23.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μ S.

7.23.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC435x/3x/2x/1x.

7.23.9 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC435x/3x/2x/1x support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
 - a. Deep-sleep mode
 - b. Power-down mode
 - c. Deep power-down mode

Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

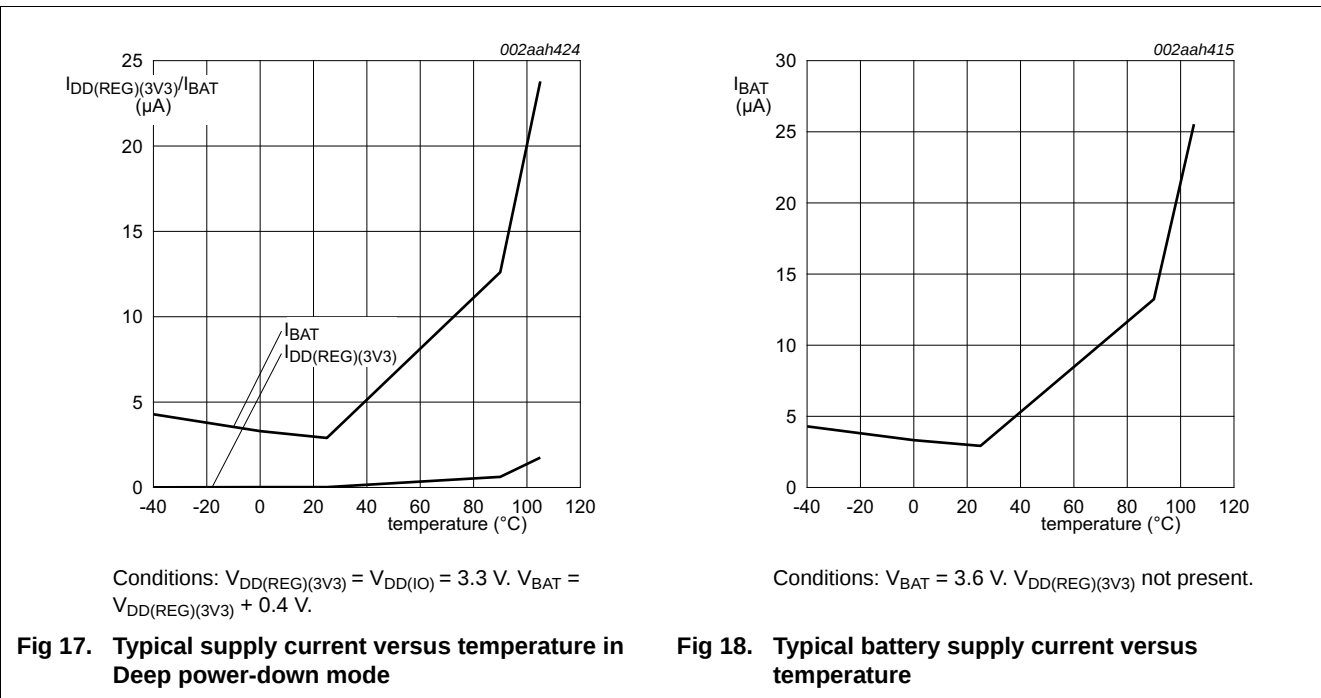
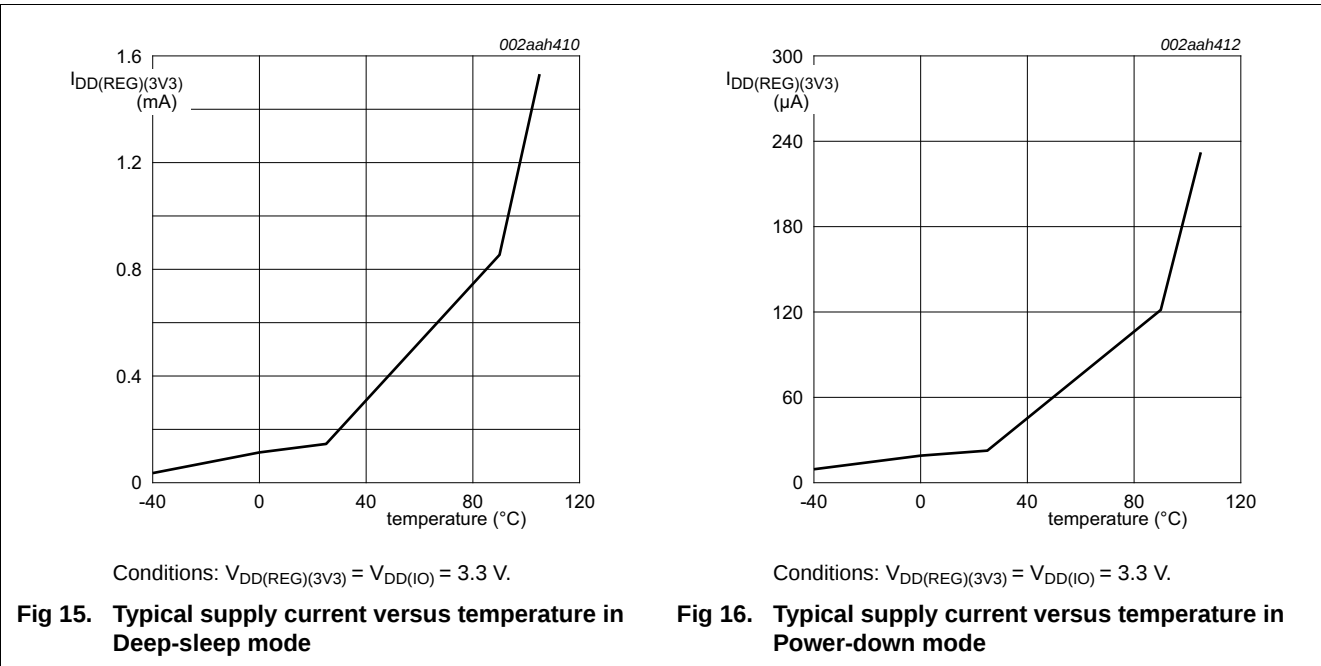
Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

Table 11. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ ^[1]	Max	Unit
V_O	output voltage	output active		0	-	$V_{DD(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(I/O)}$	-	5.5	V
V_{IL}	LOW-level input voltage			-0.5	-	$0.3 \times V_{DD(I/O)}$	V
V_{hys}	hysteresis voltage			$0.1 \times V_{DD(I/O)}$	-	-	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -6\text{ mA}$		$V_{DD(I/O)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 6\text{ mA}$		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(I/O)} - 0.4\text{ V}$		-6	-	-	mA
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$		6	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86.5	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(I/O)}$	[11]	-	-	76.5	mA
I_{pd}	pull-down current	$V_I = 5\text{ V}$	[13] [14] [15]	-	93	-	μA
I_{pu}	pull-up current	$V_I = 0\text{ V}$	[13] [14] [15]	-	-62	-	μA
		$V_{DD(I/O)} < V_I \leq 5\text{ V}$		-	10	-	μA
R_s	series resistance	on I/O pins with analog function; analog function enabled			200		Ω
I/O pins - high drive strength							
C_i	input capacitance			-	-	5.2	pF
I_{LL}	LOW-level leakage current	$V_I = 0\text{ V}$; on-chip pull-up resistor disabled		-	3	-	nA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$ to $V_{DD(I/O)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(I/O)} \geq 2.4\text{ V}$		0	-	5.5	V
		$V_{DD(I/O)} = 0\text{ V}$		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.7 \times V_{DD(I/O)}$	-	5.5	V
V_{IL}	LOW-level input voltage			-0.5	-	$0.3 \times V_{DD(I/O)}$	V



11.15 SPIFI

Table 29. Dynamic characteristics: SPIFI

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$; $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$; $2.7\text{ V} \leq V_{DD(IO)} \leq 3.6\text{ V}$. $C_L = 20\text{ pF}$. Sampled at 90 % and 10 % of the signal level. EHS = 1 for all pins. Simulated values.

Symbol	Parameter	Min	Max	Unit
$T_{cy(clk)}$	clock cycle time	9.6	-	ns
t_{DS}	data set-up time	3.2	-	ns
t_{DH}	data hold time	0	-	ns
$t_{v(Q)}$	data output valid time	-	3.2	ns
$t_{h(Q)}$	data output hold time	0.6	-	ns

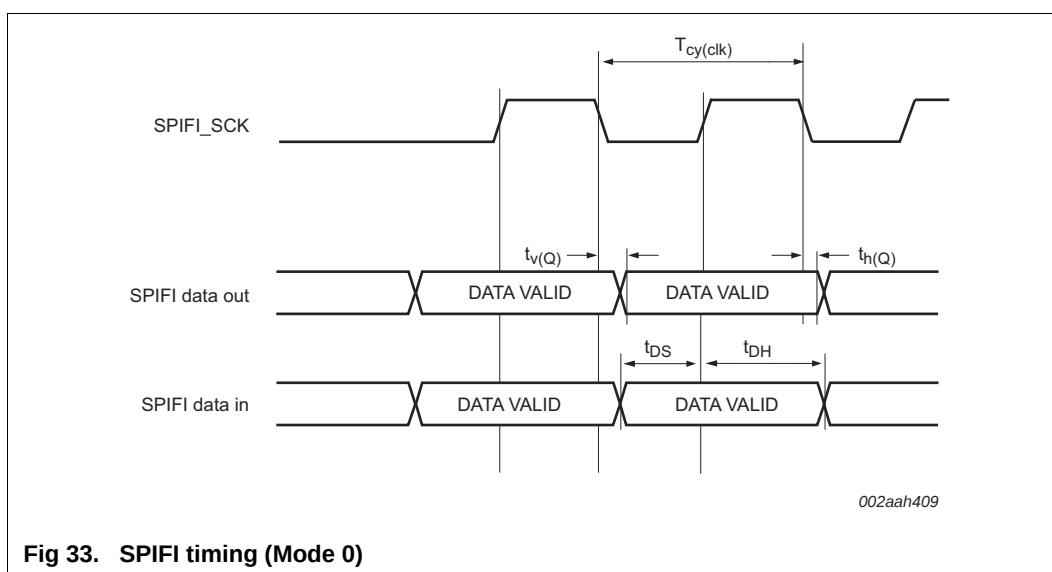


Fig 33. SPIFI timing (Mode 0)

11.16 SGPIO timing

The following considerations apply to SGPIO timing:

- SGPIO input signals are synchronized by the internal clock SGPIO_CLOCK. To guarantee that no samples are missed, all input signals should have a duration of at least one SGPIO_CLOCK cycle plus the set-up and hold times.
- When an external clock input is used to generate output data, synchronization causes a latency of at least one SGPIO_CLOCK cycle. The maximum output data rate is one output every two SGPIO_CLOCK cycles.
- Synchronization also causes a latency of one SGPIO_CLOCK cycle when sampling several inputs. This may cause inputs with very similar timings to be sampled with a difference of one SGPIO_CLOCK cycle.

Table 30. Dynamic characteristics: SGPIO

$T_{amb} = -40\text{ }^{\circ}\text{C to } +105\text{ }^{\circ}\text{C}$; $2.4\text{ V} \leq V_{DD(REG)(3V3)} \leq 3.6\text{ V}$; $2.7\text{ V} \leq V_{DD(IO)} \leq 3.6\text{ V}$. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D)}$	data input set-up time			2	-	-	ns
$t_{h(D)}$	data input hold time		[1]	$T_{SGPIO} + 2$	-	-	ns
$t_{su(D)}$	data input set-up time	sampled by SGPIO_CLOCK	[1]	$T_{SGPIO} + 2$	-	-	ns
$t_{h(D)}$	data input hold time	sampled by SGPIO_CLOCK	[1]	$T_{SGPIO} + 2$	-	-	ns
$t_{v(Q)}$	data output valid time		[1]	-	-	$2 \times T_{SGPIO}$	ns
$t_{h(Q)}$	data output hold time		[1]	T_{SGPIO}	-	-	ns
$t_{v(Q)}$	data output valid time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns
$t_{h(Q)}$	data output hold time	sampled by SGPIO_CLOCK	[1]	-3	-	3	ns

[1] SGPIO_CLOCK is the internally generated SGPIO clock. $T_{SGPIO} = 1/f_{SGPIO_CLOCK}$.

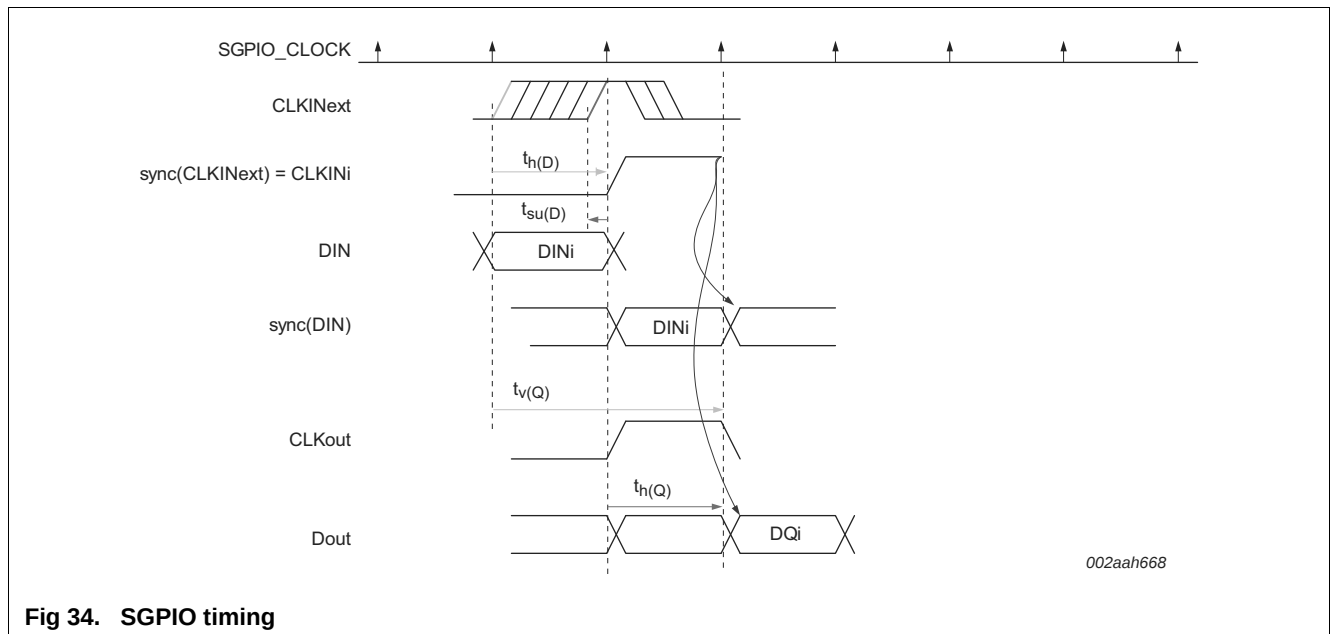


Fig 34. SGPIO timing

Table 42. LCD panel connections for STN dual panel mode

External pin	4-bit mono STN dual panel		8-bit mono STN dual panel		Color STN dual panel	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD2	P4_3	UD[2]	P4_3	UD[2]	P4_3	UD[2]
LCD_VD1	P4_4	UD[1]	P4_4	UD[1]	P4_4	UD[1]
LCD_VD0	P4_1	UD[0]	P4_1	UD[0]	P4_1	UD[0]
LCD_LP	P7_6	LCDLP	P7_6	LCDLP	P7_6	LCDLP
LCD_ENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM	P4_6	LCDENAB/ LCDM
LCD_FP	P4_5	LCDFP	P4_5	LCDFP	P4_5	LCDFP
LCD_DCLK	P4_7	LCDDCLK	P4_7	LCDDCLK	P4_7	LCDDCLK
LCD_LE	P7_0	LCDLE	P7_0	LCDLE	P7_0	LCDLE
LCD_PWR	P7_7	LCDPWR	P7_7	LCDPWR	P7_7	LCDPWR
GP_CLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN	PF_4	LCDCLKIN

Table 43. LCD panel connections for TFT panels

External pin	TFT 12 bit (4:4:4 mode)		TFT 16 bit (5:6:5 mode)		TFT 16 bit (1:5:5:5 mode)		TFT 24 bit	
	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function	LPC43xx pin used	LCD function
LCD_VD23	PB_0	BLUE3	PB_0	BLUE4	PB_0	BLUE4	PB_0	BLUE7
LCD_VD22	PB_1	BLUE2	PB_1	BLUE3	PB_1	BLUE3	PB_1	BLUE6
LCD_VD21	PB_2	BLUE1	PB_2	BLUE2	PB_2	BLUE2	PB_2	BLUE5
LCD_VD20	PB_3	BLUE0	PB_3	BLUE1	PB_3	BLUE1	PB_3	BLUE4
LCD_VD19	-	-	P7_1	BLUE0	P7_1	BLUE0	P7_1	BLUE3
LCD_VD18	-	-	-	-	P7_2	intensity	P7_2	BLUE2
LCD_VD17	-	-	-	-	-	-	P7_3	BLUE1
LCD_VD16	-	-	-	-	-	-	P7_4	BLUE0
LCD_VD15	PB_4	GREEN3	PB_4	GREEN5	PB_4	GREEN4	PB_4	GREEN7
LCD_VD14	PB_5	GREEN2	PB_5	GREEN4	PB_5	GREEN3	PB_5	GREEN6
LCD_VD13	PB_6	GREEN1	PB_6	GREEN3	PB_6	GREEN2	PB_6	GREEN5
LCD_VD12	P8_3	GREEN0	P8_3	GREEN2	P8_3	GREEN1	P8_3	GREEN4
LCD_VD11	-	-	P4_9	GREEN1	P4_9	GREEN0	P4_9	GREEN3
LCD_VD10	-	-	P4_10	GREEN0	P4_10	intensity	P4_10	GREEN2
LCD_VD9	-	-	-	-	-	-	P4_8	GREEN1
LCD_VD8	-	-	-	-	-	-	P7_5	GREEN0
LCD_VD7	P8_4	RED3	P8_4	RED4	P8_4	RED4	P8_4	RED7
LCD_VD6	P8_5	RED2	P8_5	RED3	P8_5	RED3	P8_5	RED6
LCD_VD5	P8_6	RED1	P8_6	RED2	P8_6	RED2	P8_6	RED5
LCD_VD4	P8_7	RED0	P8_7	RED1	P8_7	RED1	P8_7	RED4
LCD_VD3	-	-	P4_2	RED0	P4_2	RED0	P4_2	RED3
LCD_VD2	-	-	-	-	P4_3	intensity	P4_3	RED2
LCD_VD1	-	-	-	-	-	-	P4_4	RED1

Table 47. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	- SD/MMC timing data updated. See Table 35 "Dynamic characteristics: SD/MMC". - IEEE standard 802.3 compliance added to Section 11.18. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals. - SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 "SSP in SPI mode and SPI master timing". - Parameters t_{lead}, t_{lag}, and t_d added in Table 25 "Dynamic characteristics: SSP pins in SPI mode". - Parameter t_{CSLWEL} with condition $PB = 1$ corrected: $(WAITWEN + 1) \times T_{cy(clk)}$ added. See Table 29 "Dynamic characteristics: Static asynchronous external memory interface". - Parameter $t_{CSLBLSL}$ with condition $PB = 0$ corrected: $(WAITWEN + 1) \times T_{cy(clk)}$ added. See Table 29 "Dynamic characteristics: Static asynchronous external memory interface". - Removed restriction on C_CAN bus usage. See CAN.1 errata in Ref. 2. - General-purpose OTP size corrected.			
LPC435X_3X_2X_1X v.3	20121206	Preliminary data sheet	-	LPC4357_53_37_33 v.2.1
Modifications:	- TFBGA180 packages removed. - Part LPC432x and LPC431x added. - SCT dither engine added and SCT bi-directional event enable features added. - Figure 10 "Dual-core debug configuration" added. $T = 105^\circ\text{C}$ data added in Figure 20 to Figure 23. - Change symbol names and parameter names in Table 21. - Parameter I_{LH} updated for condition $V_I = 5\text{ V}$ and $T_{amb} = 25^\circ\text{C}/105^\circ\text{C}$ in Table 11. - Power consumption data added in Section 10.1. - SPIFI dynamic characteristics added in Section 11.16. - IRC accuracy corrected to $\pm 2\%$ for $T_{amb} = -40^\circ\text{C}$ to 0°C and $T_{amb} = 85^\circ\text{C}$ to 105°C. - Pull-up and Pull-down current data (Figure 24 and Figure 25) updated with data for $T_{amb} = 105^\circ\text{C}$. - SPIFI maximum data rate changed to 52 MB per second. - Recommendation for V_{BAT} use added: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2\text{ V}$. - Table 14 "Band gap characteristics" added. - Section 7.23.9 "Power Management Controller (PMC)" added. - Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. - OTP memory size changed to 64 bit. - Use of C_CAN peripheral restricted in Section 2. - ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.			
LPC4357_53_37_33 v.2.1	20120904	Preliminary data sheet	-	LPC4357_53_37_33 v.2
Modifications:	- SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. - SWD removed for ARM Cortex-M0. - BOD de-assertion levels added in Table 13. - Peripheral power consumption data added in Table 12. - Minimum value for all supply voltages changed to -0.5 V in Table 7.			

Table 47. Revision history ...continued

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC4357_53_37_33 v.2	20120711	Preliminary data sheet	-	LPC4357_53 v.1
Modifications:	• Data sheet status changed to preliminary. • Parts LPC4337 and LPC4333 added. • Minimum value of V_I for conditions "USB0 pins USB0_DP; USB0_DM; USB0_VBUS", "USB0 pins USB0_ID; USB0_RREF", and "USB1 pins USB1_DP and USB1_DM" changed to -0.3 V in Table 6. • Section 10.2 added. • Table 8 "Thermal resistance (LQFP packages)" and Table 9 "Thermal resistance value (BGA packages)" added. • AES removed. Available on parts LPC43Sxx only. • Dynamic characteristics of the SD/MMC controller updated in Table 30. • Dynamic characteristics of the LCD controller updated in Table 31. • Dynamic characteristics of the SSP controller updated in Table 23. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 10.			
LPC4357_53 v.1	20120604	Objective data sheet	-	-

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