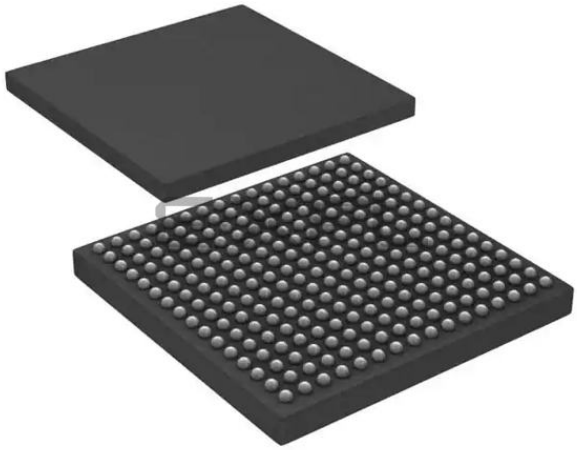

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Applications of "Embedded - Microcontrollers"

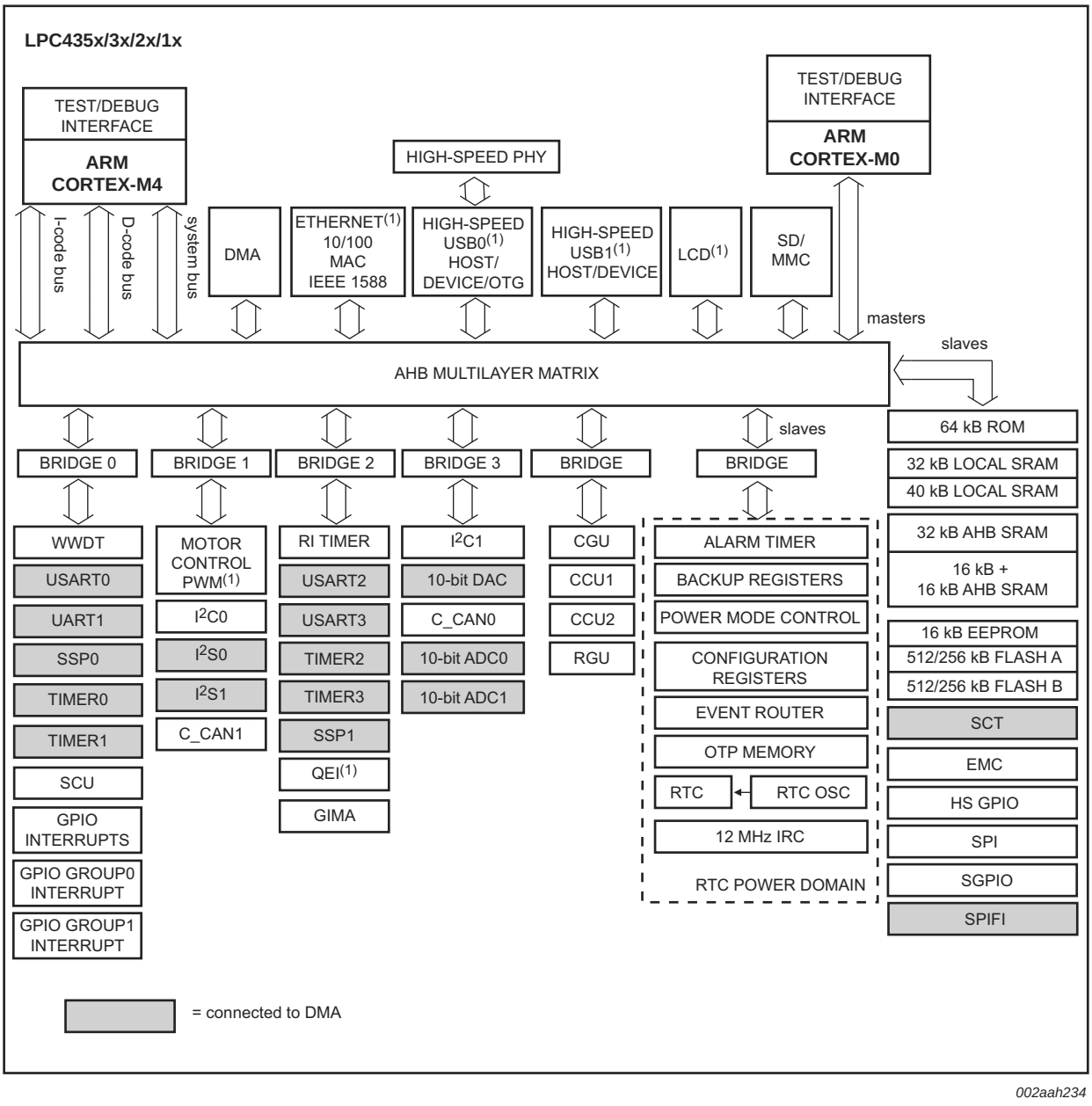
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, QEI, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	164
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-LBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4333jet256-551

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC4357FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4357JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4357JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4353FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4353JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4353JBD208	LQFP208	Plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC4337FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4337JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4337JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4337JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4333FET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4333JET256	LBGA256	Plastic low profile ball grid array package; 256 balls; body 17 × 17 × 1 mm	SOT740-2
LPC4333JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4333JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4327JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4327JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4325JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4325JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4323JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4323JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4322JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4322JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4317JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4317JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4315JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4315JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4313JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4313JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC4312JBD144	LQFP144	Plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC4312JET100	TFBGA100	Plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1

5. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. LPC435x/3x/2x/1x Block diagram

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_12	R9	K7	78	56	[2]	N; PU	I/O	**GPIO1[5] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D5 —** External memory data line 5.
							I	**T0_CAP1 —** Capture input 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
							I/O	**SD_DAT3 —** SD/MMC data bus line 3.
P1_13	R10	H8	83	60	[2]	N; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D6 —** External memory data line 6.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
							I	**SD_CD —** SD/MMC card detect input.
P1_14	R11	J8	85	61	[2]	N; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D7 —** External memory data line 7.
							O	**T0_MAT2 —** Match output 2 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO10 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
P1_15	T12	K8	87	62	[2]	N; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**SGPIO2 —** General purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1 —** Match output 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P2_5	K14	D10	131	91	[3]	N; PU	I/O	**SGPIO14 —** General purpose digital input/output pin.
							I	**CTIN_2 —** SCT input 2. Capture input 2 of timer 0.
							I	**USB1_VBUS —** Monitors the presence of USB1 bus power. **Note:** This signal must be HIGH for USB reset to occur.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**GPIO5[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output 2 of timer 3.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
P2_6	K16	G9	137	95	[2]	N; PU	I/O	**SGPIO7 —** General purpose digital input/output pin.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**EMC_A10 —** External memory address line 10.
							O	**USB0_IND0 —** USB0 port indicator LED control output 0.
							I/O	**GPIO5[6] —** General purpose digital input/output pin.
							I	**CTIN_7 —** SCT input 7.
							I	**T3_CAP3 —** Capture input 3 of timer 3.
							O	**EMC_BLS1 —** LOW active Byte Lane select signal 1.
P2_7	H14	C10	138	96	[2]	N; PU	I/O	**GPIO0[7] —** General purpose digital input/output pin. If this pin is pulled LOW at reset, the part enters ISP mode or boots from an external source (see Table 4 and Table 5).
							O	**CTOUT_1 —** SCT output 1. Match output 3 of timer 3.
							I/O	**U3_UCLK —** Serial clock input/output for USART3 in synchronous mode.
							I/O	**EMC_A9 —** External memory address line 9.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output 3 of timer 3.
							-	**R —** Function reserved.
P2_8	J16	C6	140	98	[2]	N; PU	I/O	**SGPIO15 —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_0 —** SCT output 0. Match output 0 of timer 0.
							I/O	**U3_DIR —** RS-485/EIA-485 output enable/direction control for USART3.
							I/O	**EMC_A8 —** External memory address line 8.
							I/O	**GPIO5[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P3_5	C12	B7	173	121	[2]	N; PU	I/O	**GPIO1[15] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SPIFI_SIO2 —** I/O lane 2 for SPIFI.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**I2S0_TX_SDA —** I2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**I2S1_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**LCD_VD12 —** LCD data.
P3_6	B13	C7	174	122	[2]	N; PU	I/O	**GPIO0[6] —** General purpose digital input/output pin.
							I/O	**SPI_MISO —** Master In Slave Out for SPI.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SPIFI_MISO —** Input 1 in SPIFI quad mode; SPIFI output IO1.
							-	**R —** Function reserved.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_7	C11	D7	176	123	[2]	N; PU	-	**R —** Function reserved.
							I/O	**SPI_MOSI —** Master Out Slave In for SPI.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							I/O	**SPIFI_MOSI —** Input I0 in SPIFI quad mode; SPIFI output IO0.
							I/O	**GPIO5[10] —** General purpose digital input/output pin.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P3_8	C10	E7	179	124	[2]	N; PU	-	**R —** Function reserved.
							I	**SPI_SSEL —** Slave Select for SPI. Note that this pin in an input pin only. The SPI in master mode cannot drive the CS input on the slave. Any GPIO pin can be used for SPI chip select in master mode.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							I/O	**SPIFI_CS —** SPIFI serial flash chip select.
							I/O	**GPIO5[11] —** General purpose digital input/output pin.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
Debug pins								
DBGEN	L4	A6	41	28	[2]	I	I	JTAG interface control signal. Also used for boundary scan. To use the part in functional mode, connect this pin in one of the following ways: • Leave DBGEN open. The DBGEN pin is pulled up internally by a 50 kΩ resistor. • Tie DBGEN to VDDIO. • Pull DBGEN up to VDDIO with an external pull-up resistor.
TCK/SWDCLK	J5	H2	38	27	[2]	I; F	I	Test Clock for JTAG interface (default) or Serial Wire (SW) clock.
$\overline{\text{TRST}}$	M4	B4	42	29	[2]	I; PU	I	Test Reset for JTAG interface.
TMS/SWDIO	K6	C4	44	30	[2]	I; PU	I	Test Mode Select for JTAG interface (default) or SW debug data input/output.
TDO/SWO	K5	H3	46	31	[2]	O	O	Test Data Out for JTAG interface (default) or SW trace output.
TDI	J4	G3	35	26	[2]	I; PU	I	Test Data In for JTAG interface.
USB0 pins								
USB0_DP	F2	E1	26	18	[6]	-	I/O	USB0 bidirectional D+ line. Do not add an external series resistor.
USB0_DM	G2	E2	28	20	[6]	-	I/O	USB0 bidirectional D− line. Do not add an external series resistor.
USB0_VBUS	F1	E3	29	21	[6][7]	-	I	VBUS pin (power on USB cable). This pin includes an internal pull-down resistor of 64 kΩ (typical) ± 16 kΩ.
USB0_ID	H2	F1	30	22	[8]	-	I	Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH). For OTG this pin has an internal pull-up resistor.
USB0_RREF	H1	F3	32	24	[8]	-		12.0 kΩ (accuracy 1 %) on-board resistor to ground for current reference.
USB1 pins								
USB1_DP	F12	E9	129	89	[9]	-	I/O	USB1 bidirectional D+ line. Add an external series resistor of 33 Ω +/- 2 %.
USB1_DM	G12	E10	130	90	[9]	-	I/O	USB1 bidirectional D− line. Add an external series resistor of 33 Ω +/- 2 %.
I^2C-bus pins								
I2C0_SCL	L15	D6	132	92	[10]	I; F	I/O	I^2C clock input/output. Open-drain output (for I^2C-bus compliance).
I2C0_SDA	L16	E6	133	93	[10]	I; F	I/O	I^2C data input/output. Open-drain output (for I^2C-bus compliance).
Reset and wake-up pins								
$\overline{\text{RESET}}$	D9	B6	185	128	[11]	I; IA	I	External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin does not have an internal pull-up.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
XTAL1	D1	B1	18	12	[8]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	E1	C1	19	13	[8]	-	O	Output from the oscillator amplifier.
Power and ground pins								
USB0_VDDA 3V3_DRIVER	F3	D1	24	16		-	-	Separate analog 3.3 V power supply for driver.
USB0 _VDDA3V3	G3	D2	25	17		-	-	USB 3.3 V separate power supply voltage.
USB0_VSSA _TERM	H3	D3	27	19		-	-	Dedicated analog ground for clean reference for termination resistors.
USB0_VSSA _REF	G1	F2	31	23		-	-	Dedicated clean analog ground for generation of reference currents and voltages.
VDDA	B4	B2	198	137		-	-	Analog power supply and ADC reference voltage.
VBAT	B10	C5	184	127		-	-	RTC power supply: 3.3 V on this pin supplies power to the RTC.
VDDREG	F10, F9, L8, L7	E4, E5, F4	135, 188, 195, 82, 33	94, 131, 59, 25			-	Main regulator power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.
VPP	E8	-	-	-	[12]	-	-	OTP programming voltage.
VDDIO	D7, E12, F7, F8, G10, H10, J6, J7, K7, L9, L10, N7, N13	F10, K5	6, 52, 57, 102, 110, 155, 160, 202	5, 36, 41, 71, 77, 107, 111, 141	[12]	-	-	I/O power supply. Tie the VDDREG and VDDIO pins to a common power supply to ensure the same ramp-up time for both supply voltages.

7.6.1 Features

- ARM Cortex-M4 core:
  - Controls system exceptions and peripheral interrupts
  - Support for up to 53 vectored interrupts
  - Eight programmable interrupt priority levels with hardware priority level masking
  - Relocatable vector table
  - Non-Maskable Interrupt (NMI)
  - Software interrupt generation
- ARM Cortex-M0 core:
  - Support for up to 32 interrupts
  - Four programmable interrupt priority levels with hardware priority level masking

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

7.7 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval.

Remark: The SysTick is not included in the ARM Cortex-M0 core implementation.

7.8 Event router

The event router combines various internal signals, interrupts, and the external interrupt pins (WAKEUP[3:0]) to create an interrupt in the NVIC, if enabled. In addition, the event router creates a wake-up signal to the ARM core and the CCU for waking up from Sleep, Deep-sleep, Power-down, and Deep power-down modes. Individual events can be configured as edge or level sensitive and can be enabled or disabled in the event router. The event router can be battery powered.

The following events if enabled in the event router can create a wake-up signal from sleep, deep-sleep, power-down, and deep power-down modes and/or create an interrupt:

- External pins WAKEUP0/1/2/3 and $\overline{\text{RESET}}$
- Alarm timer, RTC (32 kHz oscillator running)

The following events if enabled in the event router can create a wake-up signal from sleep mode only and/or create an interrupt:

- WWDT, BOD interrupts.
- C_CAN0/1 and QEI interrupts.
- Ethernet, USB0, USB1 signals.
- Selected outputs of combined timers (SCTimer/PWM and timer0/1/3).

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasing and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.18.2.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface (SPIFI) with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.
- Supports DMA access.

7.18.3 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

- Secure Digital memory (SD version 3.0)
- Secure Digital I/O (SDIO version 2.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1)
- MultiMedia Cards (MMC version 4.4)

7.18.4 External Memory Controller (EMC)

Remark: The EMC is available on all LPC435x/3x/2x/1x parts. The following memory bus widths are supported:

- LBGA256 packages: 32 bit
- TFBGA100 packages: 16 bit
- LQFP208 packages: 16 bit
- LQFP144 packages: 16 bit

The LPC435x/3x/2x/1x EMC is a Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and NOR flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals.

Table 6. EMC pinout for different packages

Function	LBGA256	TFBGA100	LQFP208	LQFP144
A	EMC_A[23:0]	EMC_A[13:0]	EMC_A[23:0]	EMC_A[15:0]
D	EMC_D[31:0]	EMC_D[7:0]	EMC_D[15:0]	EMC_D[15:0]
$\overline{\text{BLS}}$	$\overline{\text{EMC\_BLS[3:0]}}$	$\overline{\text{EMC\_BLS0}}$	$\overline{\text{EMC\_BLS[1:0]}}$	$\overline{\text{EMC\_BLS[1:0]}}$
$\overline{\text{CS}}$	$\overline{\text{EMC\_CS[3:0]}}$	$\overline{\text{EMC\_CS0}}$	$\overline{\text{EMC\_CS[3:0]}}$	$\overline{\text{EMC\_CS[1:0]}}$

7.19.6.1 Features

- The I^2S interfaces has separate input/output channels, each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96, 192) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I^2S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests controlled by programmable buffer levels. The DMA requests are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S-bus input and I^2S-bus output.

7.19.7 C_CAN

Remark: The LPC435x/3x/2x/1x each contain two C_CAN controllers.

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

7.19.7.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

7.20 Counter/timers and motor control

7.20.1 General purpose 32-bit timers/external event counters

Remark: The LPC435x/3x/2x/1x include four 32-bit timer/counters.

7.21 Analog peripherals

7.21.1 Analog-to-Digital Converter (ADC0/1)

Remark: The LPC435x/3x/2x/1x contain two 10-bit ADCs.

7.21.1.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 to VDDA.
- Sampling frequency up to 400 kSamples/s.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on ADCTRIG0 or ADCTRIG1 pins, combined timer outputs 8 or 15, or the PWM output MCOA2.
- Individual result registers for each A/D channel to reduce interrupt overhead.
- DMA support.

7.21.2 Digital-to-Analog Converter (DAC)

7.21.2.1 Features

- 10-bit resolution
- Monotonic by design (resistor string architecture)
- Controllable conversion speed
- Low power consumption

7.22 Peripherals in the RTC power domain

7.22.1 RTC

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power when the CPU does not access its registers, especially in the reduced power modes. A separate 32 kHz oscillator clocks the RTC. The oscillator produces a 1 Hz internal time reference and is powered by its own power supply pin, VBAT.

7.22.1.1 Features

- Measures the passage of time to maintain a calendar and clock. Provides seconds, minutes, hours, day of month, month, year, day of week, and day of year.
- Ultra-low power design to support battery powered systems. Uses power from the CPU power supply when it is present.
- Dedicated battery power supply pin.
- RTC power supply is isolated from the rest of the chip.
- Calibration counter allows adjustment to better than ±1 sec/day with 1 sec resolution.
- Periodic interrupts can be generated from increments of any field of the time registers.

10. Static characteristics

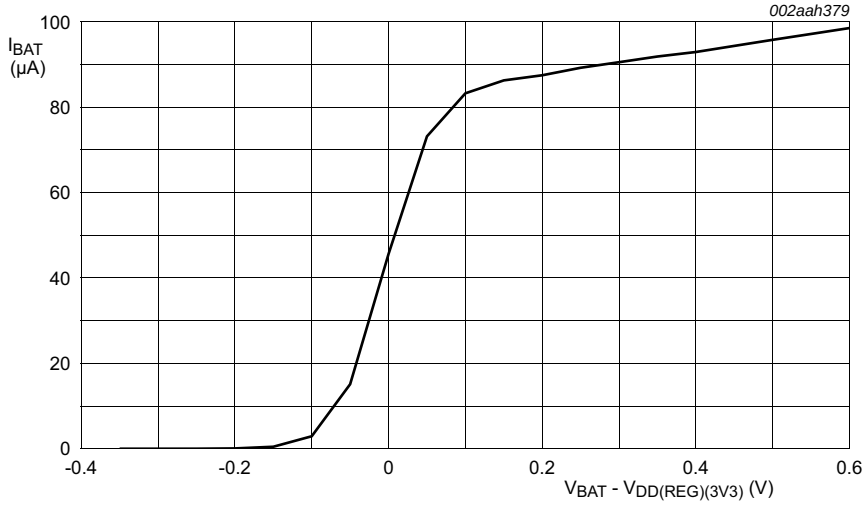
Table 11. Static characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(IO)}$	input/output supply voltage		[17]	2.4	-	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)		[2]	2.4	-	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pin VDDA		2.4	-	3.6	V
		on pins USB0_VDDA3V3_ DRIVER and USB0_VDDA3V3		3.0	3.3	3.6	V
V_{BAT}	battery supply voltage		[2]	2.4	-	3.6	V
$V_{prog(pf)}$	polyfuse programming voltage	on pin VPP (for OTP)	[3]	2.7	-	3.6	V
$I_{prog(pf)}$	polyfuse programming current	on pin VPP; OTP programming time ≤ 1.6 ms		-	-	30	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	Active mode; ARM Cortex-M0 core in reset; code `while(1){}` executed from RAM; all peripherals disabled; PLL1 enabled					
		CCLK = 12 MHz	[4]	-	10	-	mA
		CCLK = 60 MHz	[4]		28	-	mA
		CCLK = 120 MHz	[4]	-	51	-	mA
		CCLK = 180 MHz	[4]	-	74	-	mA
		CCLK = 204 MHz	[4]	-	83	-	mA
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	after WFE/WFI instruction executed from RAM; all peripherals disabled; ARM Cortex-M0 core in reset					
		sleep mode	[4][5]	-	8.8	-	mA
		deep-sleep mode	[4]	-	145	-	µA
		power-down mode	[4]	-	23	-	µA
		deep power-down mode	[4][6]	-	0.05	-	µA
		deep power-down mode; VBAT floating	[4]	-	3.0	-	µA
I_{BAT}	battery supply current	V_{BAT} = 3.0 V; $V_{DD(REG)(3V3)}$ = 3.3 V	[7]	-		0.1	nA

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76	mA
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[13] [14] [15]	-	62	-	μA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	0	-	μA
Open-drain I^2C0-bus pins							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			−0.5	0.14	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[12]	-	4.5	-	μA
		V_I = 5 V		-	-	10	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	-	1.2	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	-	1.2	V
C_{io}	input/output capacitance		[16]	-	-	0.8	pF
USB0 pins[17]							
V_I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		$V_{DD(IO)} \geq 2.4$ V		0	-	5.25	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
R_{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ



Conditions: $V_{DD(REG)(3V3)}$ = 3.0 V; V_{BAT} = 2.6 V to 3.6 V; CCLK = 12 MHz.

Remark: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V.

Fig 19. Typical battery supply current in Active mode

10.2 Peripheral power consumption

The typical power consumption at T = 25 °C for each individual peripheral is measured as follows:

1. Enable all branch clocks and measure the current $I_{DD(REG)(3V3)}$.
2. Disable the branch clock to the peripheral to be measured and keep all other branch clocks enabled.
3. Calculate the difference between measurement 1 and 2. The result is the peripheral power consumption.

Table 12. Peripheral power consumption

Peripheral	Branch clock	$I_{DD(REG)(3V3)}$ in mA	
		Branch clock frequency = 48 MHz	Branch clock frequency = 96 MHz
M0 core	CLK_M4_M0APP	3.3	6.6
I2C1	CLK_APB3_I2C1	0.01	0.01
I2C0	CLK_APB1_I2C0	< 0.01	0.02
DAC	CLK_APB3_DAC	0.01	0.02
ADC0	CLK_APB3_ADC0	0.07	0.07
ADC1	CLK_APB3_ADC1	0.07	0.07
CAN0	CLK_APB3_CAN0	0.17	0.17
CAN1	CLK_APB1_CAN1	0.16	0.15
MOTOCON	CLK_APB1_MOTOCON	0.04	0.04
I2S	CLK_APB1_I2S	0.09	0.08
SPIFI	CLK_SPIFI, CLK_M4_SPIFI	1.14	2.29

11.13 SPI interface

Table 28. Dynamic characteristics: SPI

T_{amb} = −40 °C to +105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Simulated values.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{cy(PCLK)}$	PCLK cycle time			5			ns
$T_{cy(clk)}$	clock cycle time		[1]	40	-	-	ns
Master							
t_{DS}	data set-up time			7.2	-	-	ns
t_{DH}	data hold time			0	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	3.7	ns
$t_{h(Q)}$	data output hold time			-	-	1.2	ns
Slave							
t_{DS}	data set-up time			1.2	-	-	ns
t_{DH}	data hold time			$3 \times T_{cy(PCLK)} + 0.54$	-	-	ns
$t_{v(Q)}$	data output valid time			-	-	$3 \times T_{cy(PCLK)} + 9.7$	ns
$t_{h(Q)}$	data output hold time			-	-	$2 \times T_{cy(PCLK)} + 7.1$	ns

[1] $T_{cy(clk)}$ = 8/BASE_SPI_CLK. $T_{cy(PCLK)}$ = 1/BASE_SPI_CLK.

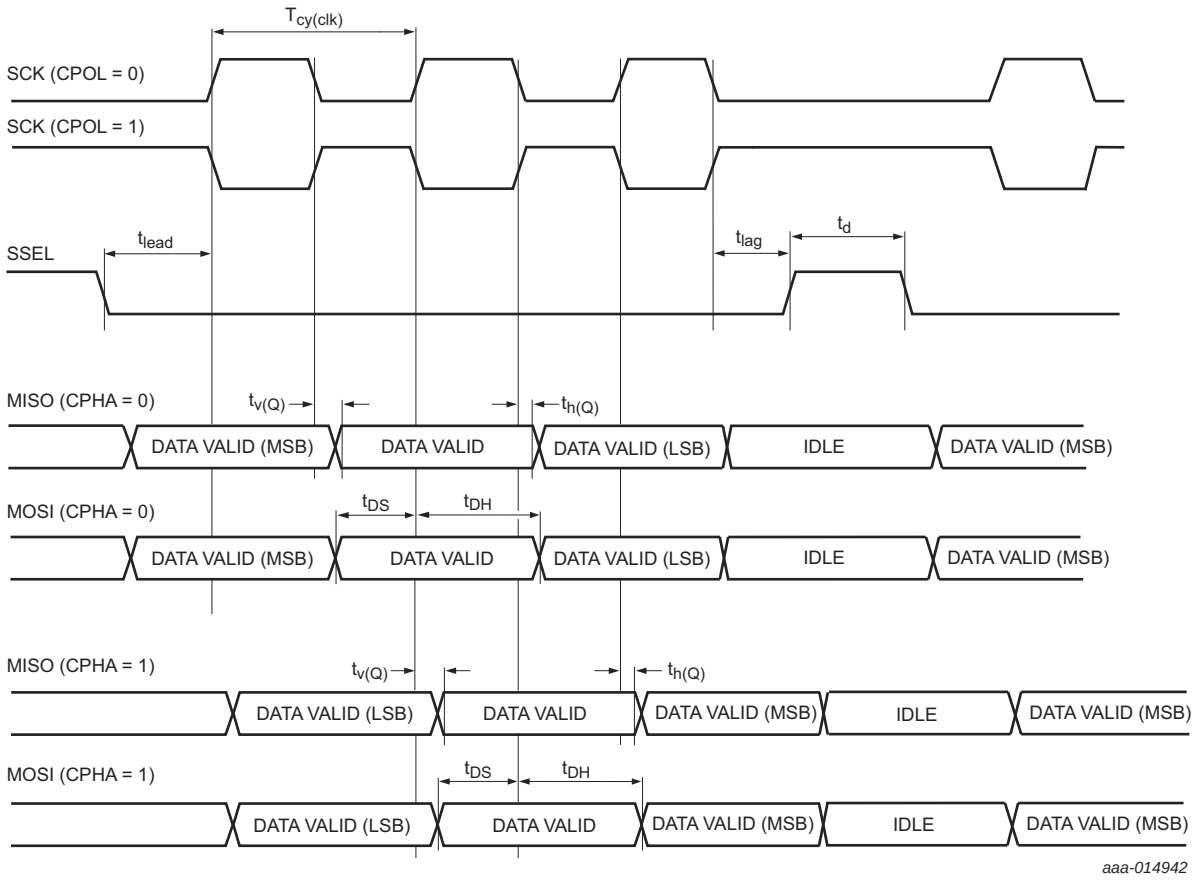
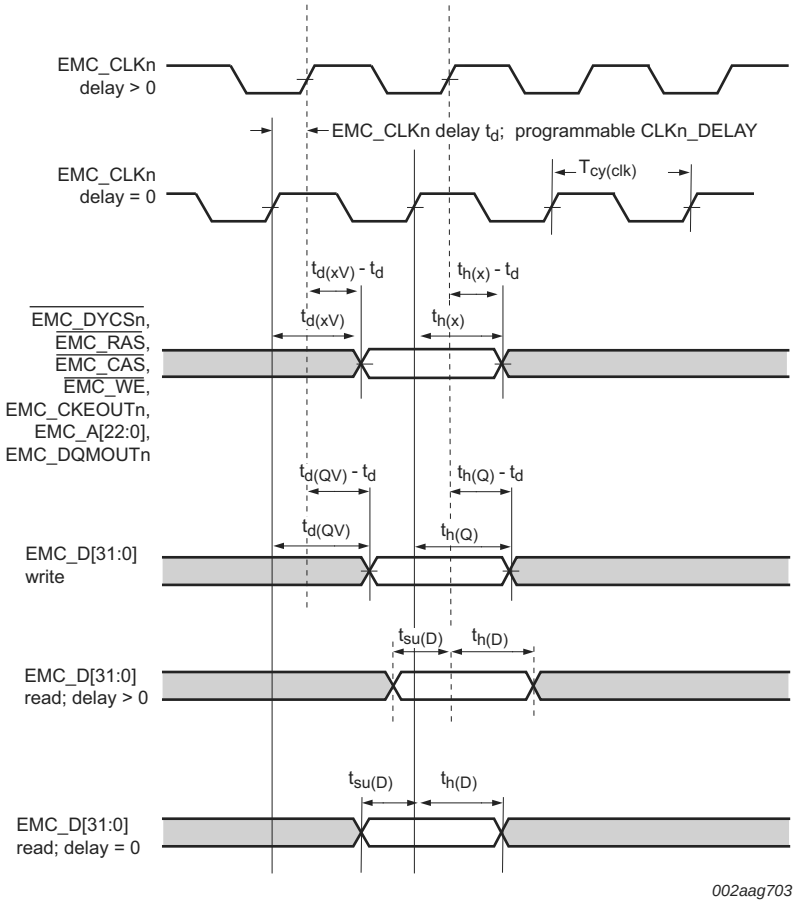


Fig 32. SSP in SPI mode and SPI slave timing



For the programmable EMC_CLK[3:0] clock delays CLKn_DELAY, see Table 31.

Remark: For SDRAM operation, set CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY in the EMCDELAYCLK register.

Fig 37. SDRAM timing

Table 35. Static characteristics: USB0 PHY pins[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
High-speed mode							
P_{cons}	power consumption		[2]	-	68	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current	[3]	-	18	-	mA
		during transmit		-	31	-	mA
		during receive		-	14	-	mA
		with driver tri-stated		-	14	-	mA
I_{DDD}	digital supply current			-	7	-	mA
Full-speed/low-speed mode							
P_{cons}	power consumption		[2]	-	15	-	mW
$I_{DDA(3V3)}$	analog supply current (3.3 V)	on pin USB0_VDDA3V3_DRIVER; total supply current		-	3.5	-	mA
		during transmit		-	5	-	mA
		during receive		-	3	-	mA
		with driver tri-stated		-	3	-	mA
I_{DDD}	digital supply current			-	3	-	mA
Suspend mode							
$I_{DDA(3V3)}$	analog supply current (3.3 V)			-	24	-	μA
		with driver tri-stated		-	24	-	μA
		with OTG functionality enabled		-	3	-	mA
I_{DDD}	digital supply current			-	30	-	μA
VBUS detector outputs							
V_{th}	threshold voltage	for VBUS valid		4.4	-	-	V
		for session end		0.2	-	0.8	V
		for A valid		0.8	-	2	V
		for B valid		2	-	4	V
V_{hys}	hysteresis voltage	for session end		-	150	10	mV
		A valid		-	200	10	mV
		B valid		-	200	10	mV

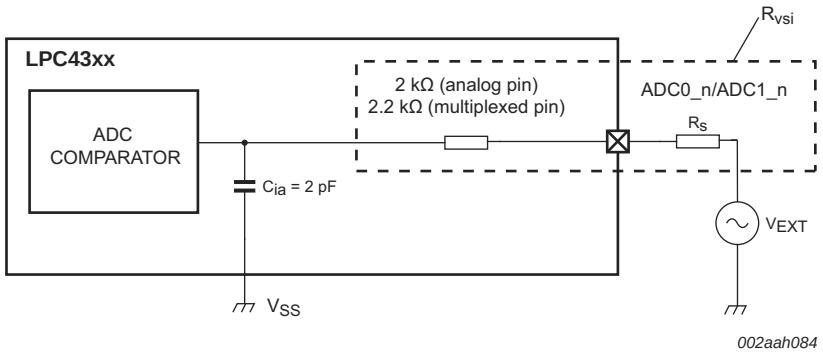
[1] Characterized but not implemented as production test.

[2] Total average power consumption.

[3] The driver is active only 20 % of the time.

11.19 Ethernet

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.



$Rs < 1/((7 \times f_{clk(ADC)} \times C_{ia}) - 2\ k\Omega)$

Fig 42. ADC interface to pins

Table 40. DAC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
E_D	differential linearity error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.8	-	LSB
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	code = 0 to 975 $2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±1.0	-	LSB
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.5	-	LSB
E_O	offset error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.8	-	LSB
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	LSB
E_G	gain error	$2.7\ V \le V_{DDA(3V3)} \le 3.6\ V$	[1]	-	±0.3	-	%
		$2.4\ V \le V_{DDA(3V3)} < 2.7\ V$		-	±1.0	-	%
C_L	load capacitance			-	-	200	pF
R_L	load resistance			1	-	-	kΩ
t_s	settling time		[2]		0.4		μσ

[1] In the DAC CR register, bit BIAS = 0 (see the *LPC43xx user manual*).

[2] Settling time is calculated within 1/2 LSB of the final value.

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Parameter t_{ret} (retention time) for EEPROM updated in Table 15. • SGPIO and SPI location corrected in Figure 1. • SGPIO-to-DMA connection updated in Figure 6. • Parameter $V_{DDA(3V3)}$ added for pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3 in Table 11. • Parameter name $I_{DD(ADC)}$ changed to I_{DDA} in Table 11. • Minimum wake-up time from sleep mode added in Table 16. • Data for $I_{DD(IO)}$ added in Table 11. • Corrected max voltage on pins USB0_DP, USB0_DM, USB0_VBUS, USB1_DP, and USB1_DM in Table 7 and Table 11 to be consistent with USB specifications. • SPI and SGPIO peripheral power consumption added in Table 12. • SPI timing characteristics added. See Section 11.12. • SGPIO timing characteristics added. See Section 11.15. • Data sheet status changed to Product data sheet. • Conditions RPHASE1 and RPHASE2 corrected in Table 15 “EEPROM characteristics”. RPHASE1: t_{wait} > 70 ns. RPHASE2: t_{wait} > 35 ns. • $I_{DD(REG)(3V3)}$ updated in Table 11 “Static characteristics” for the following conditions: – Active mode: CCLK = 12 MHz; $I_{DD(REG)(3V3)}$ changed from 9.3 mA to 10 mA. – Active mode: CCLK = 60 MHz; $I_{DD(REG)(3V3)}$ changed from 26 mA to 28 mA. – Active mode: CCLK = 120 MHz; $I_{DD(REG)(3V3)}$ changed from 46 mA to 51 mA. – Active mode: CCLK = 180 MHz; $I_{DD(REG)(3V3)}$ changed from 66 mA to 74 mA. – Active mode: CCLK = 204 MHz; $I_{DD(REG)(3V3)}$ changed from 75 mA to 83 mA. – Sleep mode: CCLK = 12 MHz; $I_{DD(REG)(3V3)}$ changed from 6.2 mA to 8.8 mA. • Power consumption data in Figure 11 to Figure 14 updated. • IRC specifications corrected in Table 19 “Dynamic characteristic: IRC oscillator”. Accuracy changed to +/- 3 % over the entire temperature range. • SPIFI timing diagram corrected and specified for mode 0. See Table 27. • Table 21 “Dynamic characteristic: I/O pins[1]” added. • Parameter C_I corrected for high-drive pins (changed from 2 pF to 5.2 pF). See Table 11. • Internal pull-up resistor configuration added for $\overline{\text{RESET}}$, WAKEUPn, and ALARM pins. See Table 3. • Description of DEBUG pin updated. • Input range for PLL1 corrected: 1 MHz to 25 MHz. See Section 7.23.7 “System PLL1”. • Signal polarity of EMC_CKEOUT and EMC_DQMOUT corrected. Both signals are active HIGH. • SPIFI output timing parameters in Table 27 corrected to apply to Mode 0: – $t_{v(Q)}$ changed to 3.2 ns. – $t_{h(Q)}$ changed to 0.2 ns,		