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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4337jbd144e

Table 3. Pin description

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
Multiplexed digital pins								
P0_0	L3	G2	47	32	[2]	N; PU	I/O	**GPIO0[0] —** General purpose digital input/output pin.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
							I/O	**SGPIO0 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**I2S1_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
P0_1	M2	G1	50	34	[2]	N; PU	I/O	**GPIO0[1] —** General purpose digital input/output pin.
							I/O	**SSP1_MOSI —** Master Out Slave in for SSP1.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SGPIO1 —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
								ENET_TX_EN — Ethernet transmit enable (RMII/MII interface).
							I/O	**I2S1_TX_SDA —** I2S1 transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
P1_0	P2	H1	54	38	[2]	N; PU	I/O	**GPIO0[4] —** General purpose digital input/output pin.
							I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
							I/O	**EMC_A5 —** External memory address line 5.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
							I/O	**EMC_D12 —** External memory data line 12.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P1_20	M10	K10	100	70	[2]	N; PU	I/O	**GPIO0[15] —** General purpose digital input/output pin.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							-	**R —** Function reserved.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							I	**T0_CAP2 —** Capture input 2 of timer 0.
							-	**R —** Function reserved.
							I/O	**SGPIO13 —** General purpose digital input/output pin.
							I/O	**EMC_D11 —** External memory data line 11.
P2_0	T16	G10	108	75	[2]	N; PU	I/O	**SGPIO4 —** General purpose digital input/output pin.
							O	**U0_TXD —** Transmitter output for USART0. See Table 4 for ISP mode.
							I/O	**EMC_A13 —** External memory address line 13.
							O	**USB0_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the USB_PPWR used on other NXP LPC parts.
							I/O	**GPIO5[0] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input 0 of timer 3.
							O	**ENET_MDC —** Ethernet MIIM clock.
P2_1	N15	G7	116	81	[2]	N; PU	I/O	**SGPIO5 —** General purpose digital input/output pin.
							I	**U0_RXD —** Receiver input for USART0. See Table 4 for ISP mode.
							I/O	**EMC_A12 —** External memory address line 12.
							I	**USB0_PWR_FAULT —** Port power fault signal indicating overcurrent condition; this signal monitors over-current on the USB bus (external circuitry required to detect over-current condition).
							I/O	**GPIO5[1] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input 1 of timer 3.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P2_9	H16	B10	144	102	[2]	N; PU	I/O	**GPIO1[10] —** General purpose digital input/output pin. Boot pin (see Table 5).
							O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
							I/O	**U3_BAUD —** Baud pin for USART3.
							I/O	**EMC_A0 —** External memory address line 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_10	G16	E8	146	104	[2]	N; PU	I/O	**GPIO0[14] —** General purpose digital input/output pin.
							O	**CTOUT_2 —** SCT output 2. Match output 2 of timer 0.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**EMC_A1 —** External memory address line 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_11	F16	A9	148	105	[2]	N; PU	I/O	**GPIO1[11] —** General purpose digital input/output pin.
							O	**CTOUT_5 —** SCT output 5. Match output 3 of timer 3.
							I	**U2_RXD —** Receiver input for USART2.
							I/O	**EMC_A2 —** External memory address line 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P2_12	E15	B9	153	106	[2]	N; PU	I/O	**GPIO1[12] —** General purpose digital input/output pin.
							O	**CTOUT_4 —** SCT output 4. Match output 3 of timer 3.
							-	**R —** Function reserved.
							I/O	**EMC_A3 —** External memory address line 3.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**U2_UCLK —** Serial clock input/output for USART2 in synchronous mode.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PD_3	P4	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_6 —** SCT output 7. Match output 2 of timer 1.
							I/O	**EMC_D17 —** External memory data line 17.
							-	**R —** Function reserved.
							I/O	**GPIO6[17] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO7 —** General purpose digital input/output pin.
PD_4	T2	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_8 —** SCT output 8. Match output 0 of timer 2.
							I/O	**EMC_D18 —** External memory data line 18.
							-	**R —** Function reserved.
							I/O	**GPIO6[18] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO8 —** General purpose digital input/output pin.
PD_5	P6	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_9 —** SCT output 9. Match output 3 of timer 3.
							I/O	**EMC_D19 —** External memory data line 19.
							-	**R —** Function reserved.
							I/O	**GPIO6[19] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO9 —** General purpose digital input/output pin.
PD_6	R6	-	68	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_10 —** SCT output 10. Match output 3 of timer 3.
							I/O	**EMC_D20 —** External memory data line 20.
							-	**R —** Function reserved.
							I/O	**GPIO6[20] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO10 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PE_2	M14	-	115	-	[2]	N; PU	I	**ADCTRIG0 —** ADC trigger input 0.
							I	**CAN0_RD —** CAN receiver input.
							-	**R —** Function reserved.
							I/O	**EMC_A20 —** External memory address line 20.
							I/O	**GPIO7[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_3	K12	-	118	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CAN0_TD —** CAN transmitter output.
							I	**ADCTRIG1 —** ADC trigger input 1.
							I/O	**EMC_A21 —** External memory address line 21.
							I/O	**GPIO7[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_4	K13	-	120	-	[2]	N; PU	-	**R —** Function reserved.
							I	**NMI —** External interrupt input to NMI.
							-	**R —** Function reserved.
							I/O	**EMC_A22 —** External memory address line 22.
							I/O	**GPIO7[4] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_5	N16	-	122	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_3 —** SCT output 3. Match output 3 of timer 0.
							O	**U1_RTS —** Request to Send output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I/O	**EMC_D24 —** External memory data line 24.
							I/O	**GPIO7[5] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PE_10	E14	-	154	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
							O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I/O	**EMC_D29 —** External memory data line 29.
							I/O	**GPIO7[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_11	D16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**EMC_D30 —** External memory data line 30.
							I/O	**GPIO7[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**EMC_D31 —** External memory data line 31.
							I/O	**GPIO7[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**GPIO7[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

7.15 One-Time Programmable (OTP) memory

The OTP provides 64 bit+ 256 bit of memory for general-purpose use.

7.16 General Purpose I/O (GPIO)

The LPC435x/3x/2x/1x provide eight GPIO ports with up to 31 GPIO pins each.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back as well as the current state of the port pins.

All GPIO pins default to inputs with pull-up resistors enabled and input buffer disabled on reset. The input buffer must be turned on in the system control block SFS register before the GPIO input can be read.

7.16.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Up to eight GPIO pins can be selected from all GPIO pins to create an edge- or level-sensitive GPIO interrupt request (GPIO interrupts).
- Two GPIO group interrupts can be triggered by any pin or pins in each port (GPIO group0 and group1 interrupts).

7.17 Configurable digital peripherals

7.17.1 State Configurable Timer (SCTimer/PWM) subsystem

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable
- Limit, halt, stop, and start conditions
- Values of Match/Capture registers, plus reload or capture control values

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.17.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Events control outputs, interrupts, and DMA requests.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states
  - Match register 0 to 5 support a fractional component for the dither engine

7.17.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.17.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.

- Each slice has a 32-bit pattern match filter.

7.18 AHB peripherals

7.18.1 General Purpose DMA

The DMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receives. The source and destination areas can each be either a memory region or a peripheral for master 1, but only memory for master 0.

7.18.1.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- Two AHB bus masters for transferring data. These interfaces transfer data when a DMA request goes active. Master 1 can access memories and peripherals, master 0 can access memories only.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.18.2 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the ARM Cortex-M4 processor with little performance penalty compared to parallel flash devices with higher pin count.

7.18.5 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on the following parts: LPC435x, LPC433x, LPC432x. USB0 is not available on the LPC431x parts.

The USB OTG module allows the LPC435x/3x/2x/1x to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.18.5.1 Features

- Contains UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.6 High-speed USB Host/Device interface with ULPI (USB1)

Remark: USB1 is available on the following parts: LPC435x and LPC433x. USB1 is not available on the LPC432x and LPC431x parts.

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.18.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.7 LCD controller

Remark: The LCD controller is only available on parts LPC435x. LCD is not available on parts LPC433x, LPC432x, and LPC431x.

7.19.6.1 Features

- The I^2S interfaces has separate input/output channels, each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 192 kHz (16, 22.05, 32, 44.1, 48, 96, 192) kHz.
- Support for an audio master clock.
- Configurable word select period in master mode (separately for I^2S-bus input and output).
- Two 8-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests controlled by programmable buffer levels. The DMA requests are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I^2S-bus input and I^2S-bus output.

7.19.7 C_CAN

Remark: The LPC435x/3x/2x/1x each contain two C_CAN controllers.

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a high level of reliability.

7.19.7.1 Features

- Conforms to protocol version 2.0 parts A and B.
- Supports bit rate of up to 1 Mbit/s.
- Supports 32 Message Objects.
- Each Message Object has its own identifier mask.
- Provides programmable FIFO mode (concatenation of Message Objects).
- Provides maskable interrupts.
- Supports Disabled Automatic Retransmission (DAR) mode for time-triggered CAN applications.
- Provides programmable loop-back mode for self-test operation.

7.20 Counter/timers and motor control

7.20.1 General purpose 32-bit timers/external event counters

Remark: The LPC435x/3x/2x/1x include four 32-bit timer/counters.

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IC}	common-mode input voltage	high-speed mode		−50	200	500	mV
		full-speed/low-speed mode		800	-	2500	mV
		chirp mode		−50	-	600	mV
$V_{i(dif)}$	differential input voltage			100	400	1100	mV
USB1 pins (USB1_DP/USB1_DM)[17]							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[17]	-	-	±10	μA
V_{BUS}	bus supply voltage		[18]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|		0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range		0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage			0.8	-	2.0	V
V_{OL}	LOW-level output voltage for low-/full-speed	R_L of 1.5 kΩ to 3.6 V		-	-	0.18	V
V_{OH}	HIGH-level output voltage (driven) for low-/full-speed	R_L of 15 kΩ to GND		2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND		-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[19]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT} + 0.2$ V. Special conditions for $V_{DD(REG)(3V3)}$ apply when writing to the flash and EEPROM. See Table 14 and Table 15.

[3] Pin VPP should either be not connected (when OTP does not need to be programmed) or tied to pins VDDIO and VDDREG to ensure the same ramp-up time for both supply voltages.

[4] $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{DD(IO)}$ = 3.3 V; T_{amb} = 25 °C.

[5] PLL1 disabled; IRC running; CCLK = 12 MHz.

[6] V_{BAT} = 3.6 V.

[7] T_{amb} = -40 °C to +105 °C; $V_{DD(IO)} = V_{DDA}$ = 3.6 V; over entire frequency range CCLK = 12 MHz to 204 MHz; in active mode, sleep mode; deep-sleep mode, power-down mode, and deep power-down mode.

[8] On pin VBAT; T_{amb} = 25 °C.

[9] V_{ps} corresponds to the output of the power switch (see Table 9) which is determined by the greater of V_{BAT} and $V_{DD(Reg)(3V3)}$.

[10] $V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C.

[11] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[12] To V_{SS}.

[13] The values specified are simulated and absolute values.

[14] The weak pull-up resistor is connected to the $V_{DD(IO)}$ rail and pulls up the I/O pin to the $V_{DD(IO)}$ level.

[15] The input cell disables the weak pull-up resistor when the applied input voltage exceeds $V_{DD(IO)}$.

10.4 BOD and band gap static characteristics

Table 13. BOD static characteristics[1]

T_{amb} = 25 °C; simulated values for nominal processing.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 2					
		assertion		-	2.95	-	V
		de-assertion		-	3.03	-	V
		interrupt level 3					
		assertion		-	3.05	-	V
		de-assertion		-	3.13	-	V
		reset level 2					
		assertion		-	2.1	-	V
		de-assertion		-	2.18	-	V
		reset level 3					
		assertion		-	2.2	-	V
		de-assertion		-	2.28	-	V

[1] Interrupt and reset levels are selected by writing to the BODLV1/2 bits in the control register CREGE0, see the *LPC43xx user manual*.

Table 14. Band gap characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Unit
$V_{ref(bg)}$	band gap reference voltage	[1]	0.707	0.745	0.783	mV

[1] Based on characterization, not tested in production.

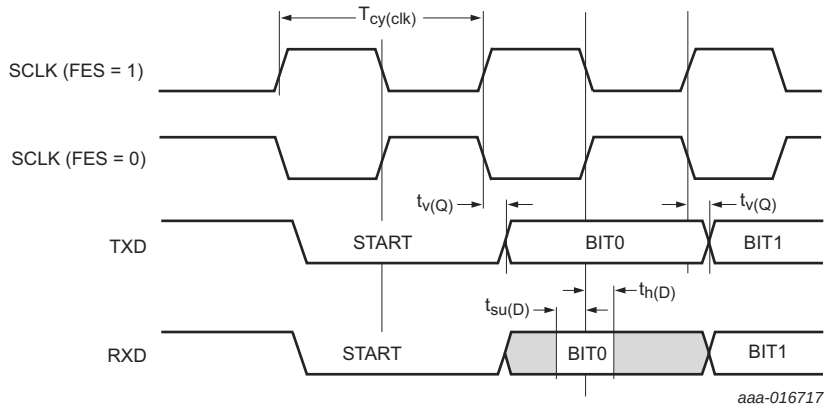


Fig 30. USART timing

Table 36. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 105 °C, 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; 2.7 V ≤ $V_{DD(IO)}$ ≤ 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
RMII mode						
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	50	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns
MII mode						
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	4	-	ns
t_h	hold time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]	2	-	ns
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	25	MHz
δ_{clk}	clock duty cycle		[1]	50	50	%
t_{su}	set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	4	-	ns
t_h	hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]	2	-	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

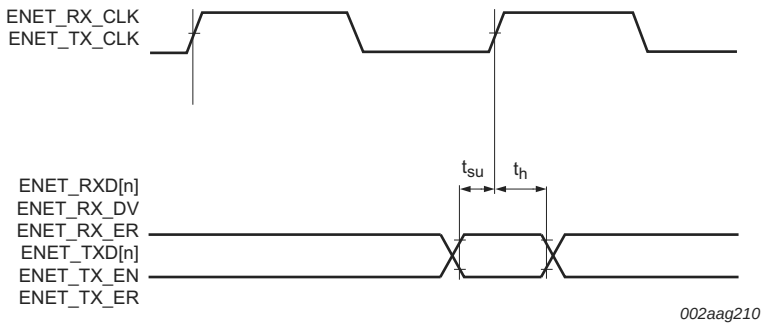


Fig 39. Ethernet timing

On the LPC435x/3x/2x/1x, USBn_VBUS pins are 5 V tolerant only when VDDIO is applied and at operating voltage level. Therefore, if the USBn_VBUS function is connected to the USB connector and the device is self-powered, the USBn_VBUS pins must be protected for situations when VDDIO = 0 V.

If VDDIO is always at operating level while VBUS = 5 V, the USBn_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where VDDIO can be 0 V and VBUS is directly applied to the USBn_VBUS pins, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USBn_VBUS pins in this case.

One method is to use a voltage divider to connect the USBn_VBUS pins to VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin will be greater than 0.7VDDIO to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

$VBUS_{max}$ = 5.25 V

VDDIO = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

For bus-powered devices, a regulator powered by USB can provide 3.3 V to VDDIO whenever bus power is present and ensure that power to the USBn_VBUS pins is always present when the 5 V VBUS signal is applied. See Figure 49.

Remark: Applying 5 V to the USBn_VBUS pins for a short time while the regulator ramps up might compromise the long-term reliability of the part but does not affect its function.

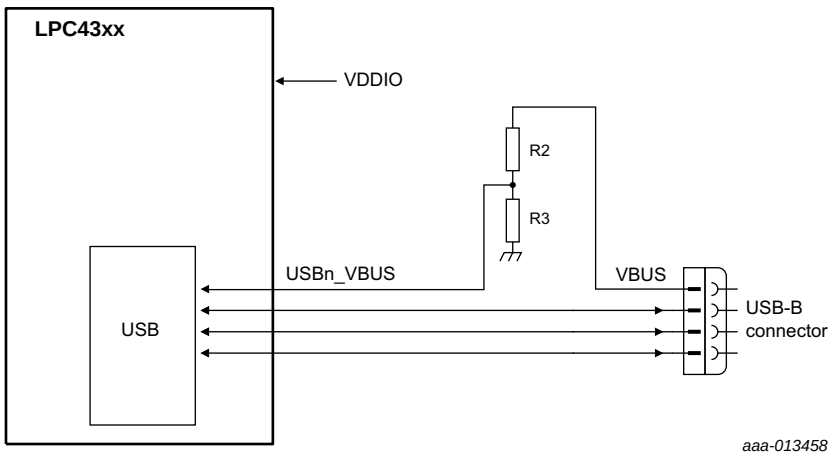
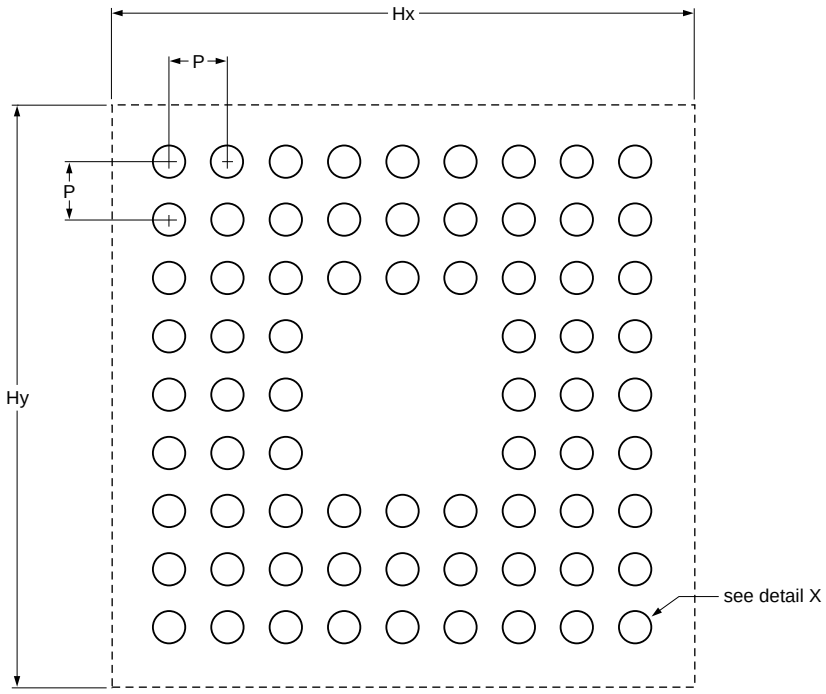


Fig 48. USB interface on a self-powered device where USBn_VBUS = 5 V

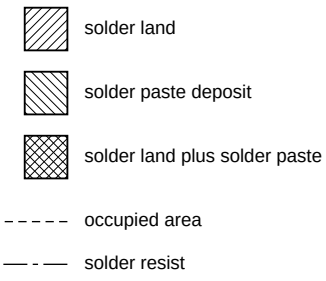
15. Soldering

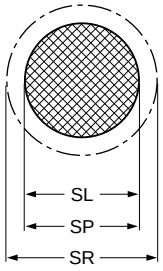
Footprint information for reflow soldering of LBGA256 package **SOT740-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

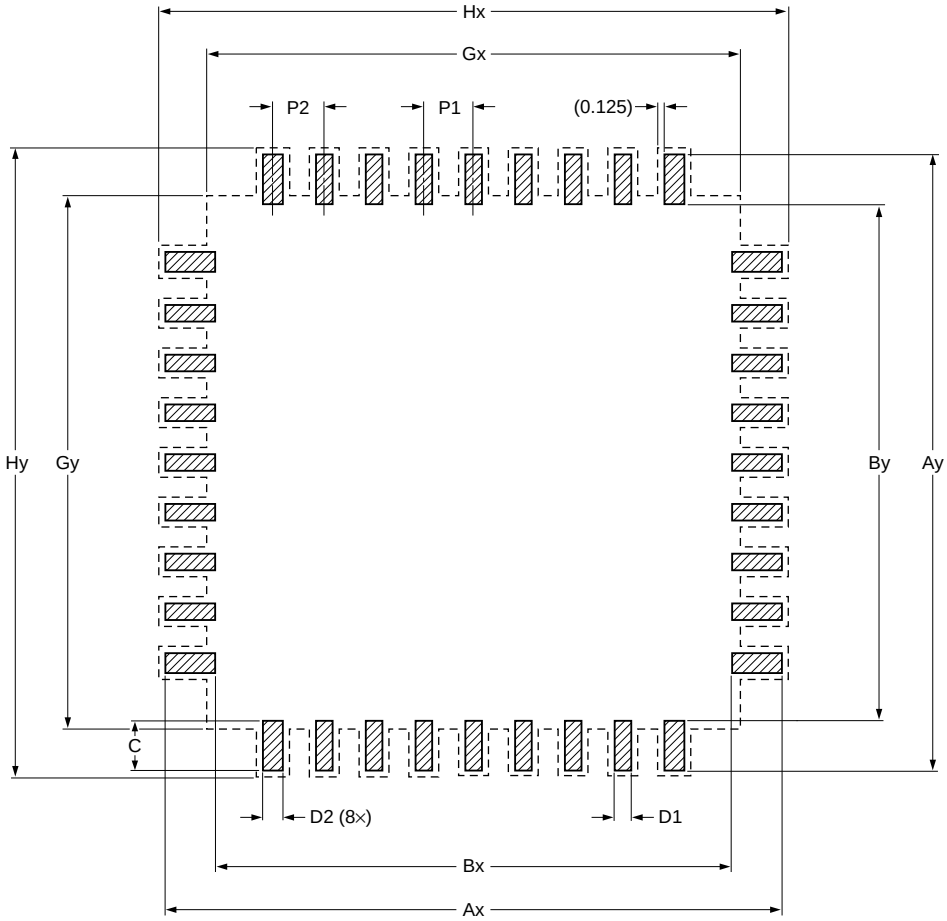
DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
1.00	0.450	0.450	0.600	17.500	17.500

sot740-2_fr

Fig 55. Reflow soldering of the LBGA256 package

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 57. Reflow soldering of the LQFP144 package

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• SD/MMC timing data updated. See Table 35 “Dynamic characteristics: SD/MMC”. • IEEE standard 802.3 compliance added to Section 11.18. Covers Ethernet dynamic characteristics of ENET_MDIO and ENET_MDC signals. • SSP master mode timing diagram updated with SSEL timing parameters. See Figure 31 “SSP in SPI mode and SPI master timing”. • Parameters t_{lead}, t_{lag}, and t_d added in Table 25 “Dynamic characteristics: SSP pins in SPI mode”. • Parameter t_{CSLWEL} with condition PB = 1 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 29 “Dynamic characteristics: Static asynchronous external memory interface”. • Parameter $t_{CSLBLSL}$ with condition PB = 0 corrected: (WAITWEN + 1) × $T_{cy(clk)}$ added. See Table 29 “Dynamic characteristics: Static asynchronous external memory interface”. • Removed restriction on C_CAN bus usage. See CAN.1 errata in Ref. 2. • General-purpose OTP size corrected.			
LPC435X_3X_2X_1X v.3	20121206	Preliminary data sheet	-	LPC4357_53_37_33 v.2.1
Modifications:	• TFBGA180 packages removed. • Part LPC432x and LPC431x added. • SCT dither engine added and SCT bi-directional event enable features added. • Figure 10 “Dual-core debug configuration” added. • T = 105 °C data added in Figure 20 to Figure 23. • Change symbol names and parameter names in Table 21. • Parameter I_{LH} updated for condition V_I = 5 V and T_{amb} = 25 °C/105 °C in Table 11. • Power consumption data added in Section 10.1. • SPIFI dynamic characteristics added in Section 11.16. • IRC accuracy corrected to ± 2 % for T_{amb} = -40 °C to 0 °C and T_{amb} = 85 °C to 105 °C. • Pull-up and Pull-down current data (Figure 24 and Figure 25) updated with data for T_{amb} = 105 °C. • SPIFI maximum data rate changed to 52 MB per second. • Recommendation for V_{BAT} use added: The recommended operating condition for the battery supply is $V_{DD(REG)(3V3)} > V_{BAT}$ + 0.2 V. • Table 14 “Band gap characteristics” added. • Section 7.23.9 “Power Management Controller (PMC)” added. • Description of ADC pins on digital/analog input pins changed. Each input to the ADC is connected to ADC0 and ADC1. See Table 3. • OTP memory size changed to 64 bit. • Use of C_CAN peripheral restricted in Section 2. • ADC channels limited to a total of 8 channels shared between ADC0 and ADC1.			
LPC4357_53_37_33 v.2.1	20120904	Preliminary data sheet	-	LPC4357_53_37_33 v.2
Modifications:	• SSP0 boot pin functions corrected in Table 5 and Table 4. Pin P3_3 = SSP0_SCK, pin P3_6 = SSP0_SSEL, pin P3_7 = SSP0_MISO, pin P3_8 = SSP0_MOSI. • SWD removed for ARM Cortex-M0. • BOD de-assertion levels added in Table 13. • Peripheral power consumption data added in Table 12. • Minimum value for all supply voltages changed to -0.5 V in Table 7.			

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