Welcome to E-XFL.COM

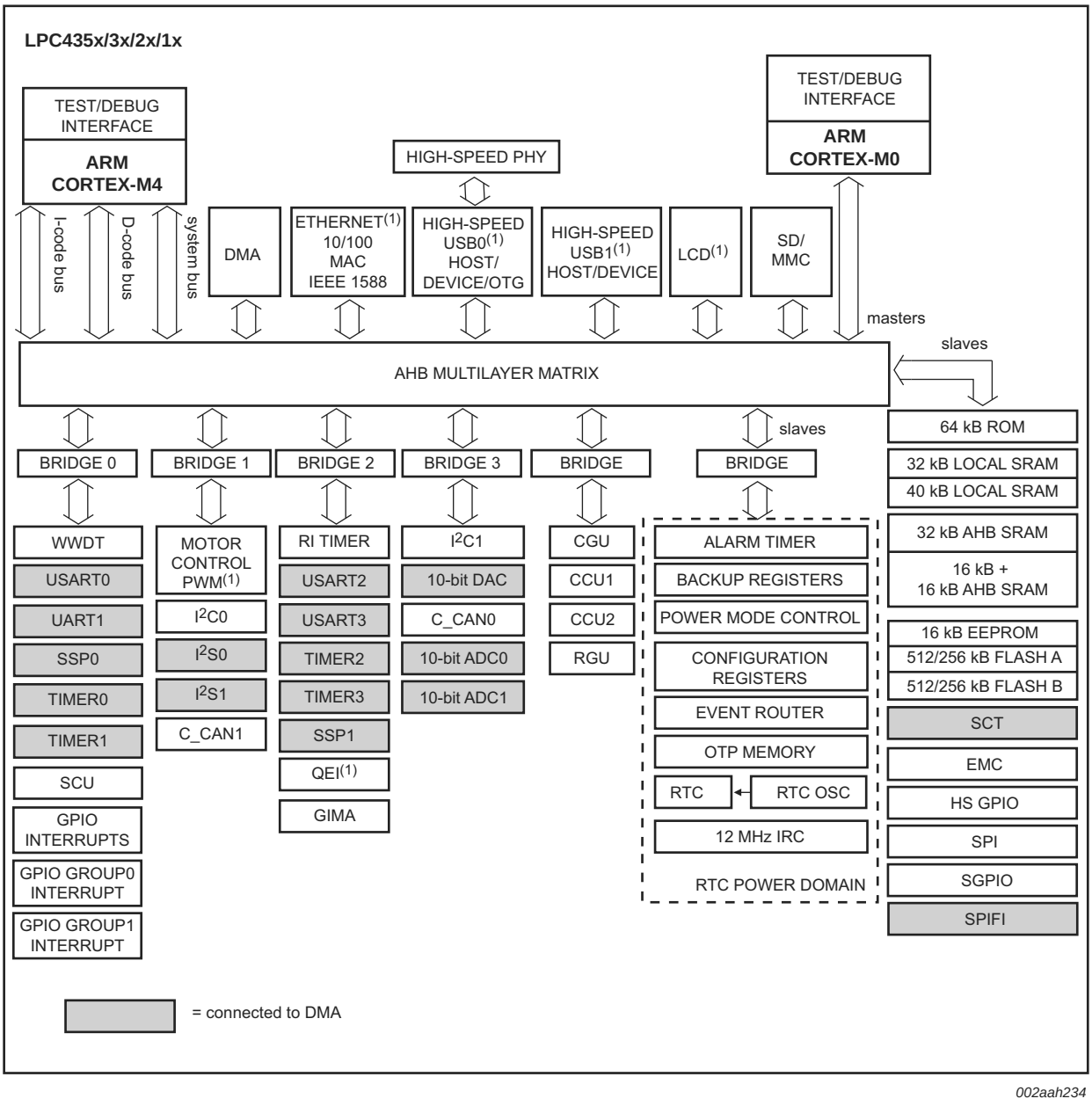
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0
Core Size	32-Bit Dual-Core
Speed	204MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, SD, SPI, SSI, SSP, UART/USART, USB, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	49
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 4x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc4337jet100e

5. Block diagram



(1) Not available on all parts. See Table 2.

Fig 1. LPC435x/3x/2x/1x Block diagram

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_0	M12	H7	105	73	[2]	N; PU	-	**R —** Function reserved.
							O	**I2S0_RX_MCLK —** I2S receive master clock.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**I2S0_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I²S-bus specification*.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_1	R15	G5	107	74	[2]	N; PU	I/O	**GPIO3[0] —** General purpose digital input/output pin.
							O	**EMC_DYCS1 —** SDRAM chip select 1.
							I/O	**U0_UCLK —** Serial clock input/output for USART0 in synchronous mode.
							I/O	**I2S0_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I²S-bus specification*.
							-	**R —** Function reserved.
							I	**T2_CAP0 —** Capture input 2 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_2	L13	J9	111	78	[2]	N; PU	I/O	**GPIO3[1] —** General purpose digital input/output pin.
							O	**EMC_CKEOUT1 —** SDRAM clock enable 1.
							I/O	**U0_DIR —** RS-485/EIA-485 output enable/direction control for USART0.
							I/O	**I2S0_RX_SDA —** I2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I²S-bus specification*.
							-	**R —** Function reserved.
							I	**T2_CAP1 —** Capture input 1 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
P6_11	H12	C9	143	101	[2]	N; PU	I/O	**GPIO3[7] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**EMC_CKEOUT0 —** SDRAM clock enable 0.
							-	**R —** Function reserved.
							O	**T2_MAT3 —** Match output 3 of timer 2.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P6_12	G15	-	145	103	[2]	N; PU	I/O	**GPIO2[8] —** General purpose digital input/output pin.
							O	**CTOUT_7 —** SCT output 7. Match output 3 of timer 1.
							-	**R —** Function reserved.
							O	**EMC_DQMOUT0 —** Data mask 0 used with SDRAM and static devices.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P7_0	B16	-	158	110	[2]	N; PU	I/O	**GPIO3[8] —** General purpose digital input/output pin.
							O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
							-	**R —** Function reserved.
							O	**LCD_LE —** Line end signal.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I/O	**SGPIO4 —** General purpose digital input/output pin.
P7_1	C14	-	162	113	[2]	N; PU	I/O	**GPIO3[9] —** General purpose digital input/output pin.
							O	**CTOUT_15 —** SCT output 15. Match output 3 of timer 3.
							I/O	**I2S0_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**LCD_VD19 —** LCD data.
							O	**LCD_VD7 —** LCD data.
							-	**R —** Function reserved.
							O	**U2_TXD —** Transmitter output for USART2.
							I/O	**SGPIO5 —** General purpose digital input/output pin.

Table 3. Pin description *…continued*

Pin name	LBGA256	TFBGA100	LQFP208	LQFP144		Reset state [1]	Type	Description
PE_10	E14	-	154	-	[2]	N; PU	-	**R —** Function reserved.
							I	**CTIN_3 —** SCT input 3. Capture input 1 of timer 1.
							O	**U1_DTR —** Data Terminal Ready output for UART 1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART 1.
							I/O	**EMC_D29 —** External memory data line 29.
							I/O	**GPIO7[10] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_11	D16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
							O	**U1_TXD —** Transmitter output for UART 1.
							I/O	**EMC_D30 —** External memory data line 30.
							I/O	**GPIO7[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
							I	**U1_RXD —** Receiver input for UART 1.
							I/O	**EMC_D31 —** External memory data line 31.
							I/O	**GPIO7[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**GPIO7[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

7.5 AHB multilayer matrix

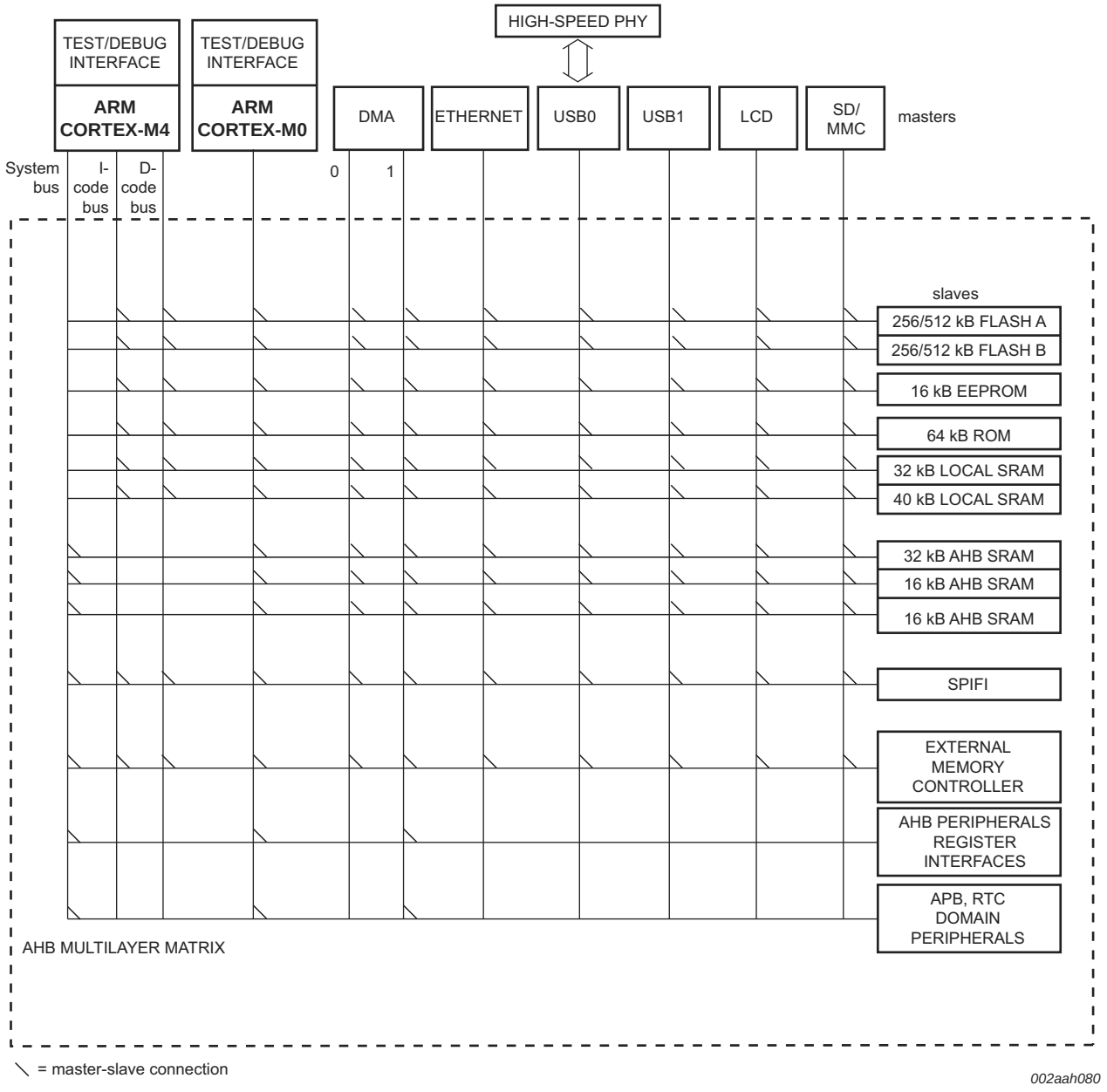


Fig 6. AHB multilayer matrix master and slave connections

7.6 Nested Vectored Interrupt Controller (NVIC)

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

The ARM Cortex-M0 co-processor has its own NVIC with 32 vectored interrupts. Most peripheral interrupts are shared between the Cortex-M0 and Cortex-M4 NVICs.

Table 5. Boot mode when OPT BOOT_SRC bits are zero

Boot mode	Pins				Description
	P2_9	P2_8	P1_2	P1_1	
USB1	LOW	HIGH	HIGH	LOW	Boot from USB1.
SPI (SSP)	LOW	HIGH	HIGH	HIGH	Boot from SPI flash connected to the SSP0 interface on P3_3 (function SSP0_SCK), P3_6 (function SSP0_SSEL), P3_7 (function SSP0_MISO), and P3_8 (function SSP0_MOSI)[1]
USART3	HIGH	LOW	LOW	LOW	Enter ISP mode using USART3 pins P2_3 and P2_4.

[1] The boot loader programs the appropriate pin function at reset to boot using either SSP0 or SPIFI.
Remark: Pin functions for SPIFI and SSP0 boot are different.

7.14 Memory mapping

The memory map shown in Figure 7 and Figure 8 is global to both the Cortex-M4 and the Cortex-M0 processors and all SRAM, flash, and EEPROM memory is shared between both processors. Each processor uses its own ARM private bus memory map for the NVIC and other system functions.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.17.1.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or and input/output condition in a specified state.
- Events control outputs, interrupts, and DMA requests.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
  - 8 inputs
  - 16 outputs
  - 16 match/capture registers
  - 16 events
  - 32 states
  - Match register 0 to 5 support a fractional component for the dither engine

7.17.2 Serial GPIO (SGPIO)

The Serial GPIOs offer standard GPIO functionality enhanced with features to accelerate serial stream processing.

7.17.2.1 Features

- Each SGPIO input/output slice can be used to perform a serial to parallel or parallel to serial data conversion.
- 16 SGPIO input/output slices each with a 32-bit FIFO that can shift the input value from a pin or an output value to a pin with every cycle of a shift clock.
- Each slice is double-buffered.
- Interrupt is generated on a full FIFO, shift clock, or pattern match.
- Slices can be concatenated to increase buffer size.

7.18.5 High-speed USB Host/Device/OTG interface (USB0)

Remark: USB0 is available on the following parts: LPC435x, LPC433x, LPC432x. USB0 is not available on the LPC431x parts.

The USB OTG module allows the LPC435x/3x/2x/1x to connect directly to a USB Host such as a PC (in device mode) or to a USB Device in host mode.

7.18.5.1 Features

- Contains UTMI+ compliant high-speed transceiver (PHY).
- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.6 High-speed USB Host/Device interface with ULPI (USB1)

Remark: USB1 is available on the following parts: LPC435x and LPC433x. USB1 is not available on the LPC432x and LPC431x parts.

The USB1 interface can operate as a full-speed USB Host/Device interface or can connect to an external ULPI PHY for High-speed operation.

7.18.6.1 Features

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals if connected to external ULPI PHY.
- Supports all full-speed USB-compliant peripherals.
- Supports interrupts.
- Supports Start Of Frame (SOF) frame length adjust.
- This module has its own, integrated DMA engine.
- USB interface electrical test software included in ROM USB stack.

7.18.7 LCD controller

Remark: The LCD controller is only available on parts LPC435x. LCD is not available on parts LPC433x, LPC432x, and LPC431x.

7.23.7 System PLL1

The PLL1 accepts an input clock frequency from an external oscillator in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz. This range is possible through an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider can be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset. After reset, software can enable the PLL. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 μs.

7.23.8 Reset Generation Unit (RGU)

The RGU allows generation of independent reset signals for individual blocks and peripherals on the LPC435x/3x/2x/1x.

7.23.9 Power Management Controller (PMC)

The PMC controls the power to the cores, peripherals, and memories.

The LPC435x/3x/2x/1x support the following power modes in order from highest to lowest power consumption:

1. Active mode
2. Sleep mode
3. Power-down modes:
   a. Deep-sleep mode
   b. Power-down mode
   c. Deep power-down mode

Active mode and sleep mode apply to the state of the core. In a dual-core system, either core can be in active or sleep mode independently of the other core.

If the core is in Active mode, it is fully operational and can access peripherals and memories as configured by software. If the core is in Sleep mode, it receives no clocks, but peripherals and memories remain running.

Either core can enter sleep mode from active mode independently of the other core and while the other core remains in active mode or is in sleep mode.

Power-down modes apply to the entire system. In the Power-down modes, both cores and all peripherals except for peripherals in the always-on power domain are shut down. Memories can remain powered for retaining memory contents as defined by the individual power-down mode.

Either core in active mode can put the part into one of the three power down modes if the core is enabled to do so. If both cores are enabled for putting the system into power-down, then the system enters power-down only once both cores have received a WFI or WFE instruction.

Wake-up from sleep mode is caused by an interrupt or event in the core's NVIC. The interrupt is captured in the NVIC and an event is captured in the Event router. Both cores can wake up from sleep mode independently of each other.

Wake-up from the Power-down modes, Deep-sleep, Power-down, and Deep power-down, is caused by an event on the WAKEUP pins or an event from the RTC or alarm timer.

When waking up from Deep power-down mode, the part resets and attempts to boot.

7.23.10 Power control

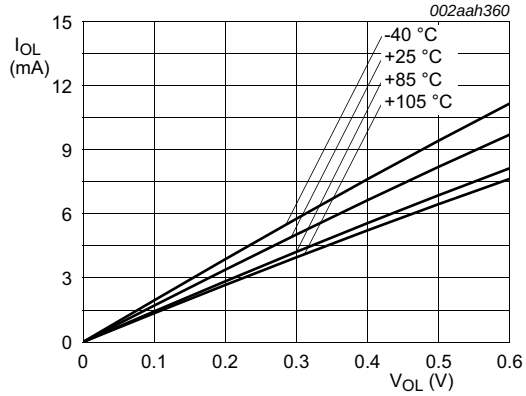
The LPC435x/3x/2x/1x feature several independent power domains to control power to the core and the peripherals (see Figure 9). The RTC and its associated peripherals (the alarm timer, the CREG block, the OTP controller, the back-up registers, and the event router) are located in the RTC power-domain. The main regulator or a battery supply can power the RTC. A power selector switch ensures that the RTC block is always powered on.

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

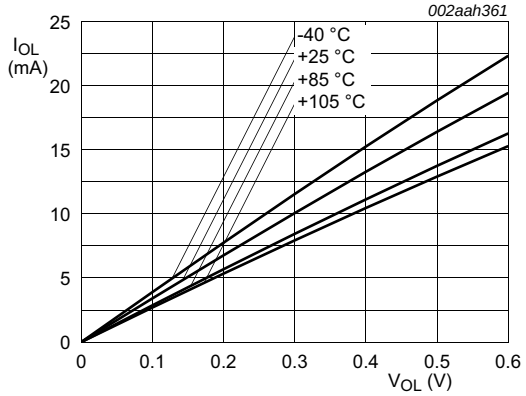
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −6 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−6	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		6	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86.5	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76.5	mA
I_{pd}	pull-down current	V_I = 5 V	[13] [14] [15]	-	93	-	μA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	10	-	μA
R_S	series resistance	on I/O pins with analog function; analog function enabled			200		Ω
I/O pins - high drive strength							
C_I	input capacitance			-	-	5.2	pF
I_{LL}	LOW-level leakage current	V_I = 0 V; on-chip pull-up resistor disabled		-	3	-	nA
I_{OZ}	OFF-state output current	V_O = 0 V to $V_{DD(IO)}$; on-chip pull-up/down resistors disabled; absolute value		-	3	-	nA
V_I	input voltage	pin configured to provide a digital function; $V_{DD(IO)} \geq 2.4$ V		0	-	5.5	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
V_O	output voltage	output active		0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{DD(IO)}$	V

Table 11. Static characteristics *…continued*
T_{amb} = −40 °C to +105 °C, unless otherwise specified.

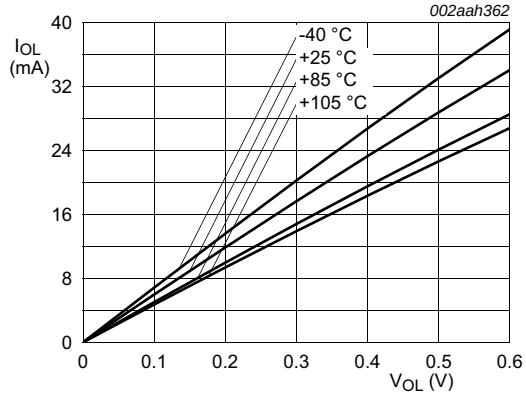
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA		$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 8 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(IO)} - 0.4$ V		−8	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		8	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	drive HIGH; connected to ground	[11]	-	-	86	mA
I_{OLS}	LOW-level short-circuit output current	drive LOW; connected to $V_{DD(IO)}$	[11]	-	-	76	mA
I_{pd}	pull-down current	$V_I = V_{DD(IO)}$	[13] [14] [15]	-	62	-	μA
I_{pu}	pull-up current	V_I = 0 V	[13] [14] [15]	-	−62	-	μA
		$V_{DD(IO)} < V_I \leq 5$ V		-	0	-	μA
Open-drain I^2C0-bus pins							
V_{IH}	HIGH-level input voltage			0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage			−0.5	0.14	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage			0.1 × $V_{DD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(IO)}$	[12]	-	4.5	-	μA
		V_I = 5 V		-	-	10	μA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	-	1.2	V
$V_{o(XTAL2)}$	output voltage on pin XTAL2			−0.5	-	1.2	V
C_{io}	input/output capacitance		[16]	-	-	0.8	pF
USB0 pins[17]							
V_I	input voltage	on pins USB0_DP; USB0_DM; USB0_VBUS					
		$V_{DD(IO)} \geq 2.4$ V		0	-	5.25	V
		$V_{DD(IO)}$ = 0 V		0	-	3.6	V
R_{pd}	pull-down resistance	on pin USB0_VBUS		48	64	80	kΩ



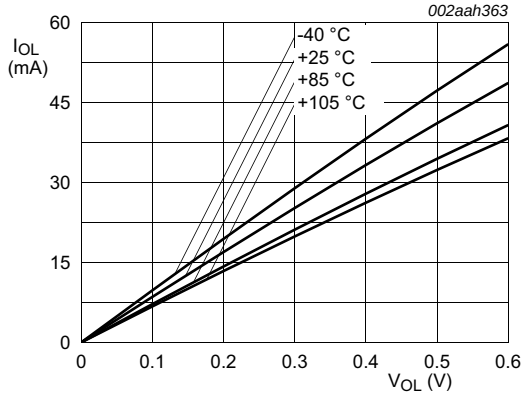
Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; normal-drive; EHD = 0x0.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; medium-drive; EHD = 0x1.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; high-drive; EHD = 0x2.



Conditions: $V_{DD(REG)(3V3)} = V_{DD(IO)} = 3.3$ V; ultra high-drive; EHD = 0x3.

Fig 22. High-drive pins; typical LOW level output current I_{OL} versus LOW level output voltage V_{OL}

Table 32. Dynamic characteristics: Dynamic external memory interface

Simulated data over temperature and process range; C_L = 10 pF for $\overline{EMC\_DYCSn}$, $\overline{EMC\_RAS}$, $\overline{EMC\_CAS}$, $\overline{EMC\_WE}$, EMC_An; C_L = 9 pF for EMC_Dn; C_L = 5 pF for EMC_DQMOUTn, EMC_CLKn, EMC_CKEOUTn; T_{amb} = −40 °C to 105 °C; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V; $V_{DD(IO)}$ = 3.3 V ± 10 %; RD = 1 (see LPC43xx User manual); EMC_CLKn delays CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY = 0.

Symbol	Parameter	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	8.4	-	-	ns
Common to read and write cycles					
$t_{d(DYCSV)}$	dynamic chip select valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DYCS)}$	dynamic chip select hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	4.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(RAS)}$	row address strobe hold time	0.5 + 0.5 × $T_{cy(clk)}$	1.1 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	-	2.9 + 0.5 × $T_{cy(clk)}$	4.6 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CAS)}$	column address strobe hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(WEV)}$	write enable valid delay time	-	3.2 + 0.5 × $T_{cy(clk)}$	5.9 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(WE)}$	write enable hold time	1.3 + 0.5 × $T_{cy(clk)}$	1.4 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(DQMOUTV)}$	DQMOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.0 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(DQMOUT)}$	DQMOUT hold time	0.2 + 0.5 × $T_{cy(clk)}$	0.8 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(AV)}$	address valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.3 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(A)}$	address hold time	0.3 + 0.5 × $T_{cy(clk)}$	0.9 + 0.5 × $T_{cy(clk)}$	-	ns
$t_{d(CKEOUTV)}$	CKEOUT valid delay time	-	3.1 + 0.5 × $T_{cy(clk)}$	5.1 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(CKEOUT)}$	CKEOUT hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns
Read cycle parameters					
$t_{su(D)}$	data input set-up time	−1.5	−0.5	-	ns
$t_{h(D)}$	data input hold time	2.2	0.8	-	ns
Write cycle parameters					
$t_{d(QV)}$	data output valid delay time	-	3.8 + 0.5 × $T_{cy(clk)}$	6.2 + 0.5 × $T_{cy(clk)}$	ns
$t_{h(Q)}$	data output hold time	0.5 × $T_{cy(clk)}$	0.7 + 0.5 × $T_{cy(clk)}$	-	ns

Table 33. Dynamic characteristics: Dynamic external memory interface; EMC_CLK[3:0] delay values

T_{amb} = −40 °C to 105 °C; $V_{DD(IO)}$ = 3.3 V ± 10 %; 2.4 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_d	delay time	delay value	[1]				
		CLKn_DELAY = 0		0.0	0.0	0.0	ns
		CLKn_DELAY = 1	[1]	0.4	0.5	0.8	ns
		CLKn_DELAY = 2	[1]	0.7	1.0	1.7	ns
		CLKn_DELAY = 3	[1]	1.1	1.6	2.5	ns
		CLKn_DELAY = 4	[1]	1.4	2.0	3.3	ns
		CLKn_DELAY = 5	[1]	1.7	2.6	4.1	ns
		CLKn_DELAY = 6	[1]	2.1	3.1	4.9	ns
		CLKn_DELAY = 7	[1]	2.5	3.6	5.8	ns

[1] Program the EMC_CLKn delay values in the EMCDELAYCLK register (see the *LPC43xx User manual*). The delay values must be the same for all SDRAM clocks EMC_CLKn: CLK0_DELAY = CLK1_DELAY = CLK2_DELAY = CLK3_DELAY.

12. ADC/DAC electrical characteristics

Table 39. ADC characteristics

$V_{DDA(3V3)}$ over specified ranges; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	2	pF
E_D	differential linearity error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[1][2]	-	±0.8	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.0	-	LSB
$E_{L(adj)}$	integral non-linearity	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[3]	-	±0.8	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±1.5	-	LSB
E_O	offset error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[4]	-	±0.15	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.15	-	LSB
E_G	gain error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[5]	-	±0.3	-	%
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±0.35	-	%
E_T	absolute error	2.7 V ≤ $V_{DDA(3V3)}$ ≤ 3.6 V	[6]	-	±3	-	LSB
		2.4 V ≤ $V_{DDA(3V3)}$ < 2.7 V		-	±4	-	LSB
R_{vsi}	voltage source interface resistance	see Figure 42		-	-	$1/(7 \times f_{clk(ADC)} \times C_{ia})$	kΩ
R_i	input resistance		[7][8]	-	-	1.2	MΩ
$f_{clk(ADC)}$	ADC clock frequency			-	-	4.5	MHz
f_s	sampling frequency	10-bit resolution; 11 clock cycles		-	-	400	kSamples/s
		2-bit resolution; 3 clock cycles				1.5	MSamples/s

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 41.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 41.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 41.

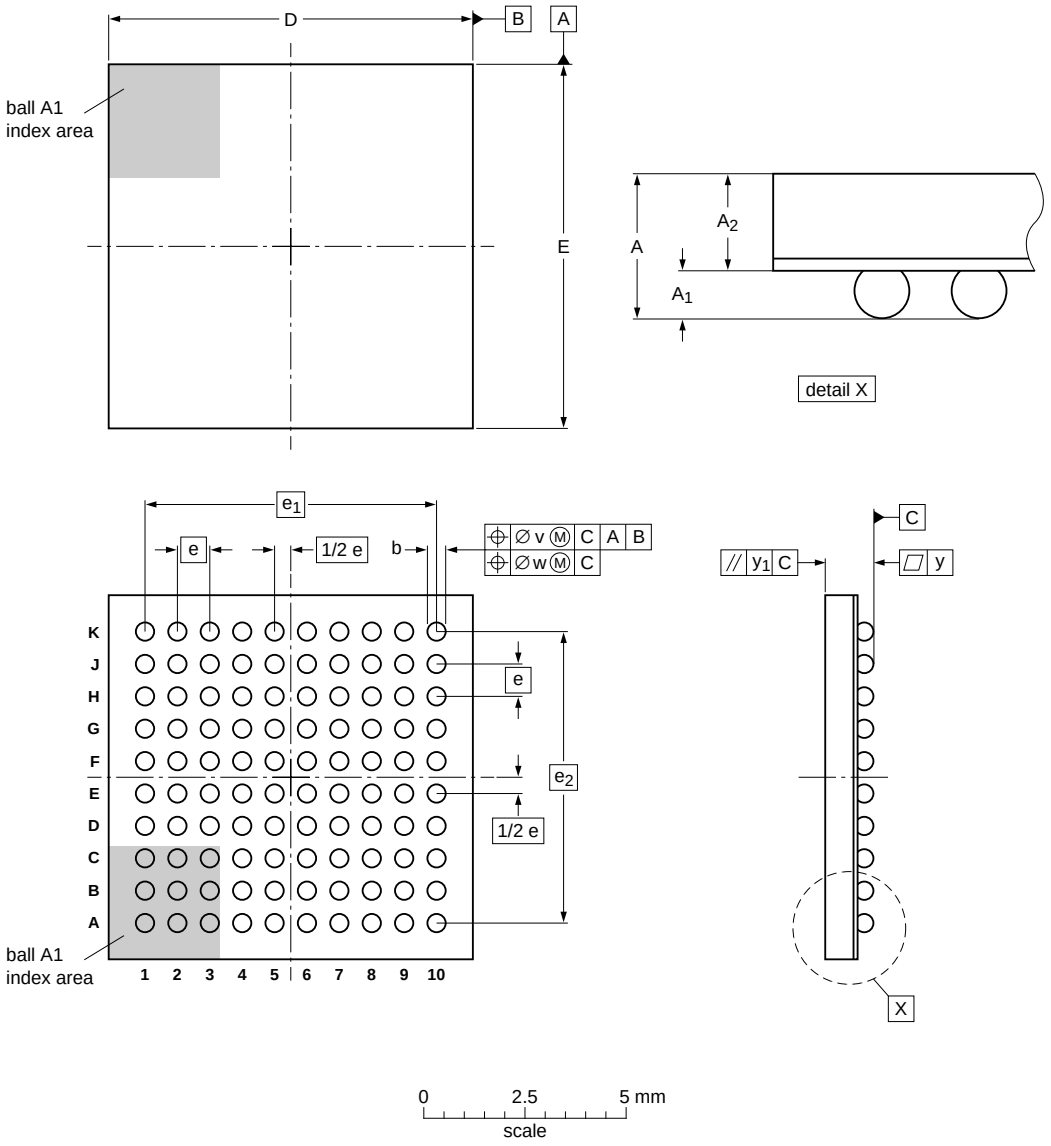
[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 41.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 41.

[7] T_{amb} = 25 °C.

[8] Input resistance R_i depends on the sampling frequency fs: $R_i = 2\ k\Omega + 1 / (f_s \times C_{ia})$.

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 53. Package outline of the TFBGA100 package

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Parameter t_{ret} (retention time) for EEPROM updated in Table 15. • SGPIO and SPI location corrected in Figure 1. • SGPIO-to-DMA connection updated in Figure 6. • Parameter $V_{DDA(3V3)}$ added for pins USB0_VDDA3V3_DRIVER and USB0_VDDA3V3 in Table 11. • Parameter name $I_{DD(ADC)}$ changed to I_{DDA} in Table 11. • Minimum wake-up time from sleep mode added in Table 16. • Data for $I_{DD(IO)}$ added in Table 11. • Corrected max voltage on pins USB0_DP, USB0_DM, USB0_VBUS, USB1_DP, and USB1_DM in Table 7 and Table 11 to be consistent with USB specifications. • SPI and SGPIO peripheral power consumption added in Table 12. • SPI timing characteristics added. See Section 11.12. • SGPIO timing characteristics added. See Section 11.15. • Data sheet status changed to Product data sheet. • Conditions RPHASE1 and RPHASE2 corrected in Table 15 “EEPROM characteristics”. RPHASE1: t_{wait} > 70 ns. RPHASE2: t_{wait} > 35 ns. • $I_{DD(REG)(3V3)}$ updated in Table 11 “Static characteristics” for the following conditions: – Active mode: CCLK = 12 MHz; $I_{DD(REG)(3V3)}$ changed from 9.3 mA to 10 mA. – Active mode: CCLK = 60 MHz; $I_{DD(REG)(3V3)}$ changed from 26 mA to 28 mA. – Active mode: CCLK = 120 MHz; $I_{DD(REG)(3V3)}$ changed from 46 mA to 51 mA. – Active mode: CCLK = 180 MHz; $I_{DD(REG)(3V3)}$ changed from 66 mA to 74 mA. – Active mode: CCLK = 204 MHz; $I_{DD(REG)(3V3)}$ changed from 75 mA to 83 mA. – Sleep mode: CCLK = 12 MHz; $I_{DD(REG)(3V3)}$ changed from 6.2 mA to 8.8 mA. • Power consumption data in Figure 11 to Figure 14 updated. • IRC specifications corrected in Table 19 “Dynamic characteristic: IRC oscillator”. Accuracy changed to +/- 3 % over the entire temperature range. • SPIFI timing diagram corrected and specified for mode 0. See Table 27. • Table 21 “Dynamic characteristic: I/O pins[1]” added. • Parameter C_I corrected for high-drive pins (changed from 2 pF to 5.2 pF). See Table 11. • Internal pull-up resistor configuration added for $\overline{\text{RESET}}$, WAKEUPn, and ALARM pins. See Table 3. • Description of DEBUG pin updated. • Input range for PLL1 corrected: 1 MHz to 25 MHz. See Section 7.23.7 “System PLL1”. • Signal polarity of EMC_CKEOUT and EMC_DQMOUT corrected. Both signals are active HIGH. • SPIFI output timing parameters in Table 27 corrected to apply to Mode 0: – $t_{v(Q)}$ changed to 3.2 ns. – $t_{h(Q)}$ changed to 0.2 ns,		

Table 47. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC4357_53_37_33 v.2	20120711	Preliminary data sheet	-	LPC4357_53 v.1
Modifications:	• Data sheet status changed to preliminary. • Parts LPC4337 and LPC4333 added. • Minimum value of V_I for conditions “USB0 pins USB0_DP; USB0_DM; USB0_VBUS”, “USB0 pins USB0_ID; USB0_RREF”, and “USB1 pins USB1_DP and USB1_DM” changed to −0.3 V in Table 6. • Section 10.2 added. • Table 8 “Thermal resistance (LQFP packages)” and Table 9 “Thermal resistance value (BGA packages)” added. • AES removed. Available on parts LPC43Sxx only. • Dynamic characteristics of the SD/MMC controller updated in Table 30. • Dynamic characteristics of the LCD controller updated in Table 31. • Dynamic characteristics of the SSP controller updated in Table 23. • Parameters I_{IL} and I_{IH} renamed to I_{LL} and I_{LH} in Table 10.			
LPC4357_53 v.1	20120604	Objective data sheet	-	-

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP B.V.

20. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

7.23.5 PLL0USB (for USB0) 84
7.23.6 PLL0AUDIO (for audio) 84
7.23.7 System PLL1 85
7.23.8 Reset Generation Unit (RGU) 85
7.23.9 Power Management Controller (PMC) 85
7.23.10 Power control 86
7.23.11 Code security (Code Read Protection - CRP) 87
7.24 Serial Wire Debug/JTAG 88
8 Limiting values 89
9 Thermal characteristics 90
10 Static characteristics 91
10.1 Power consumption 98
10.2 Peripheral power consumption 101
10.3 Electrical pin characteristics 103
10.4 BOD and band gap static characteristics . . . 107
11 Dynamic characteristics 108
11.1 Flash/EEPROM memory 108
11.2 Wake-up times 109
11.3 External clock for oscillator in slave mode . . 109
11.4 Crystal oscillator 110
11.5 IRC oscillator 110
11.6 RTC oscillator 110
11.7 GPCLKIN 111
11.8 I/O pins 111
11.9 I^2C-bus 112
11.10 I^2S-bus interface 113
11.11 USART interface 114
11.12 SSP interface 116
11.13 SPI interface 119
11.14 SSP/SPI timing diagrams 120
11.15 SPIFI 122
11.16 SGPIO timing 122
11.17 External memory interface 124
11.18 USB interface 129
11.19 Ethernet 130
11.20 SD/MMC 132
11.21 LCD 132
12 ADC/DAC electrical characteristics 133
13 Application information 136
13.1 LCD panel signal usage 136
13.2 Crystal oscillator 138
13.3 RTC oscillator 140
13.4 XTAL and RTCX Printed Circuit Board (PCB) layout guidelines 140
13.5 Standard I/O pin configuration 140
13.5.1 Reset pin configuration 141
13.5.2 Suggested USB interface solutions 141
14 Package outline 144
15 Soldering 148
16 Abbreviations 152
17 References 153
18 Revision history 154
19 Legal information 159
19.1 Data sheet status 159
19.2 Definitions 159
19.3 Disclaimers 159
19.4 Trademarks 160
20 Contact information 160
21 Contents 161

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 March 2016
Document identifier: LPC435X_3X_2X_1X