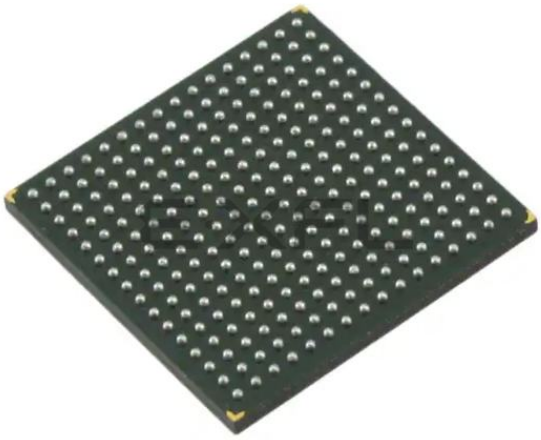
Renesas Electronics America Inc - IDT79RC32T365-150BC Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t365-150bc

- *Optimized for IPSec AH, ESP, and AH+ESP (single MAC) tunnel and transport mode processing: initialization Vector (IV) insertion and extraction, HMAC checking, AH mutable field processing for both IPv4 and IPv6 packets, IPSec pad generation and checking*

◆ Random Number Generator
- *True hardware random number generator suitable for security applications: may be used to generate symmetric and public keys, initialization vectors, and nonces*
- *Dedicated DMA engine for transferring random numbers to memory*
- *Generates random numbers at a bit rate equal to IPBus clock frequency divided by 32*
- *Provides 4 word (16 byte) FIFO to queue random numbers*
- *Randomness tester continually verifies proper operation of random number generator using a randomness test defined in FIPS 140-2*

◆ PCI Interface
- *32-bit PCI revision 2.2 compliant*
- *Supports host or satellite operation in both master and target modes*
- *PCI clock: supports frequencies from 16 MHz to 66 MHz, PCI clock may be asynchronous to master clock (CLK)*
- *PCI arbiter in Host mode: supports 3 external masters, fixed priority or round robin arbitration*
- *I_2O "like" PCI Messaging Unit*

◆ Two Ethernet Interfaces
- *10 and 100 Mb/s ISO/IEC 8802-3:1996 compliant*
- *Two IEEE 802.3u compatible Media Independent Interfaces (MII) with serial management interface*
- *MII supports IEEE 802.3u auto-negotiation speed selection*
- *Supports 64 entry hash table based multicast address filtering*
- *512 byte transmit and receive FIFOs*
- *Supports flow control functions outlined in IEEE Std. 802.3x-1997*

◆ SDRAM Controller
- *Supports up to 512 MB of memory*
- *2 chip selects (each supports 2 or 4 banks internal SDRAM banks)*
- *32-bit data width, supports 8/16/32-bit width devices*
- *Supports 16Mb, 64Mb, 128Mb, and 256Mb, and 512Mb devices*
- *Automatic refresh generation*

◆ Memory and Peripheral Device Controller
- *Provides "glueless" interface to standard SRAM, Flash, ROM, dual-port memory, and peripheral devices*
- *Provides "glueless" interface to many 16-bit PCMCIA devices*
- *Demultiplexed address and data buses: 32-bit data bus, 26-bit address bus, 6 chip selects, control for external data bus buffers*
- *Supports 8-bit, 16-bit, and 32-bit width devices: automatic byte gathering and scattering*
- *Flexible protocol configuration parameters: programmable number of wait states (0 to 63), programmable postread/post-write delay (0 to 31), supports external wait state generation, supports Intel and Motorola style peripherals*
- *Write protect capability per chip select*
- *Programmable bus transaction timer generates warm reset when counter expires*
- *Supports up to 64MB of memory per chip select*

◆ DMA Controller
- *9 DMA channels: two channels for each of the two Ethernet interfaces (transmit/receive), two channels for PCI (PCI to Memory and Memory to PCI), two channels for security engine (input/output), one channel for the hardware random number generator*
- *Provides flexible descriptor based operation*
- *Supports unaligned transfers (i.e., source or destination address may be on any byte boundary) with arbitrary byte length*

◆ General Purpose Peripherals
- *Serial port compatible with 16550 Universal Asynchronous Receiver Transmitter (UART)*
- *Three general purpose 32-bit counter/timers*
- *Interrupt Controller*
- *Serial Peripheral Interface (SPI) supporting host mode*
- *16 general purpose I/O (GPIO) pins which can be configured as interrupt sources*

◆ System Features
- *JTAG Interface (IEEE Std. 1149.1 compatible)*
- *256 pin CABGA package*
- *2.5V core supply and 3.3V I/O supply*

CPU Execution Core

The RC32365 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The instruction set is largely compatible with the MIPS32 instruction set, allowing the customer to select from a broad range of software and development tools. Cache locking guarantees real-time performance by holding critical code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

Security Engine

The RC32365 incorporates an on-chip security engine that has been designed to accelerate IPSec performance and minimize the amount of performance required by the CPU to process secure packet traffic. The engine includes hardware support for the DES, 3DES, and AES encryption algorithms and the MD5 and SHA1 hash functions. The engine also supports hardware-assisted packet processing for the various modes of IPSec, including AH, ESP, and AH+ESP tunnel and transport modes. Two dedicated DMA channels are used to transfer data to and from the security engine, allowing the CPU to work on other tasks during this time.

Signal	Type	Name/Description
General Purpose I/O		
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and Peripheral bus address bit 22 (output).
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and Peripheral bus address bit 23 (output).
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and Peripheral bus address bit 24 (output).
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and Peripheral bus address bit 25 (output).
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. The value of this pin may be used as a Counter Timer Clock input.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: SDCKENP Alternate function: SDRAM clock enable output The value of this pin may be used as a Counter Timer Clock input.
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: CEN1 Alternate function: PCMCIA chip enable 1 (CE1#) (output).
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: CEN2 Alternate function: PCMCIA chip enable 2 (CE2#) (output).
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: REGN Alternate function: PCMCIA Attribute Memory Select (REG#) (output).
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IORDN Alternate function: PCMCIA IO Read (IORD#) (output).
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOWRN Alternate function: PCMCIA IO Write (IOWR#) (output).
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[2] Alternate function: PCI bus request 2 (output).
GPIO[14]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[2] Alternate function: PCI bus grant 2 (output).

Table 1 Pin Description (Part 2 of 6)

Signal	Type	Name/Description
PCIREQN[1:0]	I/O	PCI Bus Request. In PCI host mode with internal arbiter: These signals are inputs whose assertion indicates to the internal RC32365 arbiter that an agent desires ownership of the PCI bus. In PCI host mode with external arbiter: PCIREQN[0]: asserted by the RC32365 to request ownership of the PCI bus. PCIREQN[1]: unused and driven high. In PCI satellite mode: PCIREQN[0]: this signal is asserted by the RC32365 to request ownership of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions.
PCIRSTN	I/O	PCI Reset. In host mode, this signal is asserted by the RC32365 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	PCI System Error. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	PCI Stop. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	PCI Target Ready. Driven by the bus target to indicate that the current data can complete.
Ethernet Interface		
MII0CL	I	Ethernet 0 MII Collision Detected. This signal is asserted by the ethernet PHY when a collision is detected.
MII0CRS	I	Ethernet 0 MII Carrier Sense. This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII0RXCLK	I	Ethernet 0 MII Receive Clock. This clock is a continuous clock that provides a timing reference for the reception of data.
MII0RXD[3:0]	I	Ethernet 0 MII Receive Data. This nibble wide data bus contains the data received by the ethernet PHY.
MII0RXDV	I	Ethernet 0 MII Receive Data Valid. The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MII0RXER	I	Ethernet 0 MII Receive Error. The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MII0TXCLK	I	Ethernet 0 MII Transmit Clock. This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MII0TXD[3:0]	O	Ethernet 0 MII Transmit Data. This nibble wide data bus contains the data to be transmitted.
MII0TXENP	O	Ethernet 0 MII Transmit Enable. The assertion of this signal indicates that data is present on the MII for transmission.
MII0TXER	O	Ethernet 0 MII Transmit Coding Error. When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MII1CL	I	Ethernet 1 MII Collision Detected. This signal is asserted by the ethernet PHY when a collision is detected.
MII1CRS	I	Ethernet 1 MII Carrier Sense. This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII1RXCLK	I	Ethernet 1 MII Receive Clock. This clock is a continuous clock that provides a timing reference for the reception of data.

Table 1 Pin Description (Part 4 of 6)

Signal	Type	Name/Description
Miscellaneous		
CLK	I	Master Clock. This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations except those associated with SDRAMs.
COLDRSTN	I	Cold Reset. The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	Reset. The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32365 during a warm reset. It can also be asserted by an external device to force the RC32365 to take a warm reset exception.

Table 1 Pin Description (Part 6 of 6)

Pin Characteristics

Pin Name	Type	Buffer	I/O Type	Internal Resistor	External Resistor[1]
Memory and Peripheral Bus					
BDIRN	O	LVTTL	High Drive		
BOEN[1:0]	O	LVTTL	High Drive		
BWEN[3:0]	O	LVTTL	High Drive		
CSN[5:0]	O	LVTTL	High Drive		
MADDR[21:0]	O	LVTTL	High Drive		
MDATA[31:0]	I/O	LVTTL	High Drive		
OEN	O	LVTTL	High Drive		
RWN	O	LVTTL	High Drive		
WAITACKN	I	LVTTL	STI[2]	pull-up	
RASN	O	LVTTL	High Drive		
CASN	O	LVTTL	High Drive		
SDCSN[1:0]	O	LVTTL	High Drive		
SDWEN	O	LVTTL	High Drive		
SDCLKOUT	O	LVTTL	High Drive		
SDCLKINP	I	LVTTL	STI	pull-up	
General Purpose I/O					
GPIO[15:13]	I/O	PCI	PCI		
GPIO[12:0]	I/O	LVTTL	Low Drive	pull-up	
Serial Interface					
SCK	I/O	LVTTL	Low Drive	pull-up	pull-up on board
SDI	I/O	LVTTL	Low Drive	pull-up	pull-up on board
SDO	I/O	LVTTL	Low Drive	pull-up	pull-up on board
PCI Bus Interface					
PCIAD[31:0]	I/O	PCI	PCI		
PCICBEN[3:0]	I/O	PCI	PCI		
PCICLK	I	PCI	PCI		
PCIDEVSELN	I/O	PCI	PCI		pull-up on board

Table 2 Pin Characteristics (Part 1 of 2)

Boot Configuration Vector

The boot configuration vector is read into the RC32365 during cold reset. The vector defines parameters in the RC32365 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4.

Signal	Name/Description
MDATA[2:0]	CPU Clock Multiplier. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). 0x0 - Multiply by 2 0x1 - 0x7 — Reserved
MDATA[3]	Endian. This bit specifies the endianness. 0x0 - little endian 0x1 - big endian
MDATA[4]	Reserved. This pin may be driven high or low during boot configuration and its state is recorded in the Boot Configuration Vector (BCV) field of the BCV register. This reserved bit may be used to pass boot configuration parameters to software.
MDATA[6:5]	Boot Device Width. This field specifies the width of the boot device (i.e., Device 0). 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[7]	Reset Mode. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4096 clock cycles 0x1 - reserved
MDATA[8]	Disable Watchdog Timer. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer is enabled 0x1 - Watchdog timer is disabled
MDATA[11:9]	PCI Mode. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*
MDATA[15:12]	Reserved. These pins may be driven high or low during boot configuration and their state is recorded in the Boot Configuration Vector (BCV) field of the BCV register. These reserved bits may be used to pass boot configuration parameters to software.

Table 3 Boot Configuration Vector Encoding

Logic Diagram

The following Logic Diagram shows the primary pin functions of the RC32365.

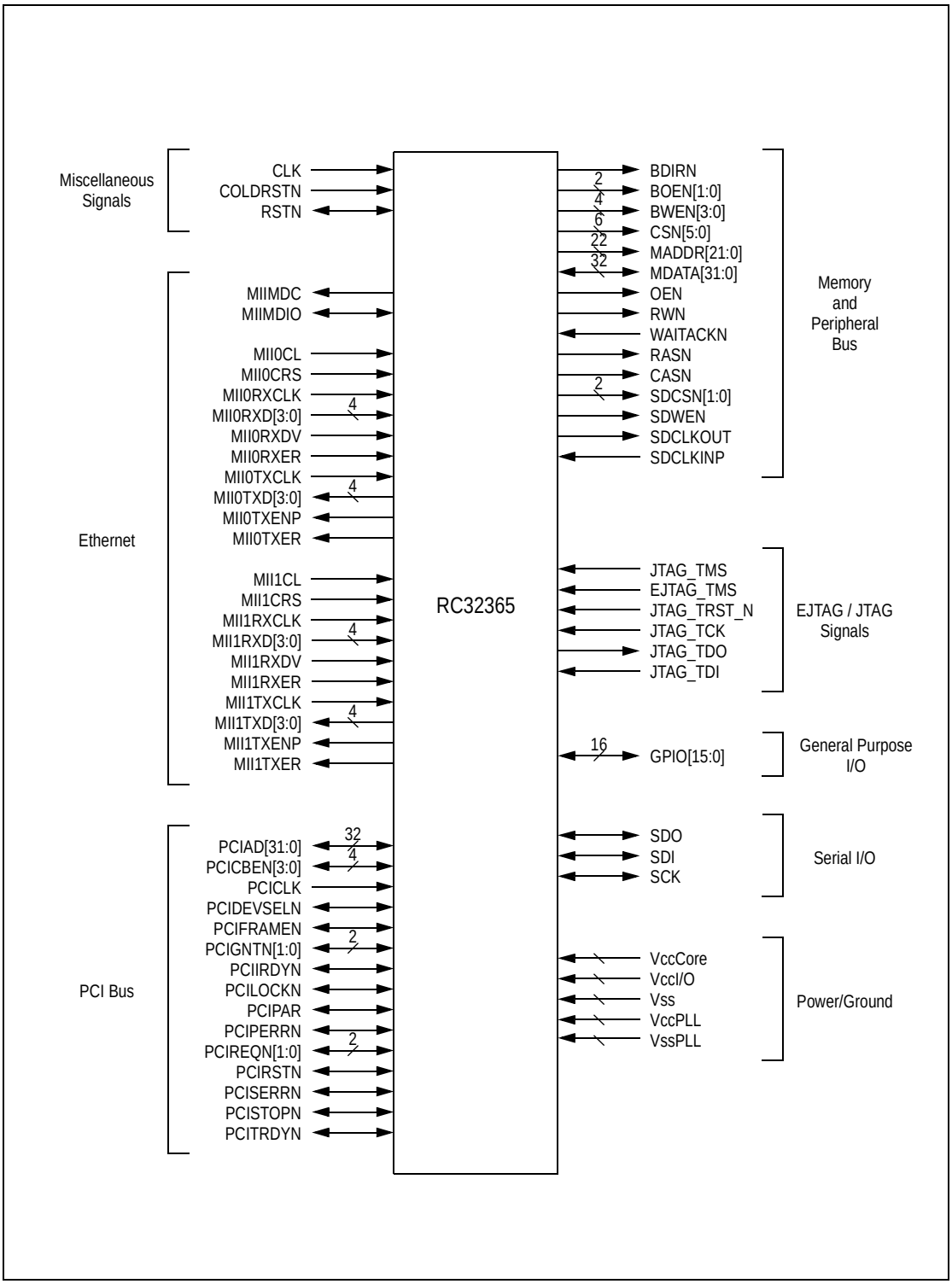


Figure 1 RC32365 Logic Diagram

Clock Parameters

The values given below are based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 14 and 15.

Parameter	Symbol	Reference Edge	150MHz		Units	Timing Diagram Reference
			Min	Max		
PCLK[1]	Frequency	none	100	150	MHz	See Figure 3
CLK[2,3]	Frequency	none	50	75	MHz	
	Tper_5a		13.3	20	ns	
	Thigh_5a, Tlow_5a		40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	ns	
	Tjitter_5a		—	± 250	ps	

Table 5 RC32365 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3).
2. Ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be less than or equal to 1/2 CLK frequency.
3. PCI clock (PCICLK) frequency must be less than or equal to two times CLK.

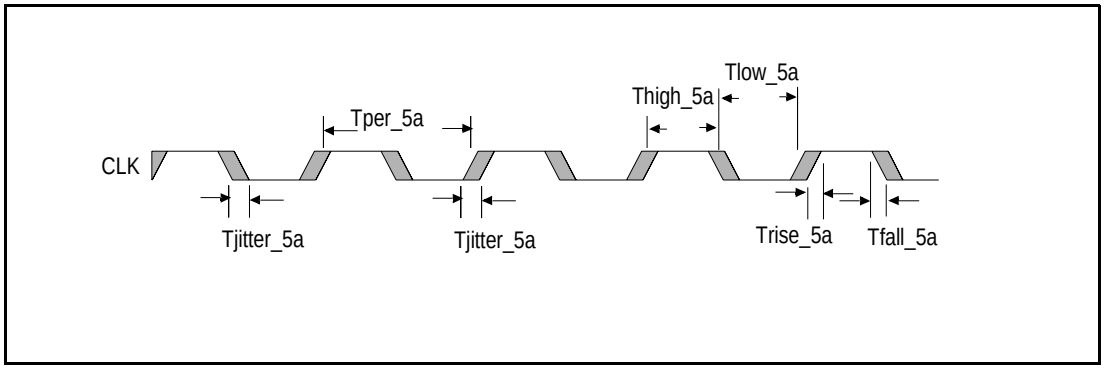
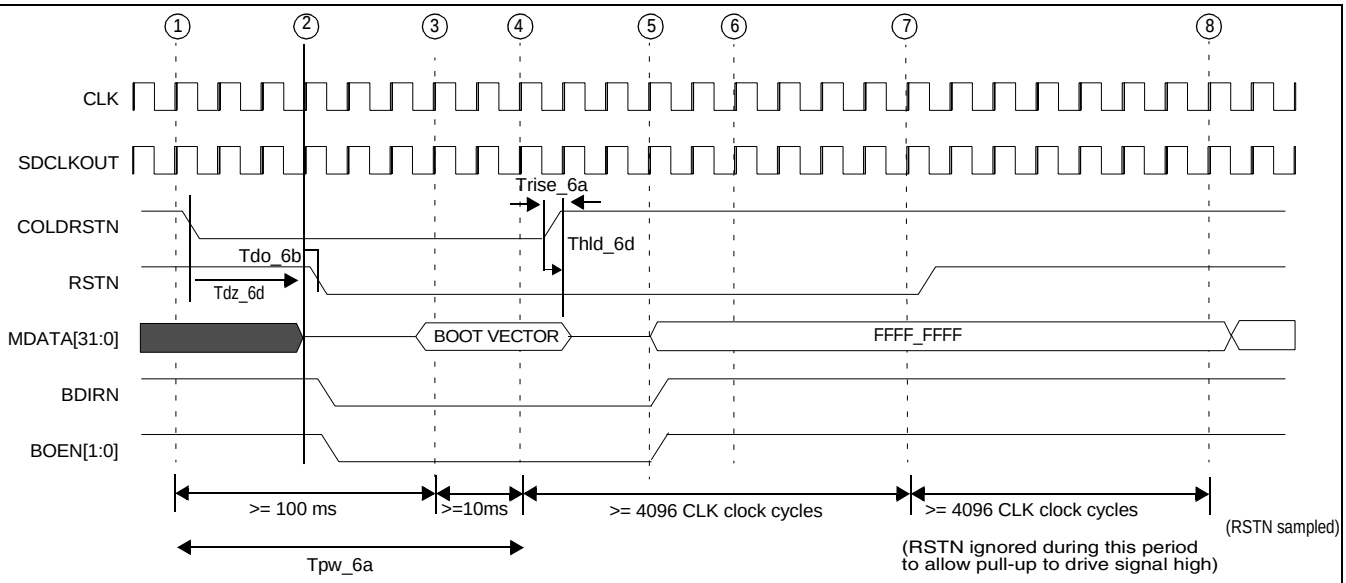
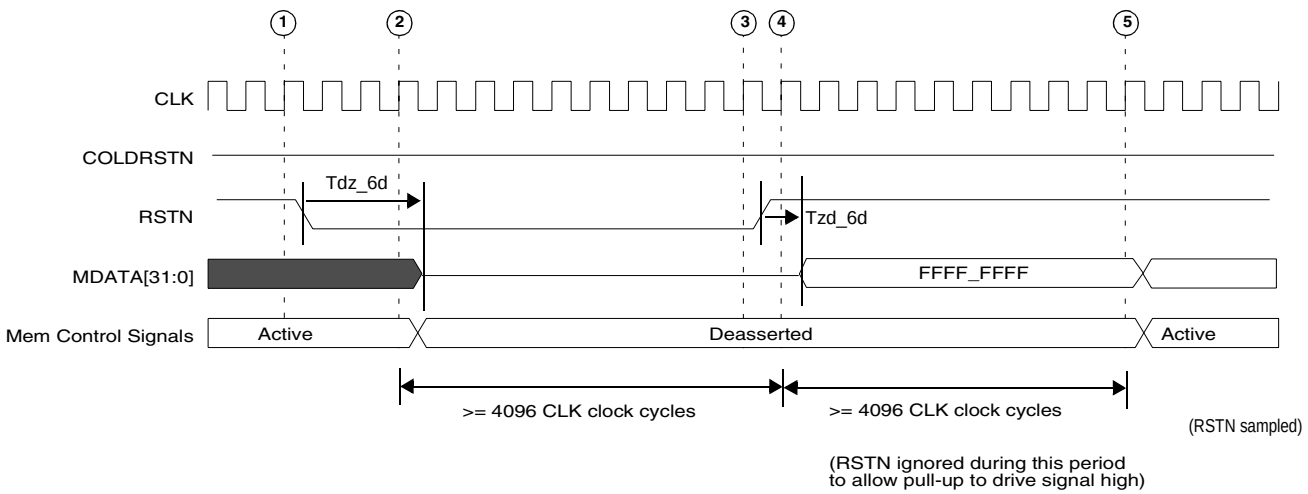


Figure 3 Clock Parameters Waveform



1. COLDRSTN asserted by external logic.
2. RC32365 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32365 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32365 stops sampling the boot configuration vector.
5. The RC32365 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLK may be held constant after this point if Hold SYSCLK Constant is selected in the boot configuration vector.
7. RSTN negated by the RC32365.
8. CPU begins executing by taking MIPS reset exception, and the RC32365 starts sampling RSTN as a warm reset input.

Figure 4 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32365 asserts RSTN output low in response.
2. The RC32365 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32365 deasserts RSTN.
4. The RC32365 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 5 Warm Reset AC Timing Waveform

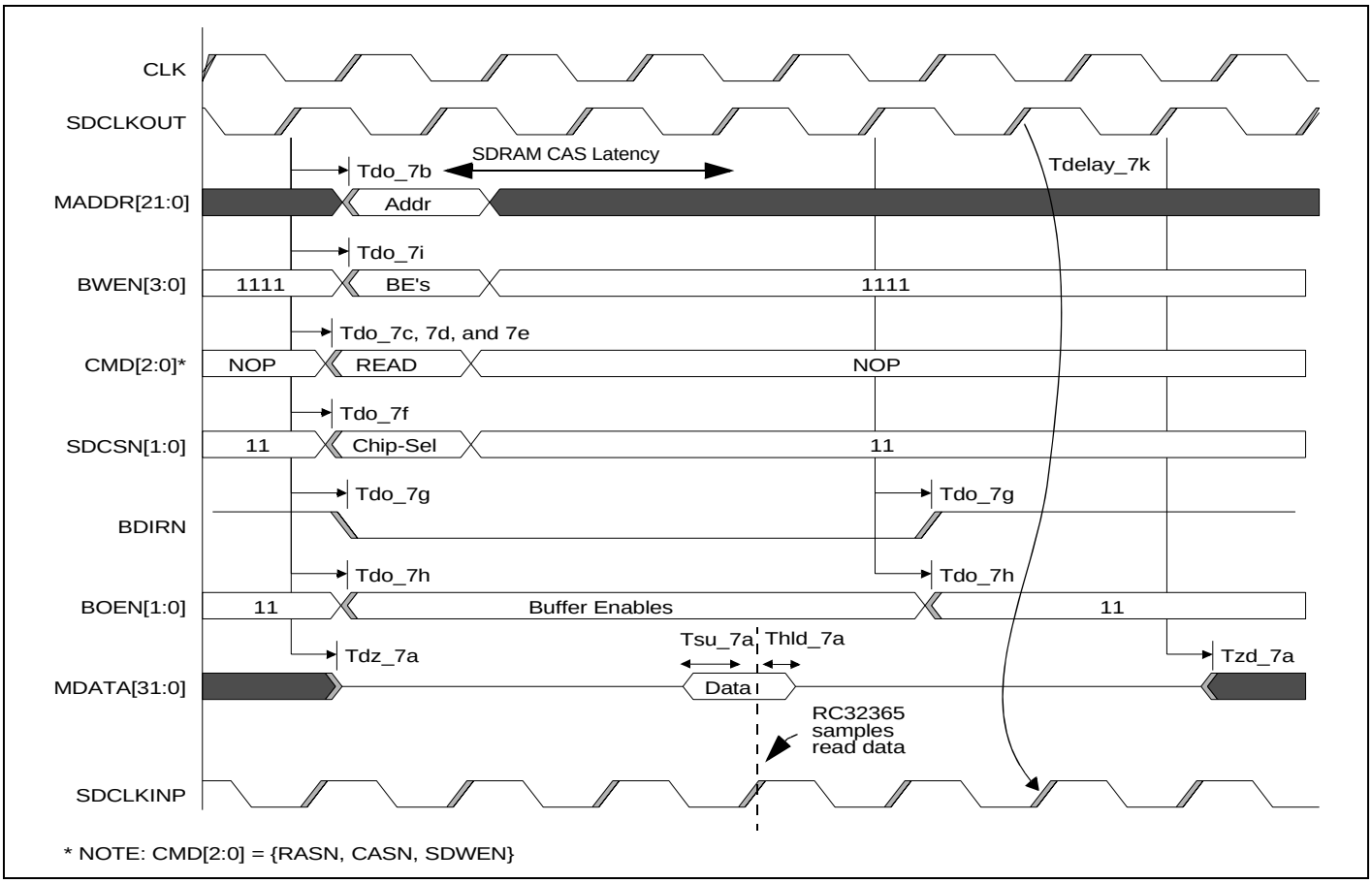


Figure 6 Memory and Peripheral Bus AC Timing Waveform - SDRAM Read Access

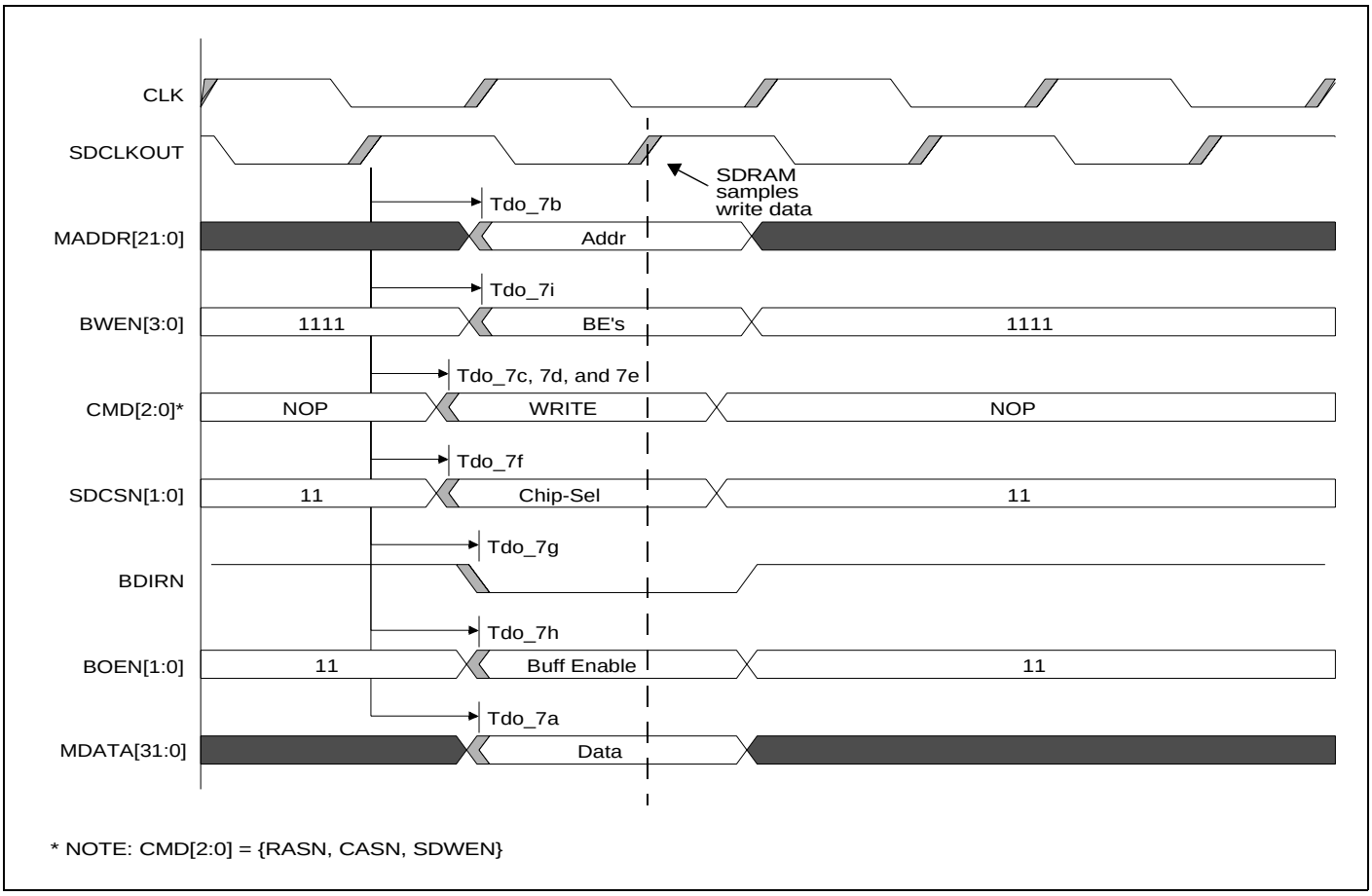


Figure 7 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

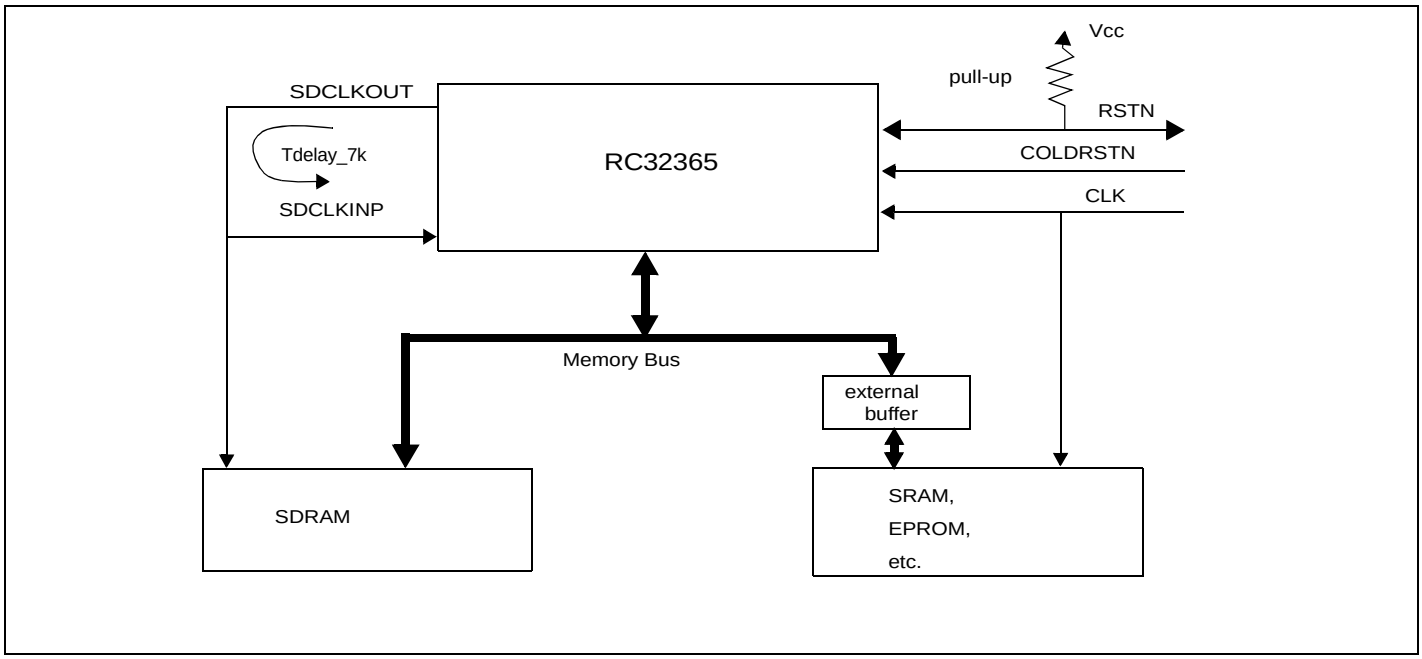


Figure 8 SDCLKOUT - SDCLKINP Relationship

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
Memory and Peripheral Bus[1] — Device Access							
MDATA[31:0]	Tsu_8a	CLK rising	2.5	—	ns		See Figures 9 and 10
	Thld_8a		1.0	—	ns		
	Tdo_8a		2.0	6.5	ns		
	Tdz_8a[2]		2.0	9.5	ns		
	Tzd_8a[2]		2.0	10.5	ns		
MADDR[21:0]	Tdo_8b	CLK rising	2.0	6.5	ns		
MADDR[25:22]	Tdo_8c	CLK rising	3.0	7.5	ns		
CSN[5:0]	Tdo_8d	CLK rising	2.0	6.5	ns		
RWN	Tdo_8e	CLK rising	2.0	6.5	ns		
OEN	Tdo_8f	CLK rising	2.0	6.5	ns		
BWEN[1:0]	Tdo_8g	CLK rising	2.0	6.5	ns		
BDIRN	Tdo_8h	CLK rising	2.0	6.5	ns		
BOEN[1:0]	Tdo_8i	CLK rising	2.0	6.5	ns		
WAITACKN[3]	Tsu_8j	CLK rising	2.0	—	ns		
	Thld_8j		0.5	—	ns		
	Tpw_8j[2]	none	2(CLK)	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics — Device Access (Part 1 of 2)

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
CEN1[4], CEN2[4]	Tdo_8k	CLK rising	3.0	7.5	ns		See Figures 9 and 10 (cont.)
REGN[4]	Tdo_8l	CLK rising	3.0	7.5	ns		
IORDN[4]	Tdo_8m	CLK rising	3.0	7.5	ns		
IOWRN[4]	Tdo_8n	CLK rising	3.0	7.5	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics — Device Access (Part 2 of 2)

1. The RC32365 provides bus turnaround cycles to prevent bus contention when going from a read to write and write to read. For example, there are no cycles where an external device and the RC32365 are both driving. See Chapter 6, Device Controller, in the RC32365 User Reference Manual.

2. The values for this symbol were determined by calculation, not by testing.

3. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

4. CEN1, CEN2, REGN, IORDN, and IOWRN are alternate functions of GPIO[12:8].

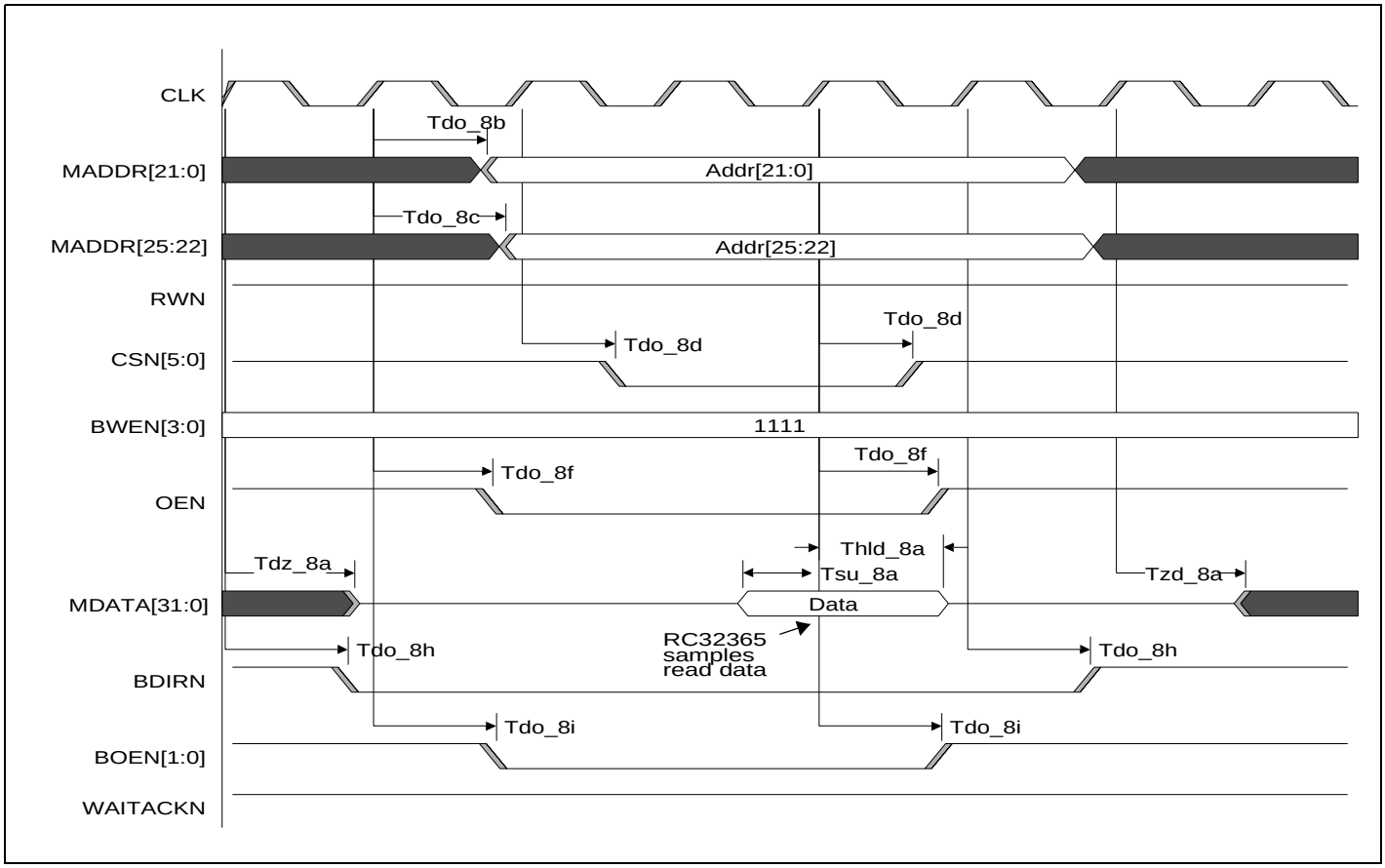


Figure 9 Memory and Peripheral Bus AC Timing Waveform - Device Read Access

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
Ethernet[1]							
MIIMDC	Tper_9a	None	53.3	—	ns		See Figure 11
	Thigh_9a, Tlow_9a		23.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	ns		
	Thld_9b		1.0	—	ns		
	Tdo_9b		1(ICLK)	3(ICLK)	ns		
MIIxRXCLK, MIIxTX-CLK[2]	Tper_9c	None	399.96	400.4	ns	10 Mbps	
	Thigh_9c, Tlow_9c		140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	ns		
MIIxRXCLK, MIIxTXCLK[2]	Tper_9d	None	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	ns		
MIIxRXD[3:0], MIIxRXDV, MIIxRXER	Tsu_9e	MIIxRXCLK rising	3.0	—	ns		
	Thld_9e		2.0	—	ns		
MIIxTXD[3:0], MIIxTXENP, MIIxTXER	Tdo_9f	MIIxTXCLK rising	5.0	13	ns		

Table 9 Ethernet AC Timing Characteristics

1. There are two MII interfaces and the timing is the same for each. “x” represents interface 0 or 1 (For example, MIIxRXCLK can be either MII0RXCLK or MII1RXCLK).

2. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 CLK (MIIxRXCLK and MIIxTXCLK <= 1/2(CLK)).

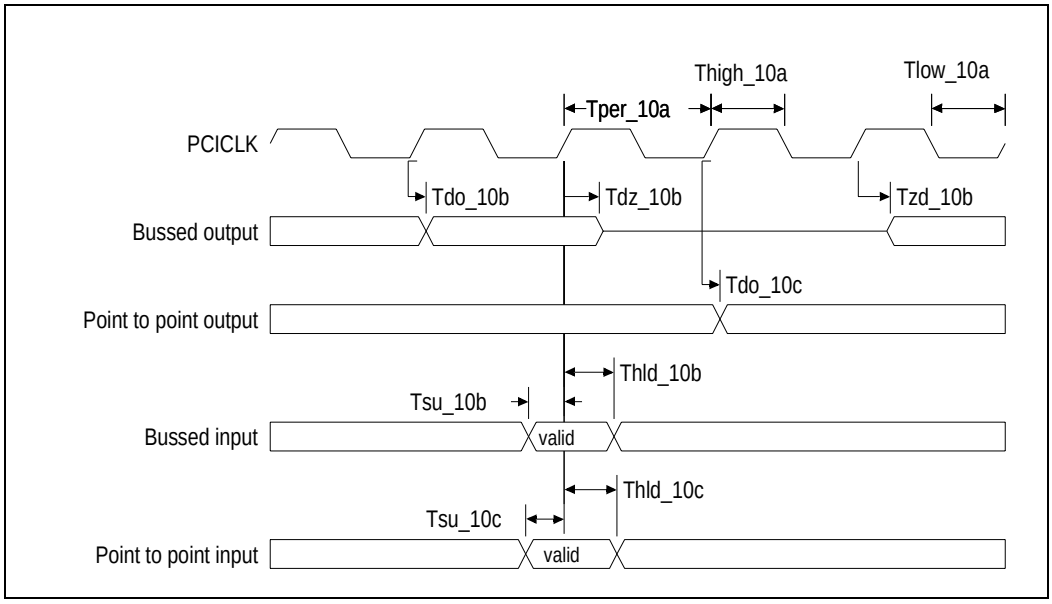


Figure 12 PCI AC Timing Waveform

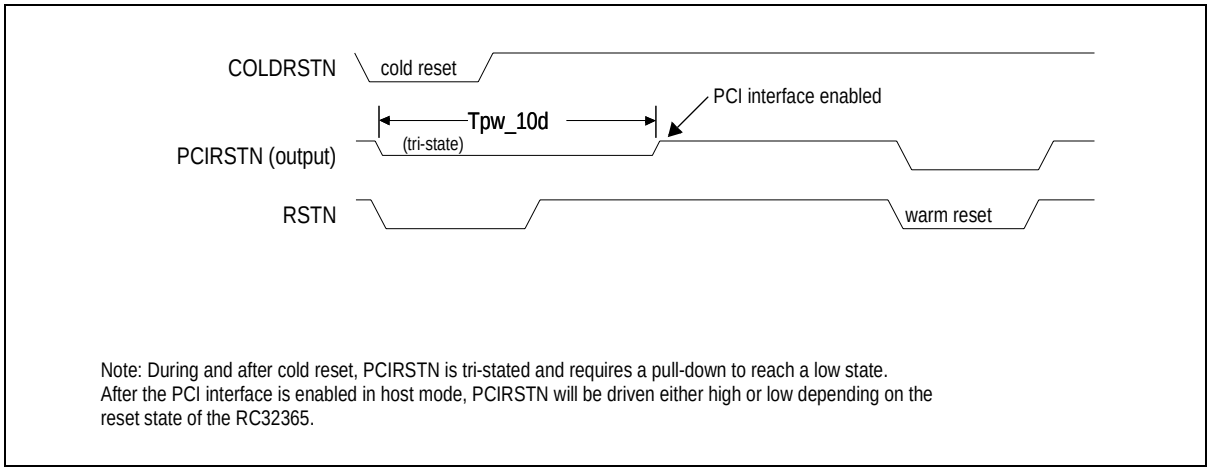


Figure 13 PCI AC Timing Waveform — PCI Reset in Host Mode

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
EJTAG and JTAG							
JTAG_TCK	Tper_14a	none	100	—	ns		See Figure 20
	Thigh_14a, Tlow_14a		40	—	ns		
	Trise_14a, Tfall_14a		—	5.0	ns		
JTAG_TDI	Tsu_14b	JTAG_TCK rising	4.0	—	ns		
	Thld_14b		4.0	—	ns		
JTAG_TMS	Tsu_14c		4.0	—	ns		
	Thld_14c		4.0	—	ns		
EJTAG_TMS	Tsu_14d		4.0	—	ns		
	Thld_14d		4.0	—	ns		
JTAG_TDO	Tdo_14e	JTAG_TCK falling	—	12.5	ns		
	Tdz_14e[1]		—	15.0	ns		
JTAG_TRST_N	Tpw_14f[1]	none	100	—	ns		
VSENSE	Trise_16f	none	—	2	sec	Measured from 0.5V (T_{active})	See Figure 22

Table 13 EJTAG/JTAG AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

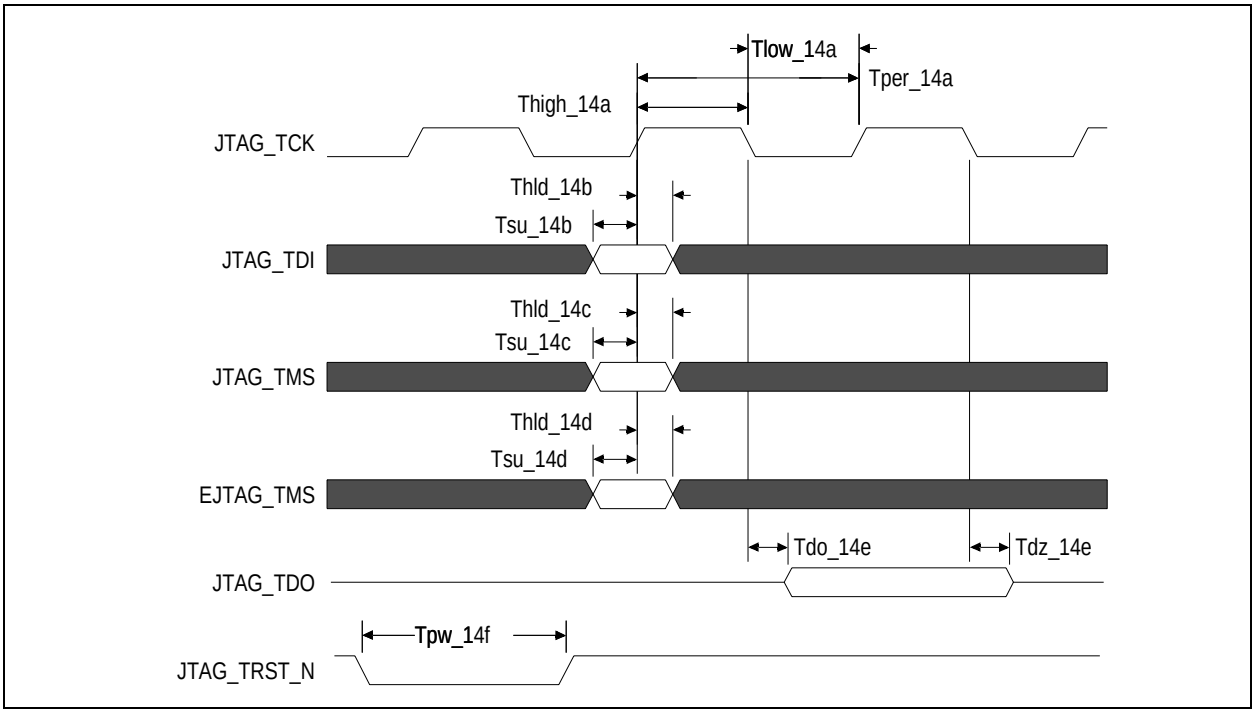


Figure 20 EJTAG/JTAG AC Timing Waveform

Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

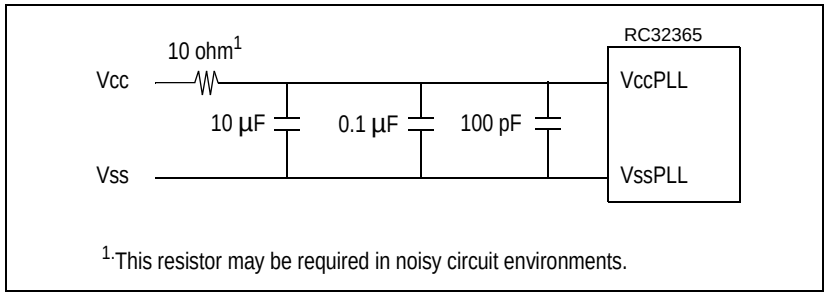


Figure 24 PLL Filter Circuit for Noisy Environments

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{ss}	Common ground	0	0	0	V
V_{ss}PLL	PLL ground				
V_{cc}I/O	I/O supply	3.135	3.3	3.465	
V_{cc}Core	Internal logic supply	2.375	2.5	2.625	
V_{cc}PLL	PLL supply				

Table 14 RC32365 Operating Supply Voltages

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C+ 70°C Ambient
Industrial	-40°C+ 85°C Ambient

Table 15 RC32365 Operating Temperature

Capacitive Load Deration

Refer to the RC32365 IBIS Model which can be found at the IDT web site (www.idt.com).

Power-on RampUp

The 2.5V V_{cc}Core and V_{cc}PLL supplies can be fully powered without the 3.3V V_{cc}I/O supply. However, the V_{cc}I/O supply cannot exceed the V_{cc}Core and V_{cc}PLL supplies by more than 1 volt during power up. A sustained large power difference could potentially damage the part. Inputs should not be driven until the part is fully powered. Specifically, the input high voltages should not be applied until the V_{cc}I/O supply is powered.

There is no special requirement for how fast V_{cc}I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc}I/O.

Power Curve

The following graph contains a power curve that shows power consumption at various bus frequencies.

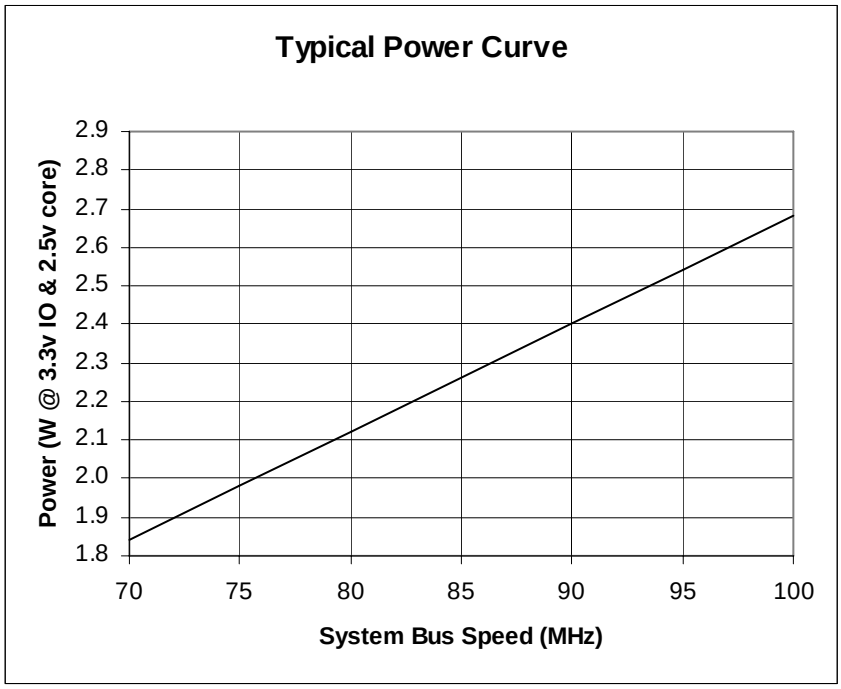


Figure 25 Typical Power Usage

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O Supply Voltage	-0.6	4.0	V
V_{CC}Core	Core Supply Voltage	-0.3	3.0	V
V_{CC}PLL	PLL Supply Voltage	-0.3	3.0	V
Vimin	Input Voltage - undershoot	-0.6	—	V
Vi	I/O Input Voltage	Gnd	V_{CC}I/O+0.6	V
Ta, Industrial	Ambient Operating Temperature	-40	+85	°C
Ta, Commercial	Ambient Operating Temperature	0	+70	°C
Tstg	Storage Temperature	-40	+125	°C

Table 18 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 14. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

Package Pin-out — 256-Pin CABGA

The following table lists the pin numbers and signal names for the RC32365.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	MII0RXD[0]		E1	GPIO[15]	1	J1	PCIGNTN[1]		N1	PCIAD[4]	
A2	MII0RXDV		E2	JTAG_TRST_N		J2	PCIDEVSELN		N2	PCIAD[20]	
A3	MII0RXER		E3	JTAG_TDO		J3	PCIGNTN[0]		N3	PCIAD[19]	
A4	MII0TXCLK		E4	JTAG_TDI		J4	PCIFRAMEN		N4	PCIAD[11]	
A5	MII0TXD[2]		E5	V_{cc}CORE		J5	V_{cc}I/O		N5	PCIAD[13]	
A6	MII0CRS		E6	V_{cc}I/O		J6	V_{ss}		N6	PCIAD[15]	
A7	VssPLL		E7	V_{cc}I/O		J7	V_{ss}		N7	BOEN[0]	
A8	MII1RXCLK		E8	V_{cc}I/O		J8	V_{ss}		N8	CSN[2]	
A9	MII1TXD[2]		E9	V_{cc}I/O		J9	V_{ss}		N9	CSN[3]	
A10	MII1CL		E10	V_{cc}I/O		J10	V_{ss}		N10	RWN	
A11	JTAG_TCK		E11	V_{cc}I/O		J11	V_{ss}		N11	MDATA[1]	
A12	GPIO[9]	1	E12	V_{cc}CORE		J12	V_{cc}I/O		N12	MDATA[3]	
A13	GPIO[5]	1	E13	MADDR[5]		J13	SDWEN		N13	MDATA[12]	
A14	GPIO[3]	1	E14	MADDR[16]		J14	SDCLKINP		N14	MDATA[30]	
A15	GPIO[1]	1	E15	MADDR[17]		J15	BWEN[2]		N15	MDATA[11]	
A16	MADDR[10]		E16	MADDR[6]		J16	BWEN[3]		N16	MDATA[27]	
B1	MII0RXD[3]		F1	GPIO[14]	1	K1	PCICBEN[1]		P1	PCIAD[5]	
B2	MII0RXD[1]		F2	GPIO[13]	1	K2	PCICBEN[2]		P2	PCIAD[21]	
B3	MII0RXCLK		F3	PCITRDYN		K3	PCICBEN[0]		P3	PCIAD[23]	
B4	MII0TXER		F4	PCISTOPN		K4	PCICLK		P4	PCIAD[10]	
B5	MII0TXD[3]		F5	V_{cc}CORE		K5	V_{cc}I/O		P5	PCIAD[28]	
B6	MII0CL		F6	V_{cc}I/O		K6	V_{ss}		P6	PCIAD[30]	
B7	VccPLL		F7	V_{ss}		K7	V_{ss}		P7	BDIRN	
B8	MII1RXDV		F8	V_{ss}		K8	V_{ss}		P8	CSN[1]	
B9	MII1TXD[3]		F9	V_{ss}		K9	V_{ss}		P9	CSN[4]	
B10	MII1CRS		F10	V_{ss}		K10	V_{ss}		P10	WAITACKN	
B11	GPIO[12]	1	F11	V_{cc}I/O		K11	V_{ss}		P11	MDATA[17]	
B12	GPIO[8]	1	F12	V_{cc}CORE		K12	V_{cc}CORE		P12	MDATA[19]	
B13	GPIO[4]	1	F13	MADDR[3]		K13	BWEN[1]		P13	MDATA[5]	
B14	GPIO[2]	1	F14	MADDR[14]		K14	RASN		P14	MDATA[9]	
B15	MADDR[21]		F15	MADDR[15]		K15	CASN		P15	MDATA[10]	
B16	MADDR[20]		F16	MADDR[4]		K16	BWEN[0]		P16	MDATA[26]	
C1	MIIMDC		G1	PCIRSTN		L1	PCIAD[16]		R1	PCIAD[6]	
C2	MIIMDIO		G2	PCISERRN		L2	PCIAD[1]		R2	PCIAD[7]	

Table 19: 256-pin CABGA Package Pin-Out (Part 1 of 2)

RC32365 Power Pins

V_{cc}I/O	V_{cc}I/O	V_{cc}Core	V_{cc}PLL
E6	J5	E5	B7
E7	J12	E12	
E8	K5	F5	
E9	L6	F12	
E10	L11	G5	
E11	M6	K12	
F6	M7	L5	
F11	M8	L12	
G12	M9	M5	
H5	M10	M12	
H12	M11		

Table 20 RC32365 Power Pins

RC32365 Ground Pins

V_{ss}	V_{ss}	V_{ss}	V_{ss}PLL
F7	H7	K6	A7
F8	H8	K7	
F9	H9	K8	
F10	H10	K9	
G6	H11	K10	
G7	J6	K11	
G8	J7	L7	
G9	J8	L8	
G10	J9	L9	
G11	J10	L10	
H6	J11		

Table 21 RC32365 Ground Pins

Package Drawing - page two