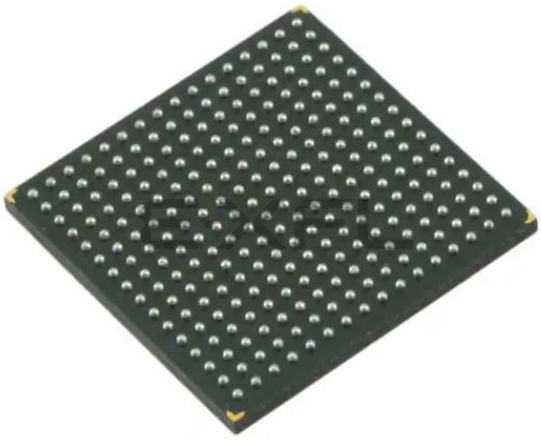
Renesas Electronics America Inc - IDT79RC32T365-150BCG Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (2)
SATA	-
USB	-
Voltage - I/O	2.5V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32t365-150bcg

Signal	Type	Name/Description
General Purpose I/O		
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and Peripheral bus address bit 22 (output).
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and Peripheral bus address bit 23 (output).
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and Peripheral bus address bit 24 (output).
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and Peripheral bus address bit 25 (output).
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. The value of this pin may be used as a Counter Timer Clock input.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: SDCKENP Alternate function: SDRAM clock enable output The value of this pin may be used as a Counter Timer Clock input.
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: CEN1 Alternate function: PCMCIA chip enable 1 (CE1#) (output).
GPIO[9]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: CEN2 Alternate function: PCMCIA chip enable 2 (CE2#) (output).
GPIO[10]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: REGN Alternate function: PCMCIA Attribute Memory Select (REG#) (output).
GPIO[11]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IORDN Alternate function: PCMCIA IO Read (IORD#) (output).
GPIO[12]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOWRN Alternate function: PCMCIA IO Write (IOWR#) (output).
GPIO[13]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[2] Alternate function: PCI bus request 2 (output).
GPIO[14]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[2] Alternate function: PCI bus grant 2 (output).

Table 1 Pin Description (Part 2 of 6)

Signal	Type	Name/Description
PCIREQN[1:0]	I/O	PCI Bus Request. In PCI host mode with internal arbiter: These signals are inputs whose assertion indicates to the internal RC32365 arbiter that an agent desires ownership of the PCI bus. In PCI host mode with external arbiter: PCIREQN[0]: asserted by the RC32365 to request ownership of the PCI bus. PCIREQN[1]: unused and driven high. In PCI satellite mode: PCIREQN[0]: this signal is asserted by the RC32365 to request ownership of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions.
PCIRSTN	I/O	PCI Reset. In host mode, this signal is asserted by the RC32365 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	PCI System Error. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	PCI Stop. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	PCI Target Ready. Driven by the bus target to indicate that the current data can complete.
Ethernet Interface		
MII0CL	I	Ethernet 0 MII Collision Detected. This signal is asserted by the ethernet PHY when a collision is detected.
MII0CRS	I	Ethernet 0 MII Carrier Sense. This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII0RXCLK	I	Ethernet 0 MII Receive Clock. This clock is a continuous clock that provides a timing reference for the reception of data.
MII0RXD[3:0]	I	Ethernet 0 MII Receive Data. This nibble wide data bus contains the data received by the ethernet PHY.
MII0RXDV	I	Ethernet 0 MII Receive Data Valid. The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MII0RXER	I	Ethernet 0 MII Receive Error. The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MII0TXCLK	I	Ethernet 0 MII Transmit Clock. This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MII0TXD[3:0]	O	Ethernet 0 MII Transmit Data. This nibble wide data bus contains the data to be transmitted.
MII0TXENP	O	Ethernet 0 MII Transmit Enable. The assertion of this signal indicates that data is present on the MII for transmission.
MII0TXER	O	Ethernet 0 MII Transmit Coding Error. When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MII1CL	I	Ethernet 1 MII Collision Detected. This signal is asserted by the ethernet PHY when a collision is detected.
MII1CRS	I	Ethernet 1 MII Carrier Sense. This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MII1RXCLK	I	Ethernet 1 MII Receive Clock. This clock is a continuous clock that provides a timing reference for the reception of data.

Table 1 Pin Description (Part 4 of 6)

Signal	Type	Name/Description
Miscellaneous		
CLK	I	Master Clock. This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations except those associated with SDRAMs.
COLDRSTN	I	Cold Reset. The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	Reset. The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32365 during a warm reset. It can also be asserted by an external device to force the RC32365 to take a warm reset exception.

Table 1 Pin Description (Part 6 of 6)

Pin Characteristics

Pin Name	Type	Buffer	I/O Type	Internal Resistor	External Resistor[1]
Memory and Peripheral Bus					
BDIRN	O	LVTTL	High Drive		
BOEN[1:0]	O	LVTTL	High Drive		
BWEN[3:0]	O	LVTTL	High Drive		
CSN[5:0]	O	LVTTL	High Drive		
MADDR[21:0]	O	LVTTL	High Drive		
MDATA[31:0]	I/O	LVTTL	High Drive		
OEN	O	LVTTL	High Drive		
RWN	O	LVTTL	High Drive		
WAITACKN	I	LVTTL	STI[2]	pull-up	
RASN	O	LVTTL	High Drive		
CASN	O	LVTTL	High Drive		
SDCSN[1:0]	O	LVTTL	High Drive		
SDWEN	O	LVTTL	High Drive		
SDCLKOUT	O	LVTTL	High Drive		
SDCLKINP	I	LVTTL	STI	pull-up	
General Purpose I/O					
GPIO[15:13]	I/O	PCI	PCI		
GPIO[12:0]	I/O	LVTTL	Low Drive	pull-up	
Serial Interface					
SCK	I/O	LVTTL	Low Drive	pull-up	pull-up on board
SDI	I/O	LVTTL	Low Drive	pull-up	pull-up on board
SDO	I/O	LVTTL	Low Drive	pull-up	pull-up on board
PCI Bus Interface					
PCIAD[31:0]	I/O	PCI	PCI		
PCICBEN[3:0]	I/O	PCI	PCI		
PCICLK	I	PCI	PCI		
PCIDEVSELN	I/O	PCI	PCI		pull-up on board

Table 2 Pin Characteristics (Part 1 of 2)

Pin Name	Type	Buffer	I/O Type	Internal Resistor	External Resistor[1]
PCIFRAMEN	I/O	PCI	PCI		pull-up on board
PCIGNTN[1:0]	I/O	PCI	PCI		pull-up on board
PCIIRDYN	I/O	PCI	PCI		pull-up on board
PCILOCKN	I/O	PCI	PCI		
PCIPAR	I/O	PCI	PCI		
PCIPERRN	I/O	PCI	PCI		
PCIREQN[1:0]	I/O	PCI	PCI		pull-up on board
PCIRSTN	I/O	PCI	PCI		pull-down on board
PCISERRN	I/O	PCI	Open Collector; PCI		pull-up on board
PCISTOPN	I/O	PCI	PCI		pull-up on board
PCITRDYN	I/O	PCI	PCI		pull-up on board
Ethernet Interfaces					
MII0CL	I	LVTTL	STI	pull-up	
MII0CRS	I	LVTTL	STI	pull-up	
MII0RXCLK	I	LVTTL	STI	pull-up	
MII0RXD[3:0]	I	LVTTL	STI	pull-up	
MII0RXDV	I	LVTTL	STI	pull-up	
MII0RXER	I	LVTTL	STI	pull-up	
MII0TXCLK	I	LVTTL	STI	pull-up	
MII0TXD[3:0]	O	LVTTL	Low Drive		
MII0TXENP	O	LVTTL	Low Drive		
MII0TXER	O	LVTTL	Low Drive		
MII1CL	I	LVTTL	STI	pull-up	
MII1CRS	I	LVTTL	STI	pull-up	
MII1RXCLK	I	LVTTL	STI	pull-up	
MII1RXD[3:0]	I	LVTTL	STI	pull-up	
MII1RXDV	I	LVTTL	STI	pull-up	
MII1RXER	I	LVTTL	STI	pull-up	
MII1TXCLK	I	LVTTL	STI	pull-up	
MII1TXD[3:0]	O	LVTTL	Low Drive		
MII1TXENP	O	LVTTL	Low Drive		
MII1TXER	O	LVTTL	Low Drive		
MIIMDC	O	LVTTL	Low Drive		
MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG					
JTAG_TMS	I	LVTTL	STI	pull-up	See Chapters 22 and 23 of the RC32365 User Reference Manual
EJTAG_TMS	I	LVTTL	STI	pull-up	
JTAG_TRST_N	I	LVTTL	STI	pull-up	
JTAG_TCK	I	LVTTL	STI	pull-up	
JTAG_TDO	O	LVTTL	Low Drive		
JTAG_TDI	I	LVTTL	STI	pull-up	
Miscellaneous					
CLK	I	LVTTL	STI		
COLDRSTN	I	LVTTL	STI		
RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Schmidt Trigger Input (STI).

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

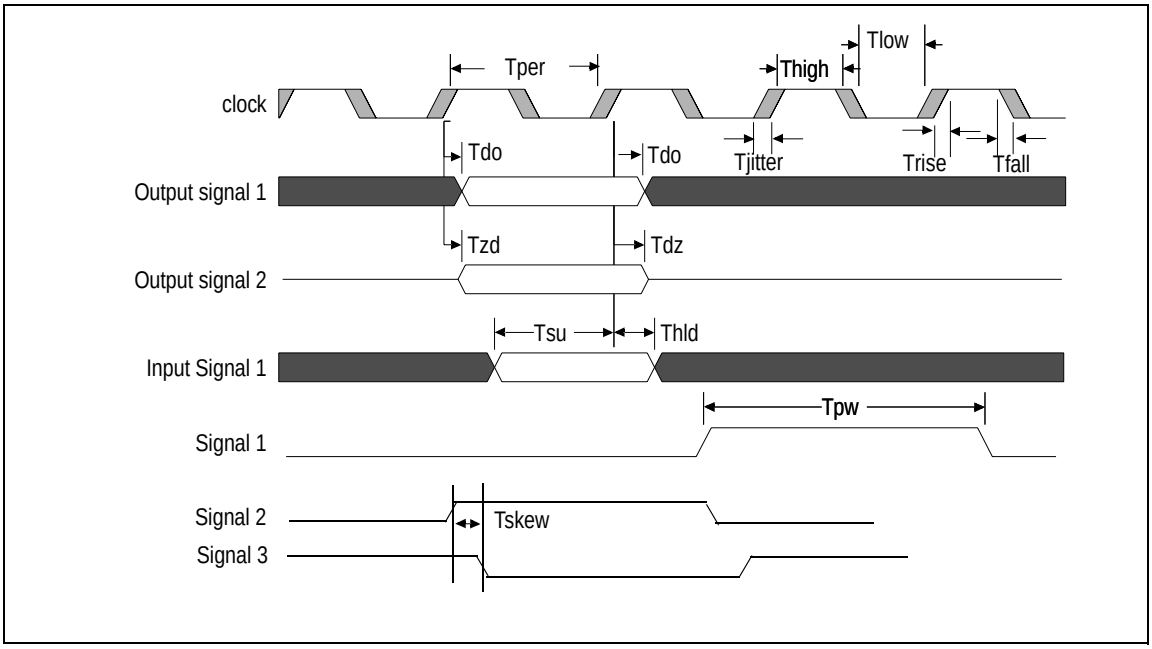


Figure 2 AC Timing Definitions Waveform

Symbol	Definition
Tper	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active for asynchronous signals.
Tslew	Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high.
X(clock)	Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200.
Tskew	Skew. The amount of time two signal edges deviate from one another.

Table 4 AC Timing Definitions

AC Timing Characteristics

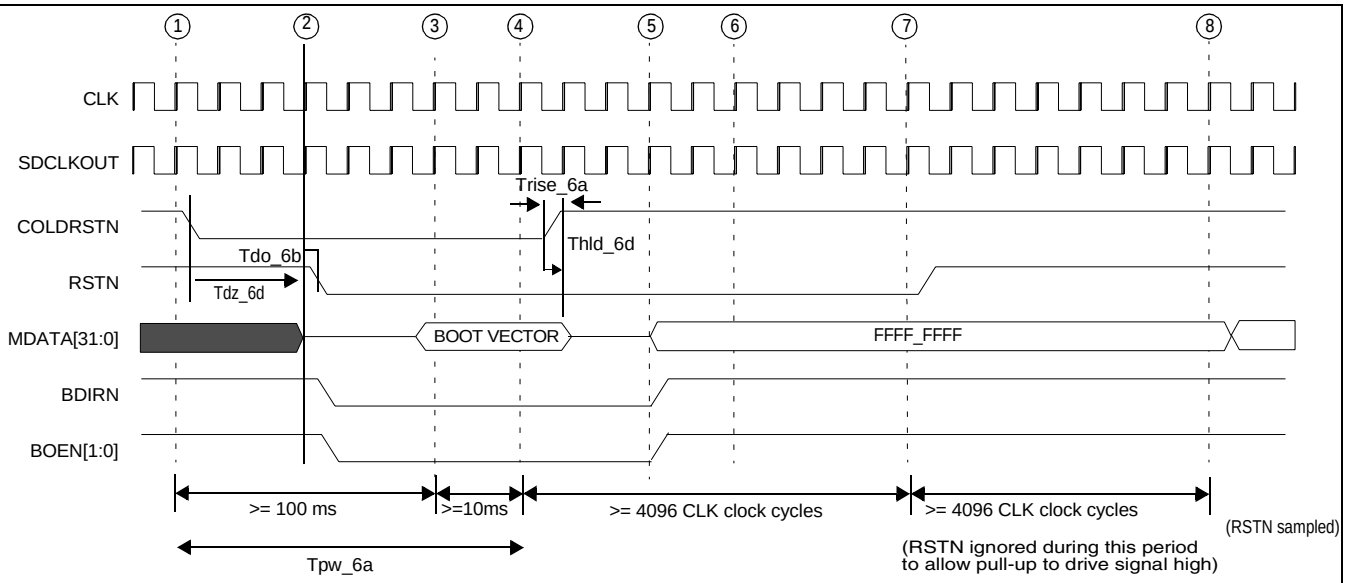
The values given below are based on systems running at recommended operating supply voltages and temperatures as shown in Tables 14 and 15.

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
Reset and System							
COLDRSTN	Tpw_6a[1]	none	110	—	ms	Cold reset	See Figures 4 and 5
	Trise_6a		—	5.0	ns	Cold reset	
RSTN[2] (output)	Tdo_6b	CLK rising	2.0	9.0	ns	Cold reset	
RSTN[2] (input)	Tpw_6c[1]	none	2(CLK)	—	ns	Cold reset	
MDATA[15:0] Boot Configuration Vector	Thld_6d	COLDRSTN rising	3.0	—	ns	Cold reset	
	Tdz_6d[1]	COLDRSTN falling	—	2(CLK)	ns	Cold reset	
	Tdz_6d[1]	RSTN falling	—	2(CLK)	ns	Warm reset	
	Tzd_6d[1]	RSTN rising	3.0	—	ns	Warm reset	

Table 6 Reset and System AC Timing Characteristics

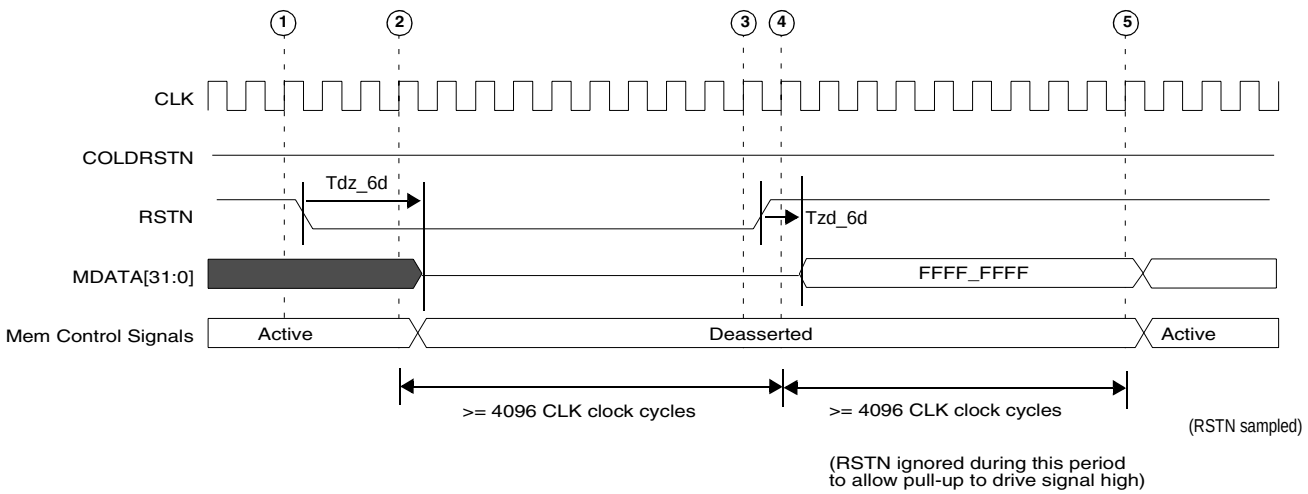
1. The values for this symbol were determined by calculation, not by testing.

2. RSTN is a bidirectional signal. It is treated as an asynchronous input.



1. COLDRSTN asserted by external logic.
2. RC32365 asserts RSTN, asserts BOEN[0] low, drives BDIRN low, and tri-states the data bus in response.
3. External logic begins driving valid boot configuration vector on the data bus, and the RC32365 starts sampling it.
4. External logic negates COLDRSTN and tri-states the boot configuration vector on MDATA[15:0]. The boot configuration vector must not be tri-stated before COLDRSTN is deasserted. The RC32365 stops sampling the boot configuration vector.
5. The RC32365 starts driving the data bus, MDATA[31:0], deasserts BOEN[0] high, and drives BDIRN high.
6. SYSCLK may be held constant after this point if Hold SYSCLK Constant is selected in the boot configuration vector.
7. RSTN negated by the RC32365.
8. CPU begins executing by taking MIPS reset exception, and the RC32365 starts sampling RSTN as a warm reset input.

Figure 4 Cold Reset AC Timing Waveform



1. Warm reset condition caused by either RSTN asserted, write to reset register, or bus transaction timer time-out. The RC32365 asserts RSTN output low in response.
2. The RC32365 tri-states the data bus, MDATA[31:0], and deasserts all memory control signals, such as RASN, CASN, RWN, OEN, etc.
3. The RC32365 deasserts RSTN.
4. The RC32365 starts driving the data bus, MDATA[31:0], again, but does not sample the RSTN input.
5. CPU begins executing by taking a MIPS soft reset exception and also starts sampling the RSTN input again.

Figure 5 Warm Reset AC Timing Waveform

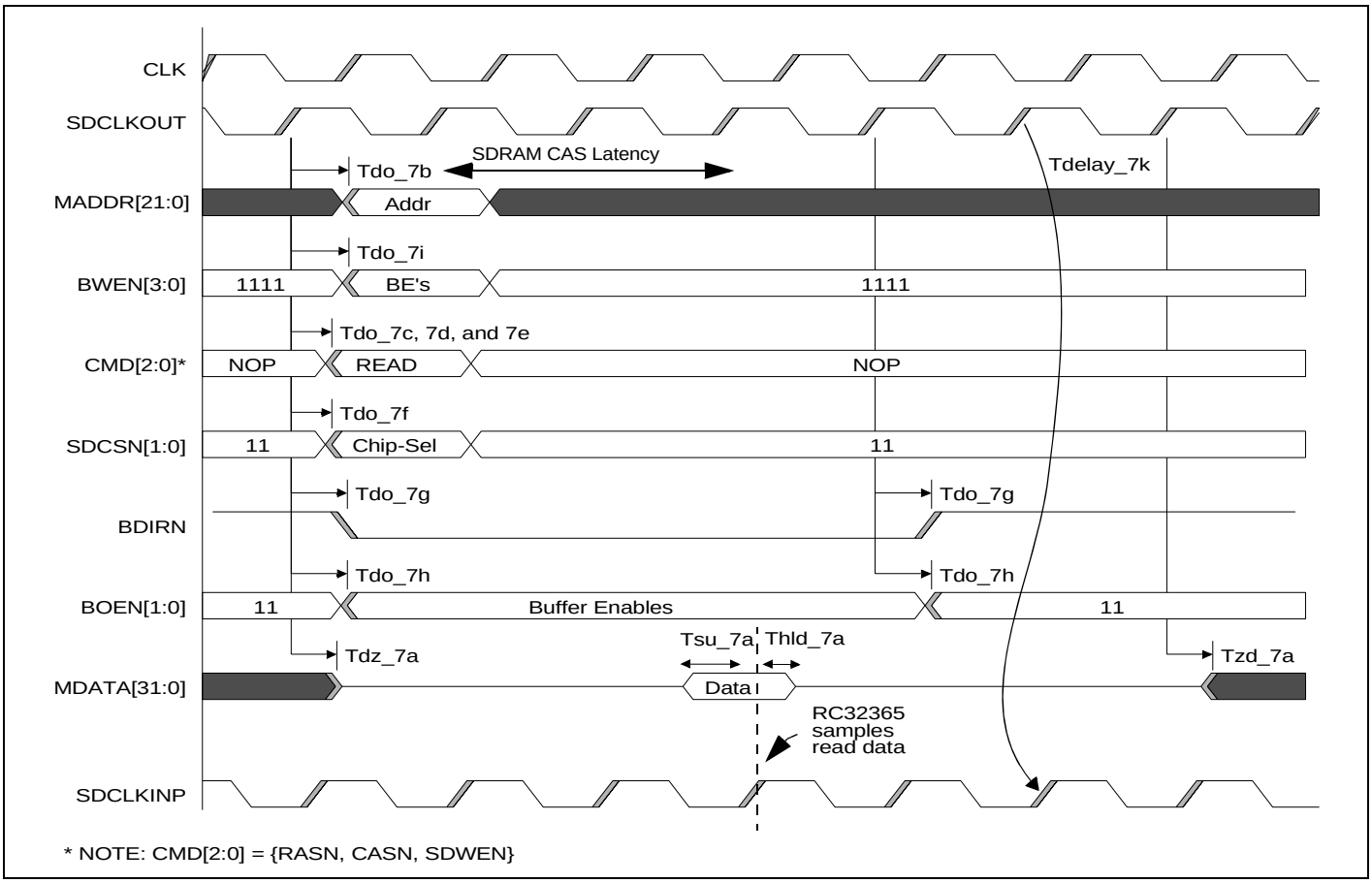


Figure 6 Memory and Peripheral Bus AC Timing Waveform - SDRAM Read Access

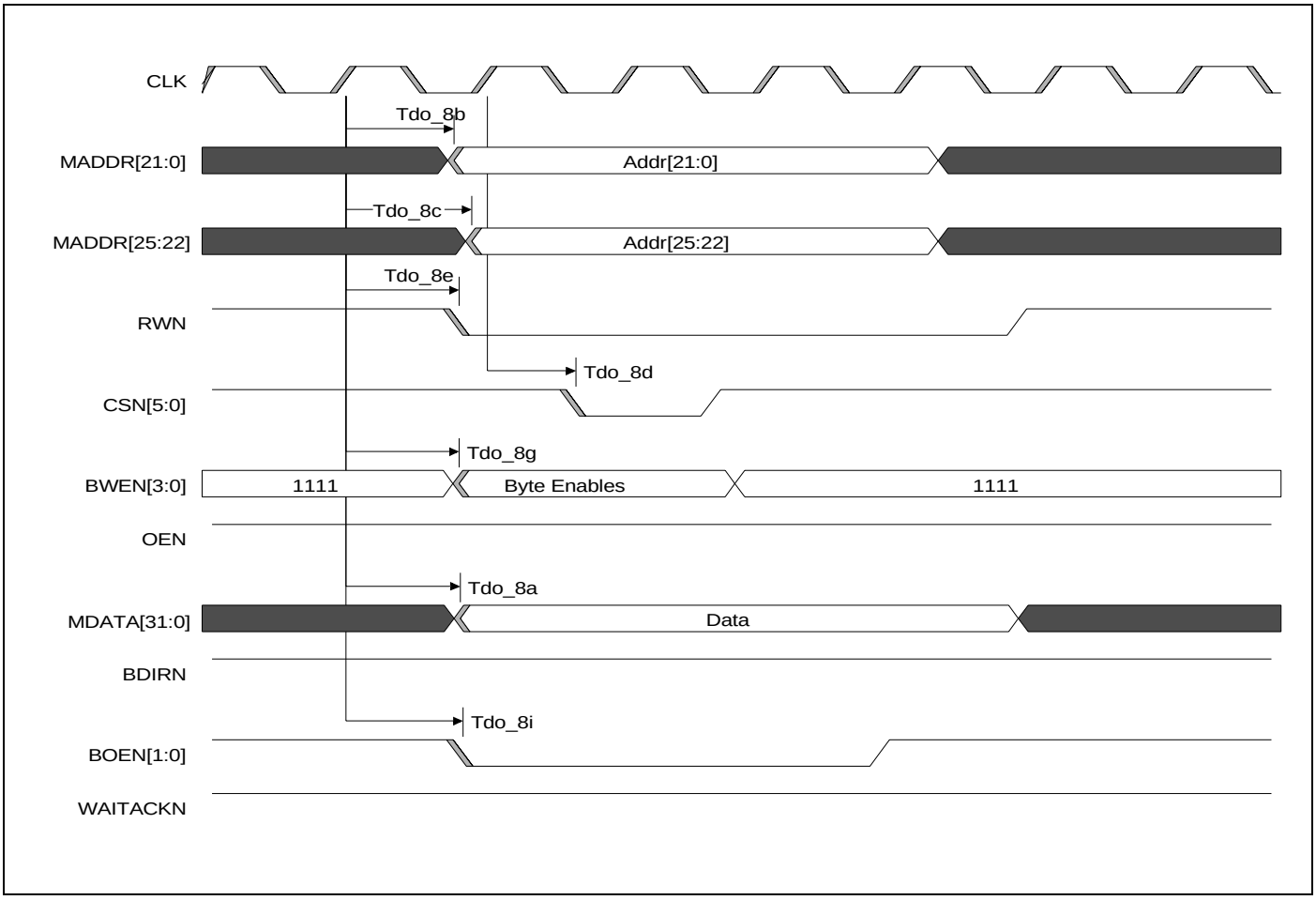


Figure 10 Memory AC and Peripheral Bus Timing Waveform - Device Write Access

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
Ethernet[1]							
MIIMDC	Tper_9a	None	53.3	—	ns		See Figure 11
	Thigh_9a, Tlow_9a		23.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	ns		
	Thld_9b		1.0	—	ns		
	Tdo_9b		1(ICLK)	3(ICLK)	ns		
MIIxRXCLK, MIIxTX-CLK[2]	Tper_9c	None	399.96	400.4	ns	10 Mbps	
	Thigh_9c, Tlow_9c		140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	ns		
MIIxRXCLK, MIIxTXCLK[2]	Tper_9d	None	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	ns		
MIIxRXD[3:0], MIIxRXDV, MIIxRXER	Tsu_9e	MIIxRXCLK rising	3.0	—	ns		
	Thld_9e		2.0	—	ns		
MIIxTXD[3:0], MIIxTXENP, MIIxTXER	Tdo_9f	MIIxTXCLK rising	5.0	13	ns		

Table 9 Ethernet AC Timing Characteristics

1. There are two MII interfaces and the timing is the same for each. “x” represents interface 0 or 1 (For example, MIIxRXCLK can be either MII0RXCLK or MII1RXCLK).

2. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 CLK (MIIxRXCLK and MIIxTXCLK <= 1/2(CLK)).

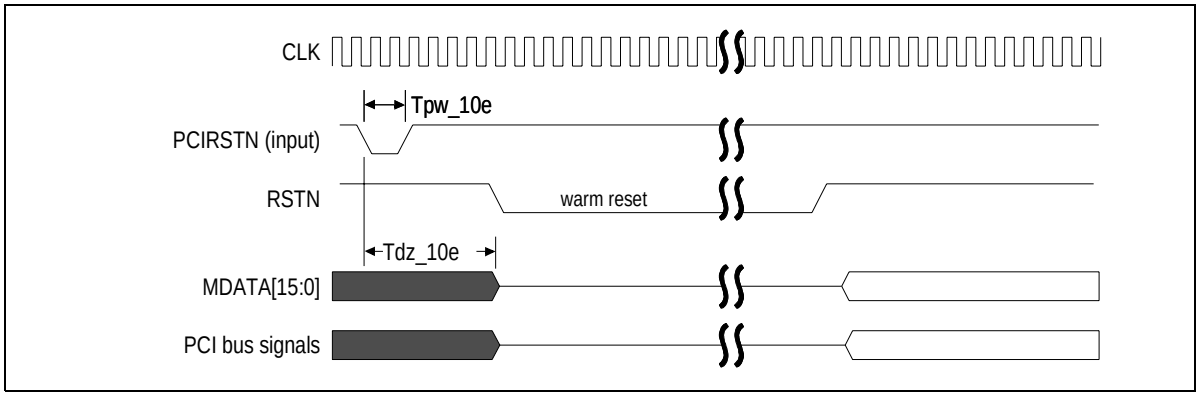


Figure 14 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	150MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max			
SPI[1]							
SCK	Tper_12a	None	—	1920	ns	33 MHz PCI	See Figures 15 through 18
	Tper_12a		—	960	ns	66 MHz PCI	
	Tper_12a		100	166667	ns	SPI	
	Thigh_12a, Tlow_12a		930	990	ns	33 MHz PCI	
	Thigh_12a, Tlow_12a		465	495	ns	66 MHz PCI	
	Thigh_12a, Tlow_12a		40	83353	ns	SPI	
SDI	Tsu_12b	SCK rising or falling	60	—	ns	SPI or PCI	
	Thld_12b		60	—	ns		
SDO	Tdo_12c	SCK rising or falling	0	60	ns	SPI or PCI	
PCIEECS[2]	Tdo_12d	SCK rising or falling	0	60	ns	PCI	
SCK, SDI, SDO[3]	Tpw_12e	None	2(CLK)	—	ns		

Table 11 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

2. PCIEECS is the PCI serial EEPROM chip select. It is an alternate function of PCIGNTN[1].

3. In Bit I/O mode, SCK, SDI, and SDO must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32365 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 21 shows the electrical connection of the EJTAG probe target system connector.

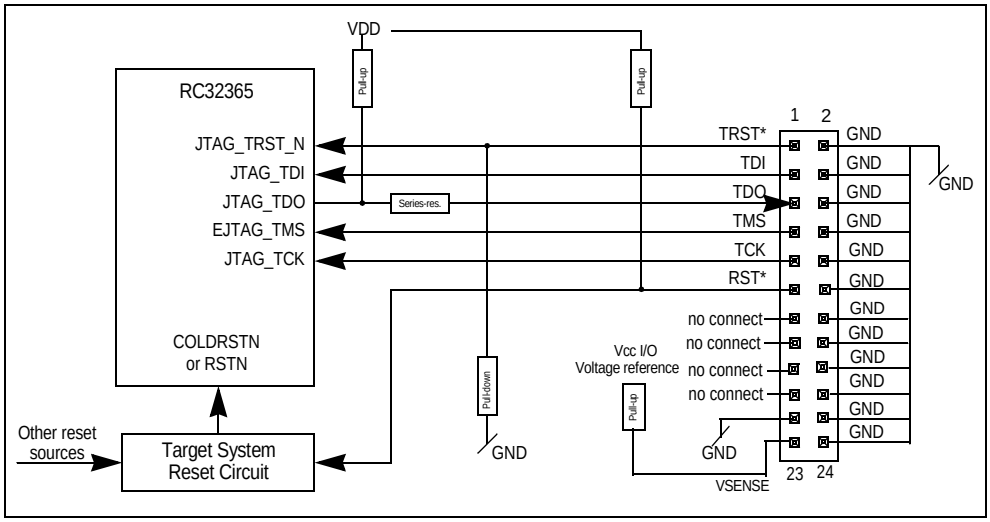


Figure 21 Target System Electrical EJTAG Connection

Using the EJTAG Probe

In Figure 21, the pull-up resistors for JTAG_TDO and RST*, the pull-down resistor for JTAG_TRST_N, and the series resistor for JTAG_TDO must be adjusted to the specific design. However, the recommended pull-up/down resistor is 1.0 kΩ because a low value reduces crosstalk on the cable to the connector, allowing higher JTAG_TCK frequencies. A typical value for the series resistor is 33 Ω. Recommended resistor values have ± 5% tolerance.

If a probe is used, the pull-up resistor on JTAG_TDO must ensure that the JTAG_TDO level is high when no probe is connected and the JTAG_TDO output is tri-stated. This requirement allows reliable connection of the probe if it is hooked-up when the power is already on (hot plug). The pull-up resistor value of around 47 kΩ should be sufficient. Optional diodes to protect against overshoot and undershoot voltage can be added on the signals of the chip with EJTAG.

If a probe is used, the RST* signal must have a pull-up resistor because it is controlled by an open-collector (OC) driver in the probe, and thus is actively pulled low only. The pull-up resistor is responsible for the high value when not driven by the probe of 25pF. The input on the target system reset circuit must be able to accept the rise time when the pull-up resistor charges the capacitance to a high logical level. Vcc I/O must connect to a voltage reference that drops rapidly to below 0.5V when the target system loses power, even with a capacitive load of 25pF. The probe can thus detect the lost power condition.

For additional information on EJTAG, refer to Chapter 23 of the RC32365 User Reference Manual.

Voltage Sense Signal Timing

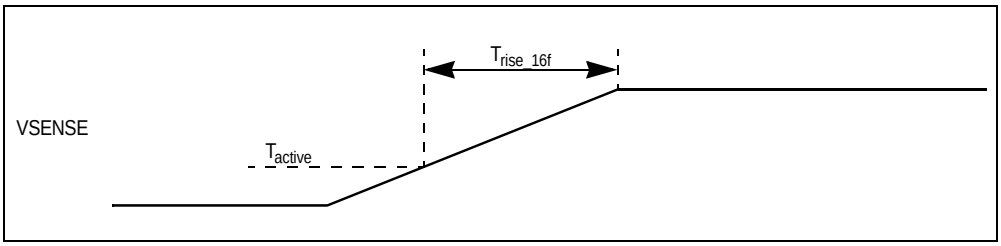
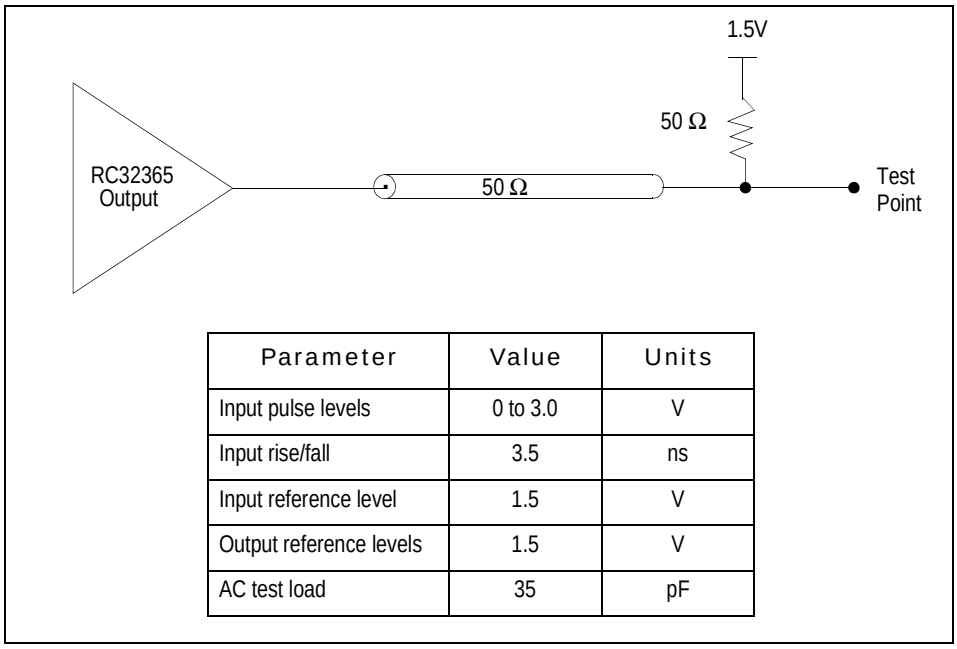


Figure 22 Voltage Sense Signal Timing

The target system must ensure that T_{rise} is obeyed after the system reaches 0.5V (T_{active}), so the probe can use this value to determine when the target has powered-up. The probe is allowed to measure the T_{rise} time from a higher value than T_{active} (but lower than Vcc I/O minimum) because the stable indication in this case comes later than the time when target power is guaranteed to be stable. If JTAG_TRST_N is asserted by a pulse at power-up, this reset must be completed after T_{rise}. If JTAG_TRST_N is asserted by a pull-down resistor, the probe will control JTAG_TRST_N. At power-down, no power is indicated to the probe when Vcc I/O drops under the T_{active} value, which the probe uses to stop driving the input signals, except for the probe RST*.

AC Test Conditions



Parameter	Value	Units
Input pulse levels	0 to 3.0	V
Input rise/fall	3.5	ns
Input reference level	1.5	V
Output reference levels	1.5	V
AC test load	35	pF

Figure 23 Output Loading for AC Timing

Phase-Locked Loop (PLL)

The processor aligns the pipeline clock, PClock, to the master input clock (CLK) by using an internal phase-locked loop (PLL) circuit that generates aligned clocks. Inherently, PLL circuits are only capable of generating aligned clocks for master input clock (CLK) frequencies within a limited range.

PLL Analog Filter

The storage capacitor required for the Phase-Locked Loop circuit is contained in the RC32365. However, it is recommended that the system designer provide a filter network of passive components for the PLL power supply.

V_{CC}PLL (circuit power) and V_{SS}PLL (circuit ground) should be isolated from V_{CC} Core (core power) and V_{SS} (common ground) with a filter circuit such as the one shown in Figure 24.

DC Electrical Characteristics

The values given below are based on systems running at recommended supply voltages, as shown in Table 14.

Note: For a complete list of I/O types, see Table 2.

	Parameter	Min	Max	Unit	Conditions
LOW Drive Output with Schmitt Trigger Input (STI)	I_{OL}	—	7.3	mA	V_{OL} = 0.4V
	I_{OH}	—	-8.0	mA	$V_{OH} = (V_{CC}I/O - 0.4)$
	V_{IL}	—	0.8	V	—
	V_{IH}	2.0	$(V_{CC}I/O + 0.5)$	V	—
HIGH Drive Output with Standard Input	I_{OL}	—	9.4	mA	V_{OL} = 0.4V
	I_{OH}	—	-15	mA	$V_{OH} = (V_{CC}I/O - 0.4)$
	V_{IL}	—	0.8	V	—
	V_{IH}	2.0	$(V_{CC}I/O + 0.5)$	V	—
Clock Drive Output	I_{OL}	39	—	mA	V_{OL} = 0.4V
	I_{OH}	-24	—	mA	$V_{OH} = (V_{CC}I/O - 0.4)$
PCI	I_{OH}(AC) Switching	$-12(V_{CC}I/O)$	—	mA	$0 < V_{OUT} < 0.3(V_{CC}I/O)$
		$-17.1(V_{CC}I/O - V_{OUT})$	—	mA	$0.3(V_{CC}I/O) < V_{OUT} < 0.9(V_{CC}I/O)$
		—	$-32(V_{CC}I/O)$	mA	$0.7(V_{CC}I/O)$
	I_{OL}(AC) Switching	$+16(V_{CC}I/O)$		mA	$V_{CC}I/O > V_{OUT} > 0.6(V_{CC}I/O)$
		$+26.7(V_{OUT})$		mA	$0.6(V_{CC}I/O) > V_{OUT} > 0.1(V_{CC}I/O)$
		—	$+38(V_{CC}I/O)$	mA	$V_{OUT} = 0.18(V_{CC}I/O)$
	V_{IL}	-0.3	$0.3(V_{CC}I/O)$	V	—
	V_{IH}	$0.5(V_{CC}I/O)$	5.5	V	—
Capacitance	C_{IN}	—	10	pF	—
Leakage	I/O_{LEAK}	—	20	µA	—

Table 16 DC Electrical Characteristics

Power Consumption

Parameter		150MHz		Unit	Conditions
		Typical	Max.		
IccI/O		60	80	mA	C_L = 25pF (affects I/O) $T_a = 25^oC$ Maximum values use the maximum voltages listed in Table 14. Typical values use the typical voltages listed in Table 14.
I_{cc}Core	Normal mode	710	750	mA	
	Standby mode[1]	620	660	mA	
Power Dissipation	Normal mode	2.07	2.2	W	
	Standby mode[1]	1.8	2.0	W	

Table 17 RC32365 Power Consumption

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions; however, other logic continues to function. Standby mode reduces power consumption by 0.6 mA per MHz of the CPU pipeline clock, PCLK.

Package Pin-out — 256-Pin CABGA

The following table lists the pin numbers and signal names for the RC32365.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	MII0RXD[0]		E1	GPIO[15]	1	J1	PCIGNTN[1]		N1	PCIAD[4]	
A2	MII0RXDV		E2	JTAG_TRST_N		J2	PCIDEVSELN		N2	PCIAD[20]	
A3	MII0RXER		E3	JTAG_TDO		J3	PCIGNTN[0]		N3	PCIAD[19]	
A4	MII0TXCLK		E4	JTAG_TDI		J4	PCIFRAMEN		N4	PCIAD[11]	
A5	MII0TXD[2]		E5	V_{cc}CORE		J5	V_{cc}I/O		N5	PCIAD[13]	
A6	MII0CRS		E6	V_{cc}I/O		J6	V_{ss}		N6	PCIAD[15]	
A7	VssPLL		E7	V_{cc}I/O		J7	V_{ss}		N7	BOEN[0]	
A8	MII1RXCLK		E8	V_{cc}I/O		J8	V_{ss}		N8	CSN[2]	
A9	MII1TXD[2]		E9	V_{cc}I/O		J9	V_{ss}		N9	CSN[3]	
A10	MII1CL		E10	V_{cc}I/O		J10	V_{ss}		N10	RWN	
A11	JTAG_TCK		E11	V_{cc}I/O		J11	V_{ss}		N11	MDATA[1]	
A12	GPIO[9]	1	E12	V_{cc}CORE		J12	V_{cc}I/O		N12	MDATA[3]	
A13	GPIO[5]	1	E13	MADDR[5]		J13	SDWEN		N13	MDATA[12]	
A14	GPIO[3]	1	E14	MADDR[16]		J14	SDCLKINP		N14	MDATA[30]	
A15	GPIO[1]	1	E15	MADDR[17]		J15	BWEN[2]		N15	MDATA[11]	
A16	MADDR[10]		E16	MADDR[6]		J16	BWEN[3]		N16	MDATA[27]	
B1	MII0RXD[3]		F1	GPIO[14]	1	K1	PCICBEN[1]		P1	PCIAD[5]	
B2	MII0RXD[1]		F2	GPIO[13]	1	K2	PCICBEN[2]		P2	PCIAD[21]	
B3	MII0RXCLK		F3	PCITRDYN		K3	PCICBEN[0]		P3	PCIAD[23]	
B4	MII0TXER		F4	PCISTOPN		K4	PCICLK		P4	PCIAD[10]	
B5	MII0TXD[3]		F5	V_{cc}CORE		K5	V_{cc}I/O		P5	PCIAD[28]	
B6	MII0CL		F6	V_{cc}I/O		K6	V_{ss}		P6	PCIAD[30]	
B7	VccPLL		F7	V_{ss}		K7	V_{ss}		P7	BDIRN	
B8	MII1RXDV		F8	V_{ss}		K8	V_{ss}		P8	CSN[1]	
B9	MII1TXD[3]		F9	V_{ss}		K9	V_{ss}		P9	CSN[4]	
B10	MII1CRS		F10	V_{ss}		K10	V_{ss}		P10	WAITACKN	
B11	GPIO[12]	1	F11	V_{cc}I/O		K11	V_{ss}		P11	MDATA[17]	
B12	GPIO[8]	1	F12	V_{cc}CORE		K12	V_{cc}CORE		P12	MDATA[19]	
B13	GPIO[4]	1	F13	MADDR[3]		K13	BWEN[1]		P13	MDATA[5]	
B14	GPIO[2]	1	F14	MADDR[14]		K14	RASN		P14	MDATA[9]	
B15	MADDR[21]		F15	MADDR[15]		K15	CASN		P15	MDATA[10]	
B16	MADDR[20]		F16	MADDR[4]		K16	BWEN[0]		P16	MDATA[26]	
C1	MIIMDC		G1	PCIRSTN		L1	PCIAD[16]		R1	PCIAD[6]	
C2	MIIMDIO		G2	PCISERRN		L2	PCIAD[1]		R2	PCIAD[7]	

Table 19: 256-pin CABGA Package Pin-Out (Part 1 of 2)

RC32365 Power Pins

V_{cc}I/O	V_{cc}I/O	V_{cc}Core	V_{cc}PLL
E6	J5	E5	B7
E7	J12	E12	
E8	K5	F5	
E9	L6	F12	
E10	L11	G5	
E11	M6	K12	
F6	M7	L5	
F11	M8	L12	
G12	M9	M5	
H5	M10	M12	
H12	M11		

Table 20 RC32365 Power Pins

RC32365 Ground Pins

V_{ss}	V_{ss}	V_{ss}	V_{ss}PLL
F7	H7	K6	A7
F8	H8	K7	
F9	H9	K8	
F10	H10	K9	
G6	H11	K10	
G7	J6	K11	
G8	J7	L7	
G9	J8	L8	
G10	J9	L9	
G11	J10	L10	
H6	J11		

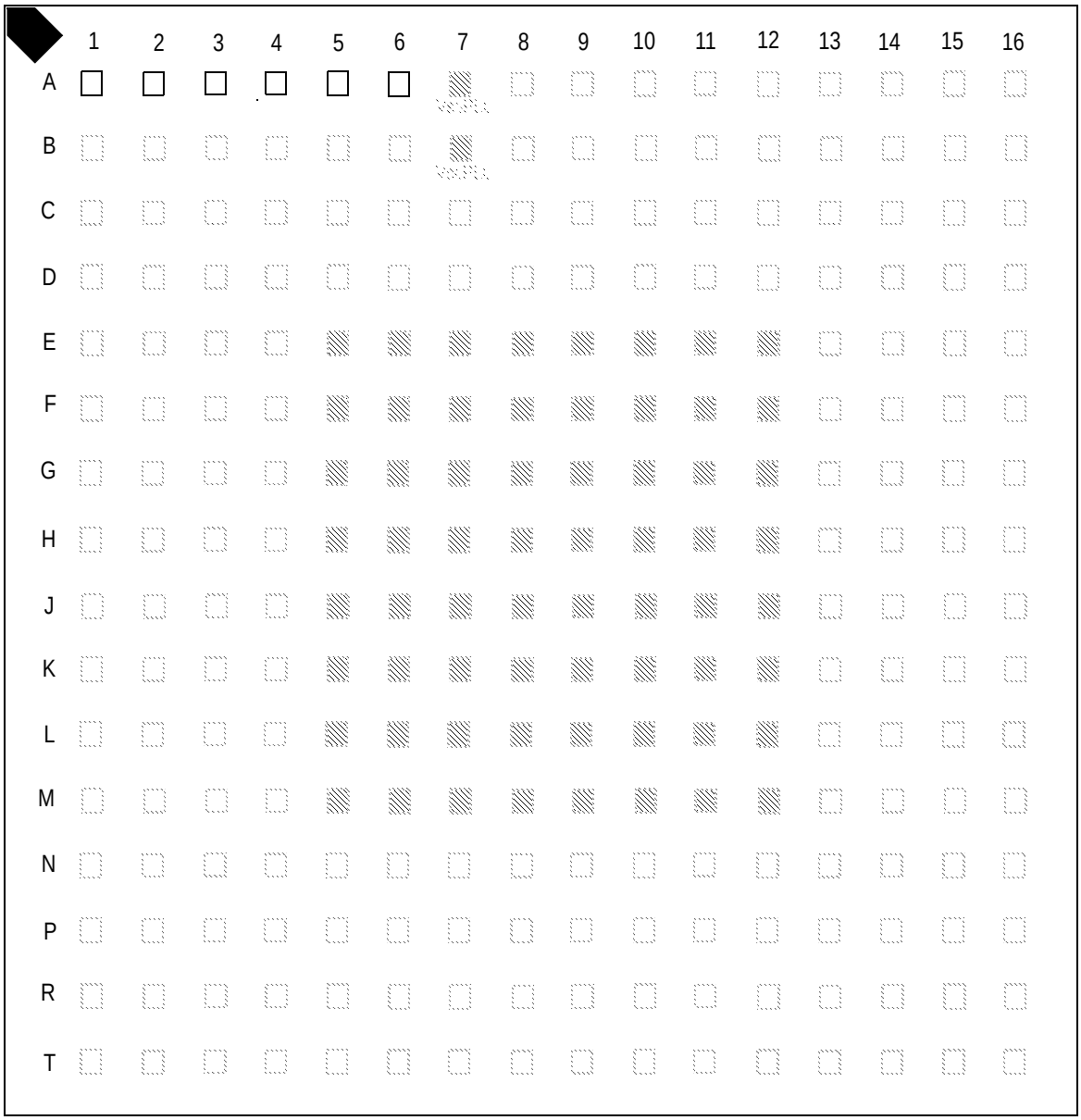
Table 21 RC32365 Ground Pins

Alternate Pin Functions

Pin	Primary	Alt #1
C14	GPIO[0]	U0SOUT
A15	GPIO[1]	U0SINP
B14	GPIO[2]	MADDR[22]
A14	GPIO[3]	MADDR[23]
B13	GPIO[4]	MADDR[24]
A13	GPIO[5]	MADDR[25]
C13	GPIO[6]	N/A
D13	GPIO[7]	SDCKENP
B12	GPIO[8]	CEN1
A12	GPIO[9]	CEN2
C12	GPIO[10]	REGN
D12	GPIO[11]	IORDN
B11	GPIO[12]	IOWRN
F2	GPIO[13]	PCIREQN[2]
F1	GPIO[14]	PCIGNTN[2]
E1	GPIO[15]	PCIMUNITN

Table 22 Alternate Pin Functions

RC32365 Pinout — Top View



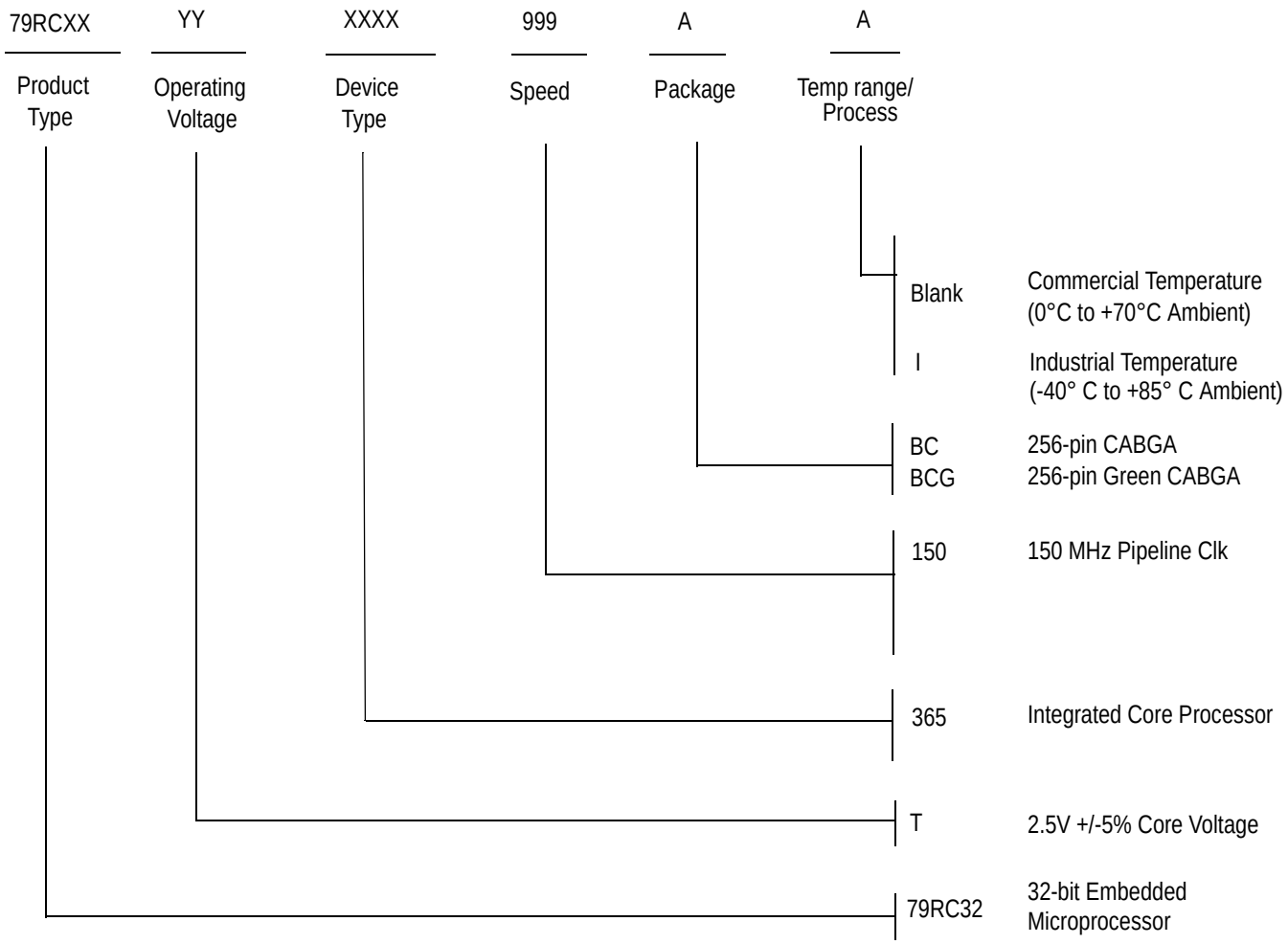
V_{SS} (Ground)

V_{CC}I/O (Power)

V_{CC}Core (Power)

Package Drawing - page two

Ordering Information



Valid Combinations

79RC32T365 - 150BC	256-pin CABGA package, Commercial Temperature
79RC32T365 - 150BCG	256-pin CABGA package, Commercial Temperature (Green)
79RC32T365 - 150BCI	256-pin CABGA package, Industrial Temperature
79RC32T365 - 150BCGI	256-pin CABGA package, Industrial Temperature (Green)

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