Intel - EPF81188AQC208-2 Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	126
Number of Logic Elements/Cells	1008
Total RAM Bits	-
Number of I/O	148
Number of Gates	12000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf81188aqc208-2

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block

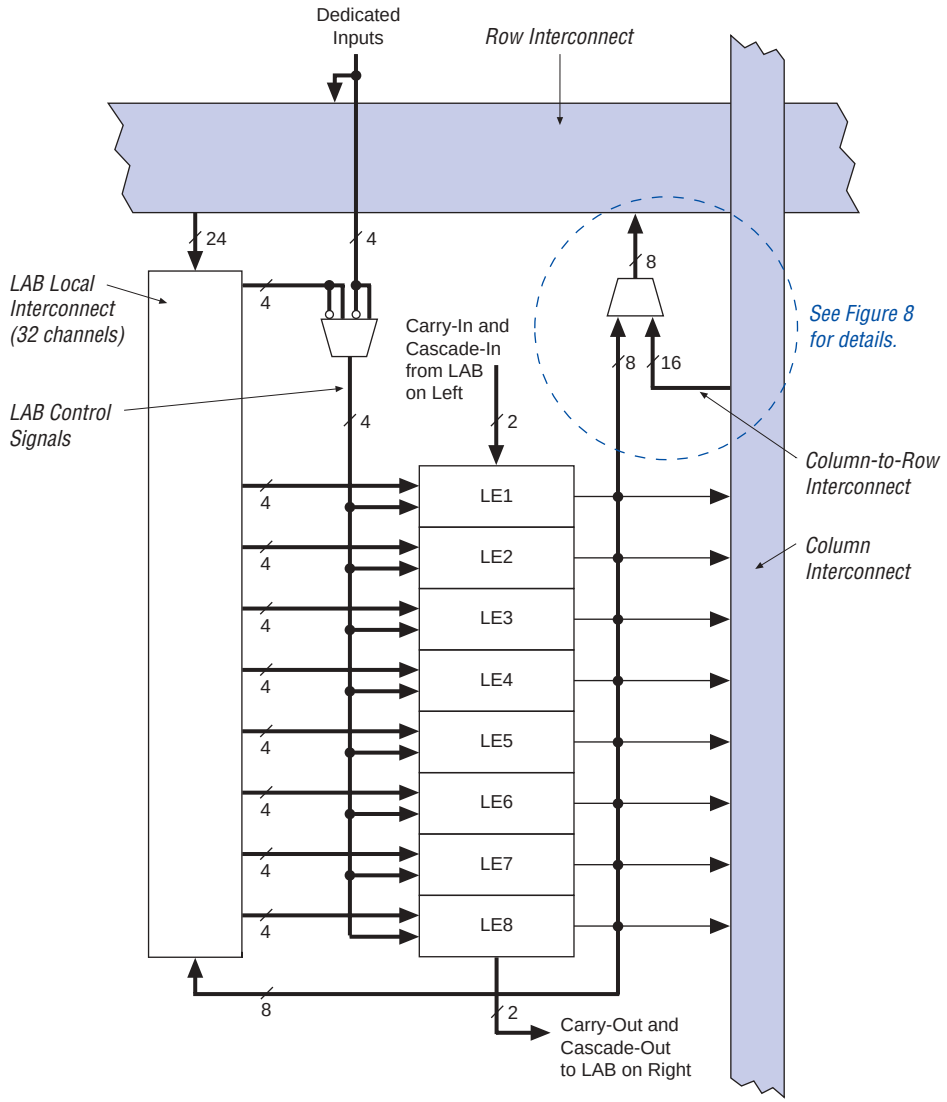
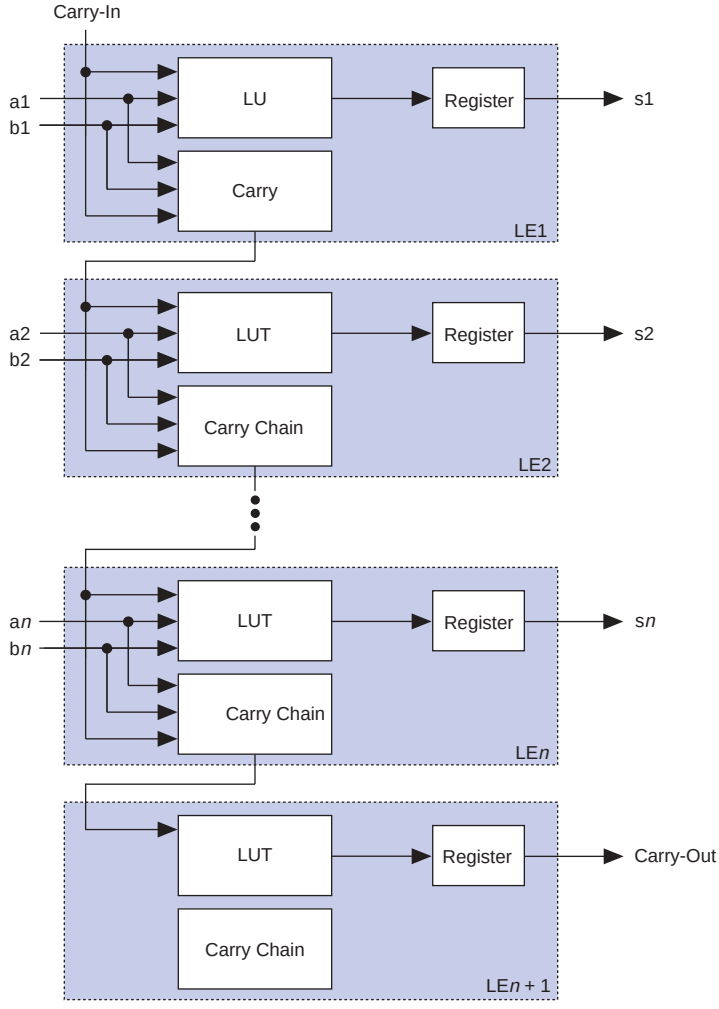


Figure 4. FLEX 8000 Carry Chain Operation



Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.6 ns per LE.

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

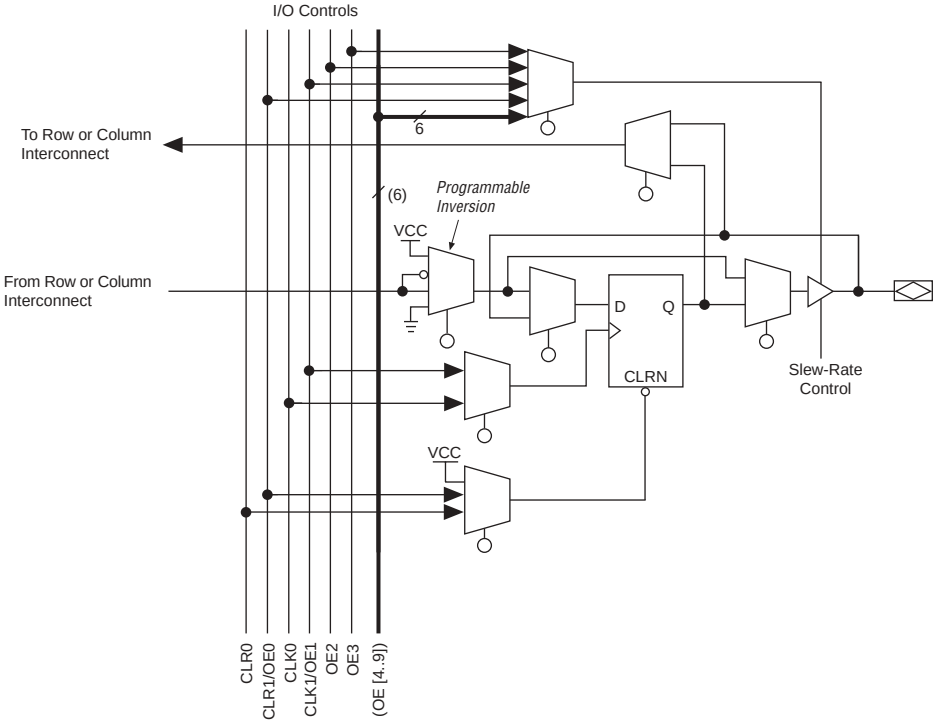
Table 4. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282A EPF8282AV	2	168	13	16
EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820A	4	168	21	16
EPF81188A	6	168	21	16
EPF81500A	6	216	27	16

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 10. FLEX 8000 IOE

Numbers in parentheses are for EPF81500A devices only.



Row-to-IOE Connections

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 5. Row Sources of FLEX 8000 Peripheral Control Signals

Peripheral Control Signal	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	–	–	–	–	–	Row B
OE5	–	–	–	–	–	Row C
OE6	–	–	–	–	–	Row D
OE7	–	–	–	–	–	Row D
OE8	–	–	–	–	–	Row E
OE9	–	–	–	–	–	Row F

Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

For more information on high-speed system design, go to *Application Note 75 (High-Speed Board Designs)*.

Table 10. FLEX 8000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	*(3)*, *(4)*	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		–0.5	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 11. FLEX 8000 5.0-V Device DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC *(7)* V_{CCIO} = 4.75 V	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC *(7)* V_{CCIO} = 3.00 V	2.4			V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC *(7)* V_{CCIO} = 3.00 V	V_{CCIO} – 0.2			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC *(7)* V_{CCIO} = 4.75 V			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC *(7)* V_{CCIO} = 3.00 V			0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC *(7)* V_{CCIO} = 3.00 V			0.2	V
I_I	Input leakage current	V_I = V_{CC} or ground	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or ground	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load		0.5	10	mA

Table 19. FLEX 8000 Interconnect Timing Parameters Note (1)	
Symbol	**Parameter**
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay *(4)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay *(4)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 20. FLEX 8000 External Reference Timing Characteristics Note (5)	
Symbol	**Parameter**
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)*
t_{ODH}	Output data hold time after clock *(7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.
(4) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

Figure 19. FLEX 8000 Timing Model

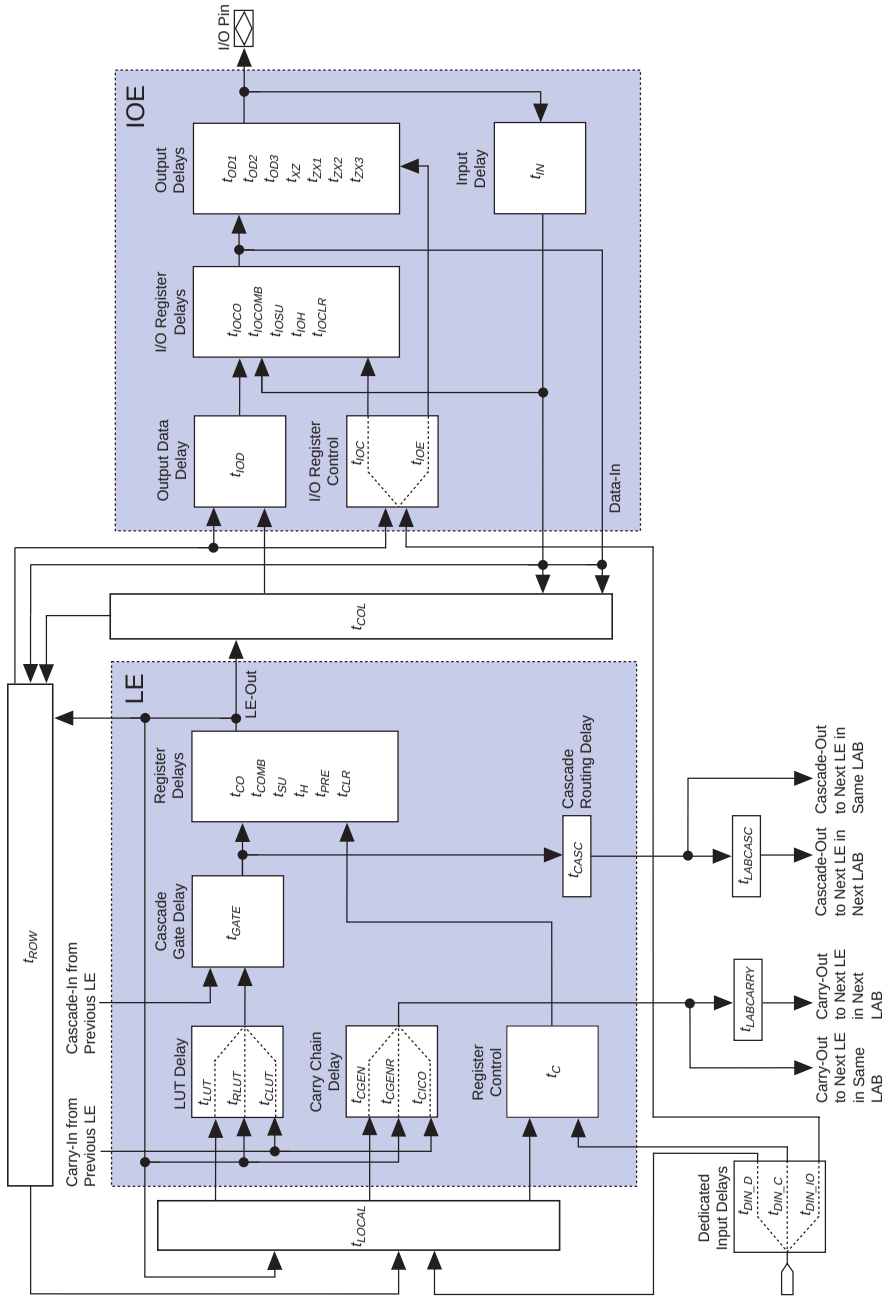


Table 23. EPF8282A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.2		7.2		7.2	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 28. EPF8282AV Logic Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{LUT}		3.2		7.3	ns
t_{CLUT}		0.0		1.4	ns
t_{RLUT}		1.5		5.1	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		0.9		2.8	ns
t_{CICO}		0.6		1.5	ns
t_{CGEN}		0.7		2.2	ns
t_{CGENR}		1.5		3.7	ns
t_{C}		2.5		4.7	ns
t_{CH}	4.0		6.0		ns
t_{CL}	4.0		6.0		ns
t_{CO}		0.6		0.9	ns
t_{COMB}		0.6		0.9	ns
t_{SU}	1.2		2.4		ns
t_{H}	1.5		4.6		ns
t_{PRE}		0.8		1.3	ns
t_{CLR}		0.8		1.3	ns

Table 29. EPF8282AV External Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{DRR}		24.8		50.1	ns
t_{ODH}	1.0		1.0		ns

Table 32. EPF8452A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_{C}		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_{H}	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 33. EPF8452A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 34. EPF8636A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 35. EPF8636A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 38. EPF8820A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 39. EPF8820A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 44. EPF81188A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 45. EPF81188A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 46. EPF81500A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 47. EPF81500A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 48. EPF81500A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 49. EPF81500A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.1		20.1		25.1	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
nSP *(2)*	120	1	R15	207	207	5
MSEL0 *(2)*	117	3	T15	4	4	21
MSEL1 *(2)*	84	38	T3	49	49	33
nSTATUS *(2)*	37	83	B3	108	108	124
nCONFIG *(2)*	40	81	C3	103	103	107
DCLK *(2)*	1	120	C15	158	158	154
CONF_DONE *(2)*	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
DATA4	154	127	E17	165	172	170
DATA3	157	124	G15	162	171	168
DATA2	159	122	F15	160	167	166
DATA1	11	115	E16	149	165	163
DATA0	12	113	C16	147	162	161
SDOUT *(3)*	128	152	C7 *(11)*	198	124	119
TDI *(4)*	–	55	R11	72	20	–
TDO *(4)*	–	95	B9	120	129	–
TCK *(4)*, *(6)*	–	57	U8	74	30	–
TMS *(4)*	–	59	U7	76	32	–
TRST *(7)*	–	40	R3	54	54	–
Dedicated Inputs *(10)*	5, 36, 85, 116	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146
VCCINT (5.0 V)	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147
VCCIO (5.0 V or 3.3 V)	–	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192
GND	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201
No Connect (N.C.)	2, 3, 38, 39, 70, 82, 83, 118, 119, 148	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4 *(12)*	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208
Total User I/O Pins *(9)*	116	114	132, 148 *(13)*	132	148	144

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP *(2)*	A15	C14	237	237	W1	304
MSEL0 *(2)*	B14	G15	21	19	N1	26
MSEL1 *(2)*	R15	L15	40	38	H3	51
nSTATUS *(2)*	P2	L3	141	142	G19	178
nCONFIG *(2)*	R1	R4	117	120	B18	152
DCLK *(2)*	B2	C4	184	183	U18	230
CONF_DONE *(2)*	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDYnBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

Notes to tables:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a V_{CC} pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) SDOUT does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.