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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 126 |
| Number of Logic Elements/Cells | 1008 |
| Total RAM Bits | - |
| Number of I/O | 148 |
| Number of Gates | 12000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf81188aqc208-4 |

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 8000 architecture.

For more information on the MAX+PLUS II software, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

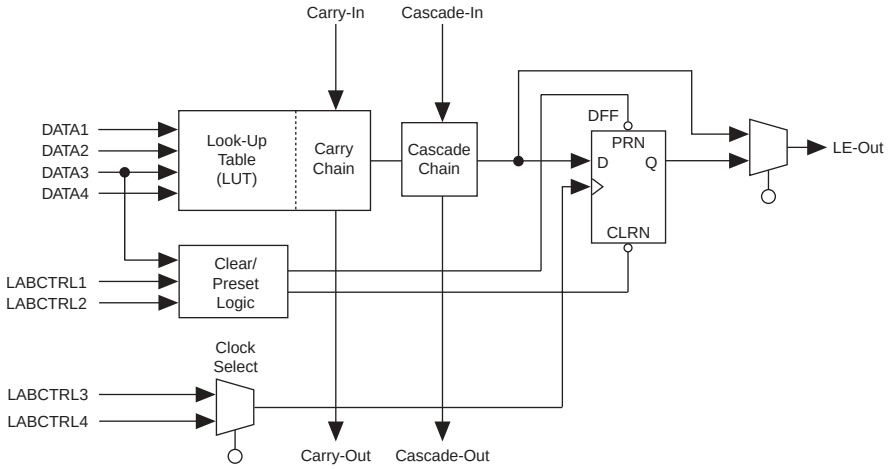
Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

## Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

*Figure 3. FLEX 8000 LE*

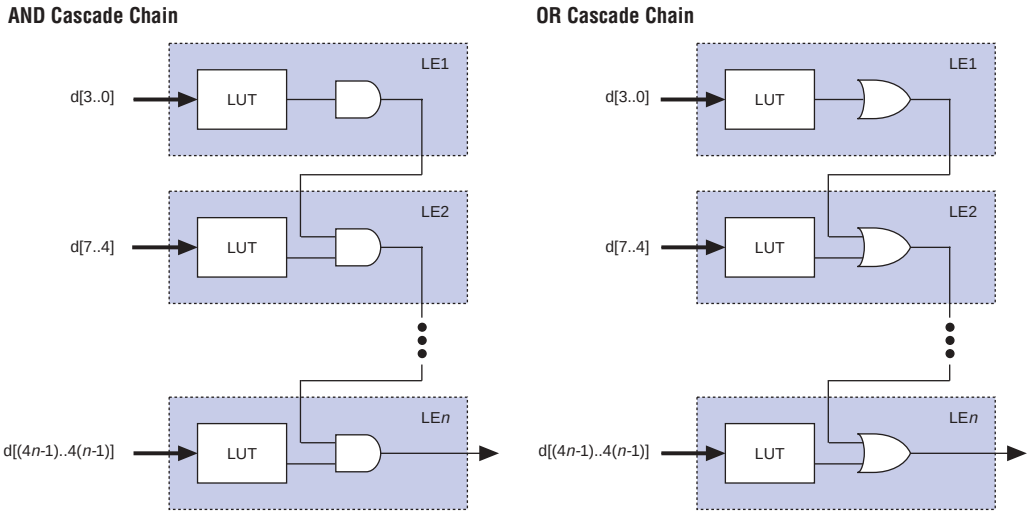



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

***Figure 5. FLEX 8000 Cascade Chain Operation***




## *LE Operating Modes*

The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

### Asynchronous Clear

A register is cleared by one of the two LABCTRL signals. When the CLRn port receives a low signal, the register is set to zero.

### Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load or an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a 1 into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### Asynchronous Clear & Preset

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. The DATA3 input is tied to VCC; therefore, asserting LABCTRL1 asynchronously loads a 1 into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### Asynchronous Load with Clear

When implementing an asynchronous load with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear.

### Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 clears the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives the DATA3 signal to account for the inversion of the register's output.

### Asynchronous Load without Clear or Preset

When implementing an asynchronous load without the clear or preset, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

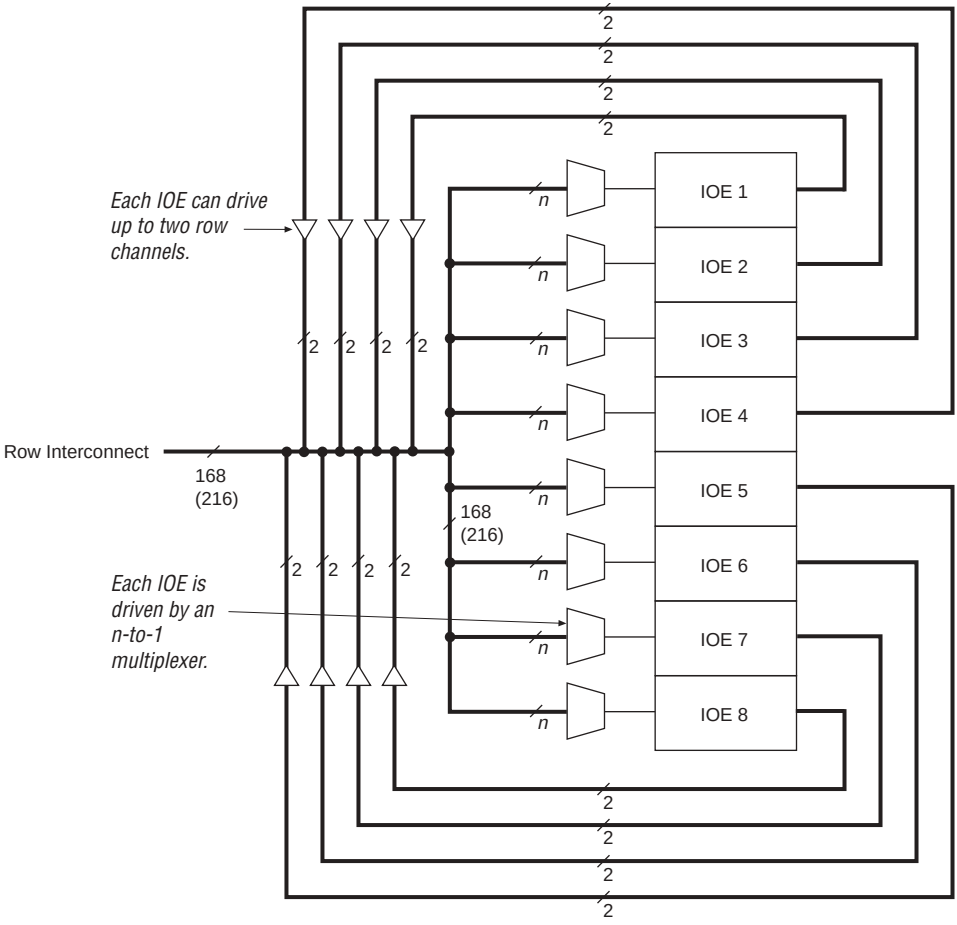
*Table 4. FLEX 8000 FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF8282A<br>EPF8282AV | 2 | 168 | 13 | 16 |
| EPF8452A | 2 | 168 | 21 | 16 |
| EPF8636A | 3 | 168 | 21 | 16 |
| EPF8820A | 4 | 168 | 21 | 16 |
| EPF81188A | 6 | 168 | 21 | 16 |
| EPF81500A | 6 | 216 | 27 | 16 |

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

***Figure 11. FLEX 8000 Row-to-IOE Connections***

*Numbers in parentheses are for EPF81500A devices. See Note (1).*




***Note:***

(1) $n$ = 13 for EPF8282A and EPF8282AV devices.
$n$ = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
$n$ = 27 for EPF81500A devices.

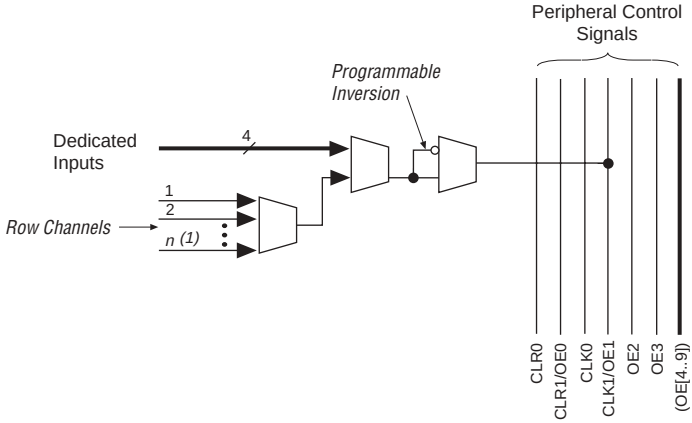
## *Column-to-IOE Connections*

Two IOEs are located at the top and bottom of the column channels (see Figure 12). When an IOE is used as an input, it can drive up to two separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

***Figure 13. FLEX 8000 Peripheral Bus***

*Numbers in parentheses are for EPF81500A devices.*




***Note:***

(1) $n$ = 13 for EPF8282A and EPF8282AV devices.
$n$ = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
$n$ = 27 for EPF81500A devices.

*Table 10. FLEX 8000 5.0-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 11. FLEX 8000 5.0-V Device DC Operating Conditions* *Notes (5), (6)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CCINT}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC *(7)*<br>$V_{CCIO}$ = 4.75 V | 2.4 | | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | $V_{CCIO}$ – 0.2 | | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC *(7)*<br>$V_{CCIO}$ = 4.75 V | | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | | | 0.2 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or ground | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or ground | –40 | | 40 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load | | 0.5 | 10 | mA |

*Table 15. FLEX 8000 3.3-V Device DC Operating Conditions* *Note (4)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –0.1 mA DC *(5)* | $V_{CC}$ – 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA DC *(5)* | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or ground | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or ground | –40 | | 40 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load *(6)* | | 0.3 | 10 | mA |

*Table 16. FLEX 8000 3.3-V Device Capacitance* *Note (7)*

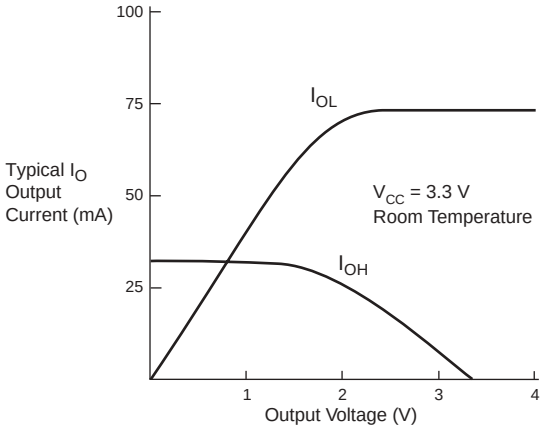
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum $V_{CC}$ rise time is 100 ms. $V_{CC}$ must rise monotonically.
(4) These values are specified in Table 14 on page 29.
(5) The $I_{OH}$ parameter refers to high-level TTL output current; the $I_{OL}$ parameter refers to low-level TTL output current.
(6) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 3.3 V.
(7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

*Figure 18. Output Drive Characteristics of EPF8282AV Devices*




## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

| Table 19. FLEX 8000 Interconnect Timing Parameters Note (1) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs |
| $t_{LOCAL}$ | LAB local interconnect delay |
| $t_{ROW}$ | Row interconnect routing delay *(4)* |
| $t_{COL}$ | Column interconnect routing delay |
| $t_{DIN\_C}$ | Dedicated input to LE control delay |
| $t_{DIN\_D}$ | Dedicated input to LE data delay *(4)* |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay |

| Table 20. FLEX 8000 External Reference Timing Characteristics Note (5) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)* |
| $t_{ODH}$ | Output data hold time after clock *(7)* |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the $t_{OD3}$ and $t_{ZX3}$ parameters, $V_{CCIO}$ = 3.3 V or 5.0 V.
(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

*Figure 19. FLEX 8000 Timing Model*

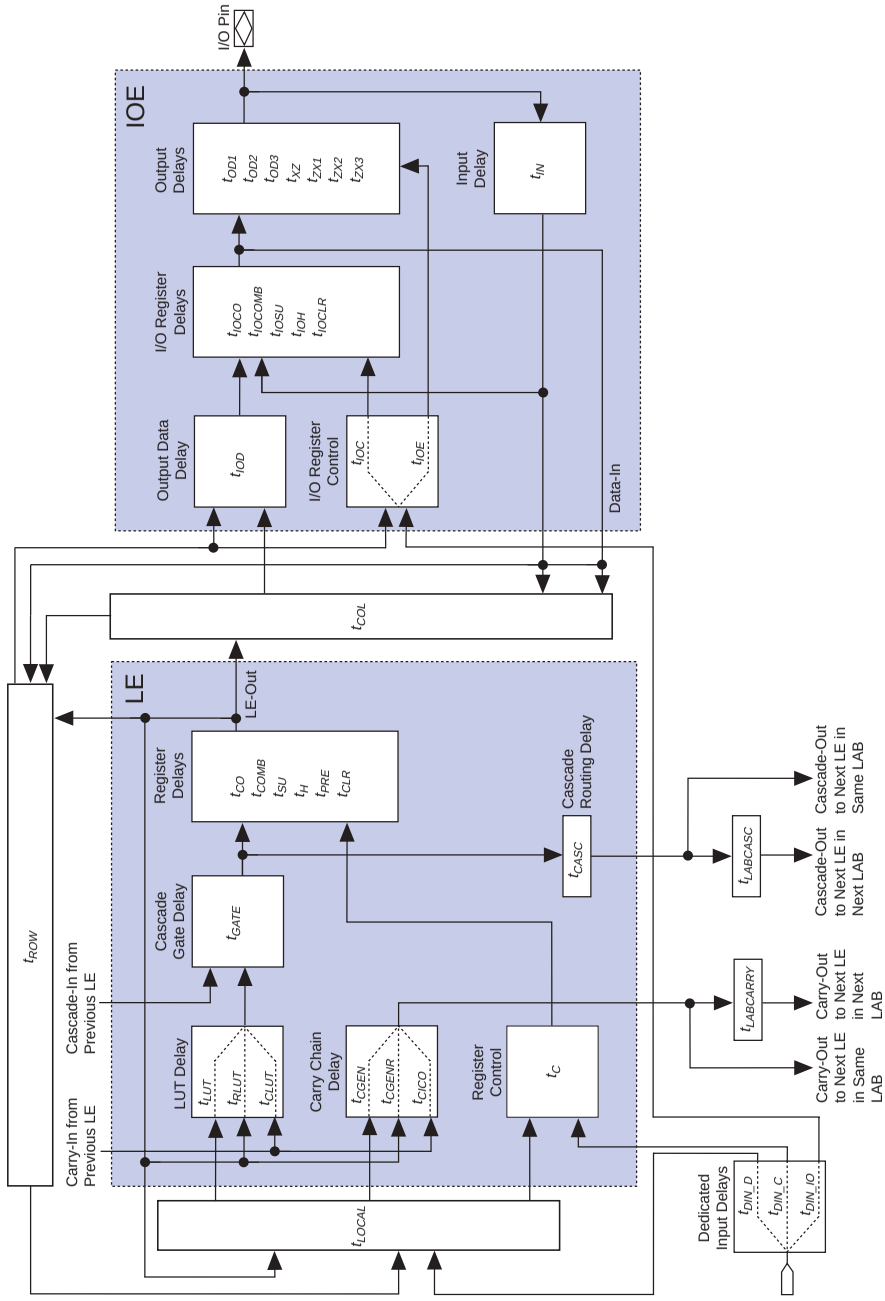


*Table 23. EPF8282A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 4.2 | | 4.2 | | 4.2 | ns |
| $t_{COL}$ | | 2.5 | | 2.5 | | 2.5 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.2 | | 7.2 | | 7.2 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 30. EPF8452A I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | – | | – | | – | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | – | | – | | – | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 31. EPF8452A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{ROW}$ | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 32. EPF8452A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.3 | | 3.0 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.2 | | 0.1 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.6 | | 1.6 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.9 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.4 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.0 | | 1.1 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.4 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 33. EPF8452A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.0 | | 20.0 | | 25.0 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 44. EPF81188A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 45. EPF81188A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.0 | | 20.0 | | 25.0 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 84-Pin PLCC EPF8282A | 84-Pin PLCC EPF8452A EPF8636A | 100-Pin TQFP EPF8282A EPF8282AV | 100-Pin TQFP EPF8452A | 144-Pin TQFP EPF8820A | 160-Pin PGA EPF8452A | 160-Pin PQFP EPF8820A *(1)* |
|---|---|---|---|---|---|---|---|
| ADD0 | 78 | 76 | 78 | 77 | 106 | N3 | 6 |
| DATA7 | 3 | 2 | 90 | 89 | 131 | P8 | 140 |
| DATA6 | 4 | 4 | 91 | 91 | 132 | P10 | 139 |
| DATA5 | 6 | 6 | 92 | 95 | 133 | R12 | 138 |
| DATA4 | 7 | 7 | 95 | 96 | 134 | R13 | 136 |
| DATA3 | 8 | 8 | 97 | 97 | 135 | P13 | 135 |
| DATA2 | 9 | 9 | 99 | 98 | 137 | R14 | 133 |
| DATA1 | 13 | 13 | 4 | 4 | 138 | N15 | 132 |
| DATA0 | 14 | 14 | 5 | 5 | 140 | K13 | 129 |
| SDOUT *(3)* | 79 | 78 | 79 | 79 | 23 | P4 | 97 |
| TDI *(4)* | 55 | 45 *(5)* | 54 | – | 96 | – | 17 |
| TDO *(4)* | 27 | 27 *(5)* | 18 | – | 18 | – | 102 |
| TCK *(4)*, *(6)* | 72 | 44 *(5)* | 72 | – | 88 | – | 27 |
| TMS *(4)* | 20 | 43 *(5)* | 11 | – | 86 | – | 29 |
| TRST *(7)* | 52 | 52 *(8)* | 50 | – | 71 | – | 45 |
| Dedicated Inputs *(10)* | 12, 31, 54, 73 | 12, 31, 54, 73 | 3, 23, 53, 73 | 3, 24, 53, 74 | 9, 26, 82, 99 | C3, D14, N2, R15 | 14, 33, 94, 113 |
| VCCINT | 17, 38, 59, 80 | 17, 38, 59, 80 | 6, 20, 37, 56, 70, 87 | 9, 32, 49, 59, 82 | 8, 28, 70, 90, 111 | B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12 | 3, 24, 46, 92, 114, 160 |
| VCCIO | – | – | – | – | 16, 40, 60, 69, 91, 112, 122, 141 | – | 23, 47, 57, 69, 79, 104, 127, 137, 149, 159 |

*Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)*

| Pin Name | 160-Pin PQFP EPF8452A | 160-Pin PQFP EPF8636A | 192-Pin PGA EPF8636A EPF8820A | 208-Pin PQFP EPF8636A *(1)* | 208-Pin PQFP EPF8820A *(1)* | 208-Pin PQFP EPF81188A *(1)* |
|---|---|---|---|---|---|---|
| nSP *(2)* | 120 | 1 | R15 | 207 | 207 | 5 |
| MSEL0 *(2)* | 117 | 3 | T15 | 4 | 4 | 21 |
| MSEL1 *(2)* | 84 | 38 | T3 | 49 | 49 | 33 |
| nSTATUS *(2)* | 37 | 83 | B3 | 108 | 108 | 124 |
| nCONFIG *(2)* | 40 | 81 | C3 | 103 | 103 | 107 |
| DCLK *(2)* | 1 | 120 | C15 | 158 | 158 | 154 |
| CONF_DONE *(2)* | 4 | 118 | B15 | 153 | 153 | 138 |
| nWS | 30 | 89 | C5 | 114 | 114 | 118 |
| nRS | 71 | 50 | B5 | 66 | 116 | 121 |
| RDCLK | 73 | 48 | C11 | 64 | 137 | 137 |
| nCS | 29 | 91 | B13 | 116 | 145 | 142 |
| CS | 27 | 93 | A16 | 118 | 148 | 144 |
| RDYnBUSY | 125 | 155 | A8 | 201 | 127 | 128 |
| CLKUSR | 76 | 44 | A10 | 59 | 134 | 134 |
| ADD17 | 78 | 43 | R5 | 57 | 43 | 46 |
| ADD16 | 91 | 33 | U3 | 43 | 42 | 45 |
| ADD15 | 92 | 31 | T5 | 41 | 41 | 44 |
| ADD14 | 94 | 29 | U4 | 39 | 40 | 39 |
| ADD13 | 95 | 27 | R6 | 37 | 39 | 37 |
| ADD12 | 96 | 24 | T6 | 31 | 35 | 36 |
| ADD11 | 97 | 23 | R7 | 30 | 33 | 31 |
| ADD10 | 98 | 22 | T7 | 29 | 31 | 30 |
| ADD9 | 99 | 21 | T8 | 28 | 29 | 29 |
| ADD8 | 101 | 20 | U9 | 24 | 25 | 26 |
| ADD7 | 102 | 19 | U10 | 23 | 23 | 25 |
| ADD6 | 103 | 18 | U11 | 22 | 21 | 24 |
| ADD5 | 104 | 17 | U12 | 21 | 19 | 18 |
| ADD4 | 105 | 13 | R12 | 14 | 14 | 17 |
| ADD3 | 106 | 11 | U14 | 12 | 13 | 16 |
| ADD2 | 109 | 9 | U15 | 10 | 11 | 10 |
| ADD1 | 110 | 7 | R13 | 8 | 10 | 9 |
| ADD0 | 123 | 157 | U16 | 203 | 9 | 8 |
| DATA7 | 144 | 137 | H17 | 178 | 178 | 177 |
| DATA6 | 150 | 132 | G17 | 172 | 176 | 175 |
| DATA5 | 152 | 129 | F17 | 169 | 174 | 172 |

*Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)*

| Pin Name | 225-Pin BGA EPF8820A | 232-Pin PGA EPF81188A | 240-Pin PQFP EPF81188A | 240-Pin PQFP EPF81500A | 280-Pin PGA EPF81500A | 304-Pin RQFP EPF81500A |
|---|---|---|---|---|---|---|
| nSP *(2)* | A15 | C14 | 237 | 237 | W1 | 304 |
| MSEL0 *(2)* | B14 | G15 | 21 | 19 | N1 | 26 |
| MSEL1 *(2)* | R15 | L15 | 40 | 38 | H3 | 51 |
| nSTATUS *(2)* | P2 | L3 | 141 | 142 | G19 | 178 |
| nCONFIG *(2)* | R1 | R4 | 117 | 120 | B18 | 152 |
| DCLK *(2)* | B2 | C4 | 184 | 183 | U18 | 230 |
| CONF_DONE *(2)* | A1 | G3 | 160 | 161 | M16 | 204 |
| nWS | L4 | P1 | 133 | 134 | F18 | 167 |
| nRS | K5 | N1 | 137 | 138 | G18 | 171 |
| RDCLK | F1 | G2 | 158 | 159 | M17 | 202 |
| nCS | D1 | E2 | 166 | 167 | N16 | 212 |
| CS | C1 | E3 | 169 | 170 | N18 | 215 |
| RDYnBUSY | J3 | K2 | 146 | 147 | J17 | 183 |
| CLKUSR | G2 | H2 | 155 | 156 | K19 | 199 |
| ADD17 | M14 | R15 | 58 | 56 | E3 | 73 |
| ADD16 | L12 | T17 | 56 | 54 | E2 | 71 |
| ADD15 | M15 | P15 | 54 | 52 | F4 | 69 |
| ADD14 | L13 | M14 | 47 | 45 | G1 | 60 |
| ADD13 | L14 | M15 | 45 | 43 | H2 | 58 |
| ADD12 | K13 | M16 | 43 | 41 | H1 | 56 |
| ADD11 | K15 | K15 | 36 | 34 | J3 | 47 |
| ADD10 | J13 | K17 | 34 | 32 | K3 | 45 |
| ADD9 | J15 | J14 | 32 | 30 | K4 | 43 |
| ADD8 | G14 | J15 | 29 | 27 | L1 | 34 |
| ADD7 | G13 | H17 | 27 | 25 | L2 | 32 |
| ADD6 | G11 | H15 | 25 | 23 | M1 | 30 |
| ADD5 | F14 | F16 | 18 | 16 | N2 | 20 |
| ADD4 | E13 | F15 | 16 | 14 | N3 | 18 |
| ADD3 | D15 | F14 | 14 | 12 | N4 | 16 |
| ADD2 | D14 | D15 | 7 | 5 | U1 | 8 |
| ADD1 | E12 | B17 | 5 | 3 | U2 | 6 |
| ADD0 | C15 | C15 | 3 | 1 | V1 | 4 |
| DATA7 | A7 | A7 | 205 | 199 | W13 | 254 |
| DATA6 | D7 | D8 | 203 | 197 | W14 | 252 |
| DATA5 | A6 | B7 | 200 | 196 | W15 | 250 |

*Notes to tables:*

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a $V_{CC}$ pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) SDOUT does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

## Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.