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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                       |
|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                              |
| Number of LABs/CLBs            | 126                                                                                                                                   |
| Number of Logic Elements/Cells | 1008                                                                                                                                  |
| Total RAM Bits                 | -                                                                                                                                     |
| Number of I/O                  | 184                                                                                                                                   |
| Number of Gates                | 12000                                                                                                                                 |
| Voltage - Supply               | 4.75V ~ 5.25V                                                                                                                         |
| Mounting Type                  | Surface Mount                                                                                                                         |
| Operating Temperature          | 0°C ~ 70°C (TA)                                                                                                                       |
| Package / Case                 | 240-BFQFP                                                                                                                             |
| Supplier Device Package        | 240-PQFP (32x32)                                                                                                                      |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/epf81188aqc240-2">https://www.e-xfl.com/product-detail/intel/epf81188aqc240-2</a> |

|                    |     |    |     |     |    |     |
|--------------------|-----|----|-----|-----|----|-----|
| JTAG BST circuitry | Yes | No | Yes | Yes | No | Yes |
|--------------------|-----|----|-----|-----|----|-----|

## ...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see [Table 2](#))
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

**Table 2. FLEX 8000 Package Options & I/O Pin Count** *Note (1)*

| Device    | 84-Pin PLCC | 100-Pin TQFP | 144-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 225-Pin BGA | 232-Pin PGA | 240-Pin PQFP | 280-Pin PGA | 304-Pin RQFP |
|-----------|-------------|--------------|--------------|--------------|-------------|-------------|--------------|-------------|-------------|--------------|-------------|--------------|
| EPF8282A  | 68          | 78           |              |              |             |             |              |             |             |              |             |              |
| EPF8282AV |             | 78           |              |              |             |             |              |             |             |              |             |              |
| EPF8452A  | 68          | 68           |              | 120          | 120         |             |              |             |             |              |             |              |
| EPF8636A  | 68          |              |              | 118          |             | 136         | 136          |             |             |              |             |              |
| EPF8820A  |             |              | 112          | 120          |             | 152         | 152          | 152         |             |              |             |              |
| EPF81188A |             |              |              |              |             |             | 148          |             | 184         | 184          |             |              |
| EPF81500A |             |              |              |              |             |             |              |             |             | 181          | 208         | 208          |

**Note:**

- (1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

## General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide-data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. [Table 3](#) shows FLEX 8000 performance and LE requirements for typical applications.

**Table 3. FLEX 8000 Performance**

| Application             | LEs Used | Speed Grade |     |     | Units |
|-------------------------|----------|-------------|-----|-----|-------|
|                         |          | A-2         | A-3 | A-4 |       |
| 16-bit loadable counter | 16       | 125         | 95  | 83  | MHz   |
| 16-bit up/down counter  | 16       | 125         | 95  | 83  | MHz   |
| 24-bit accumulator      | 24       | 87          | 67  | 58  | MHz   |
| 16-bit address decode   | 4        | 4.2         | 4.9 | 6.3 | ns    |
| 16-to-1 multiplexer     | 10       | 6.6         | 7.9 | 9.5 | ns    |

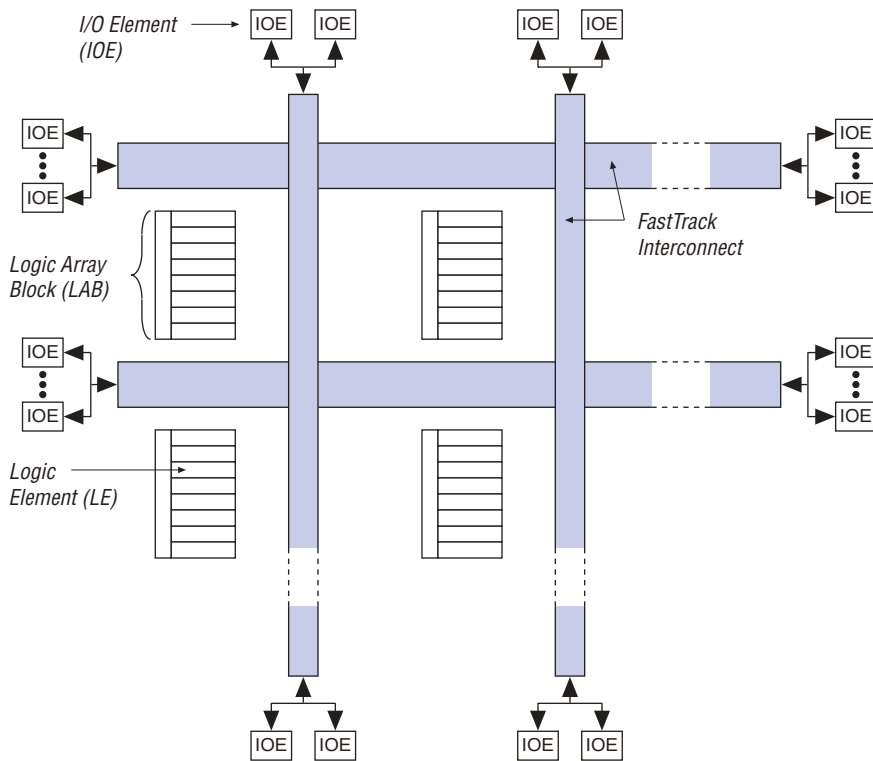
All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial configuration devices, or with data provided by a system controller. Altera offers the EPC1, EPC1213, EPC1064, and EPC1441 configuration devices, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32 K × 8 bit or larger configuration device, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation. For information on how to configure FLEX 8000 devices, go to the following documents:

- [Configuration Devices for APEX & FLEX Devices Data Sheet](#)
- [BitBlaster Serial Download Cable Data Sheet](#)
- [ByteBlasterMV Parallel Port Download Cable Data Sheet](#)
- [Application Note 33 \(Configuring FLEX 8000 Devices\)](#)
- [Application Note 38 \(Configuring Multiple FLEX 8000 Devices\)](#)

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

**Figure 1. FLEX 8000 Device Block Diagram**

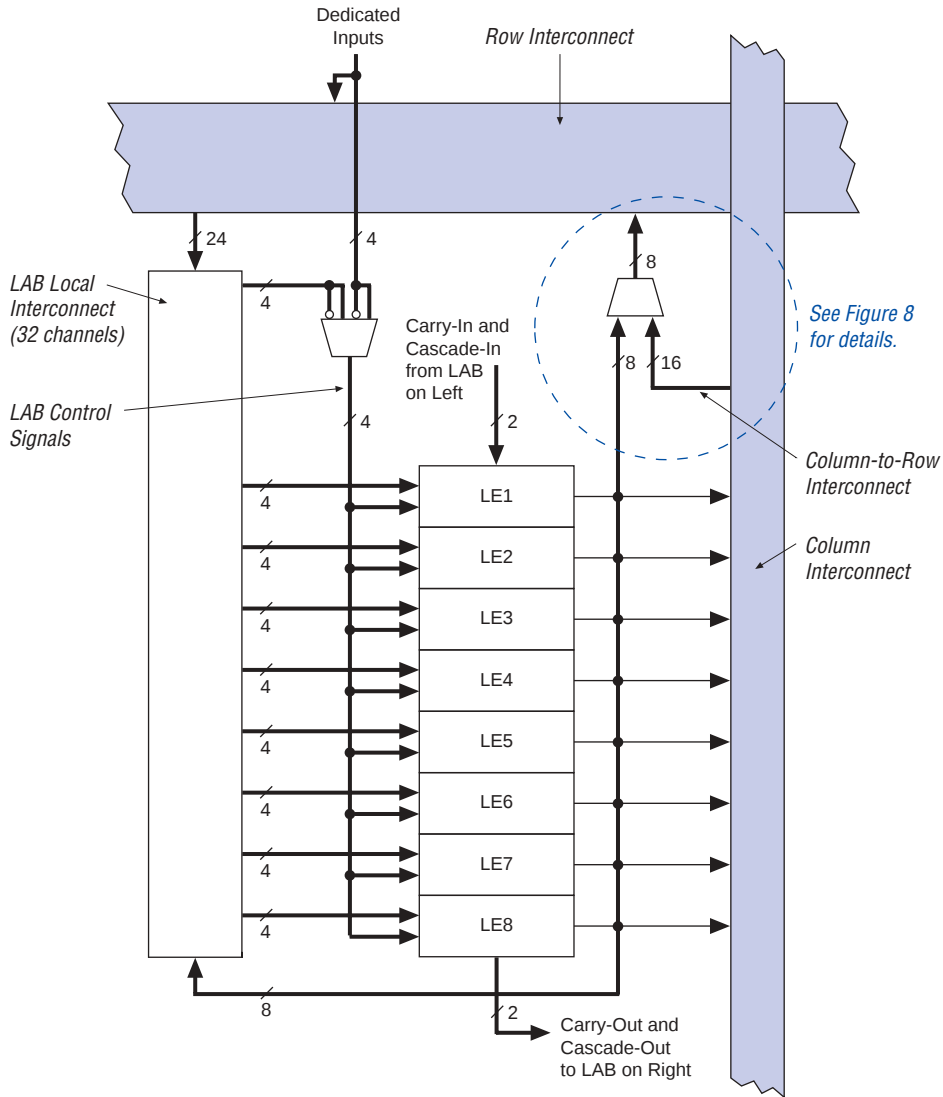


Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block



### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

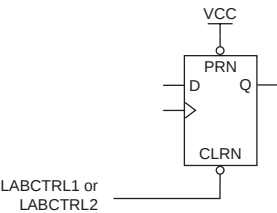
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See [Figure 7](#).

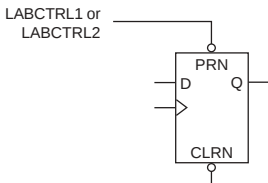
- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes

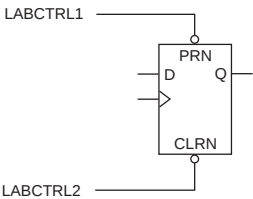
Asynchronous Clear



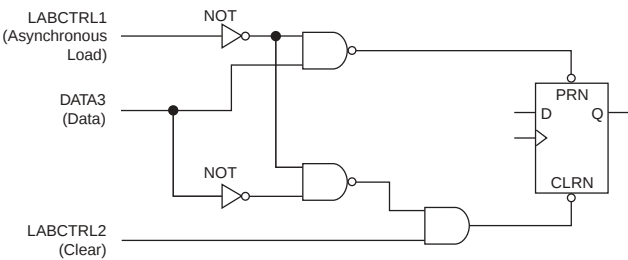
Asynchronous Preset



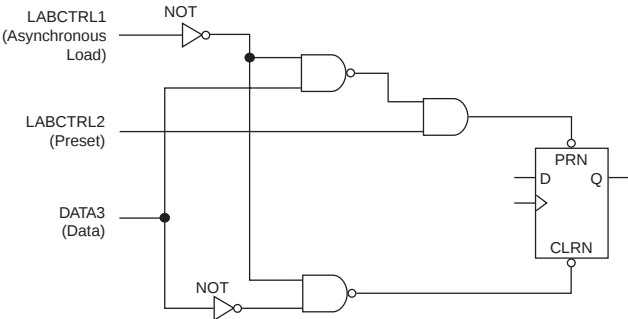
Asynchronous Clear & Preset



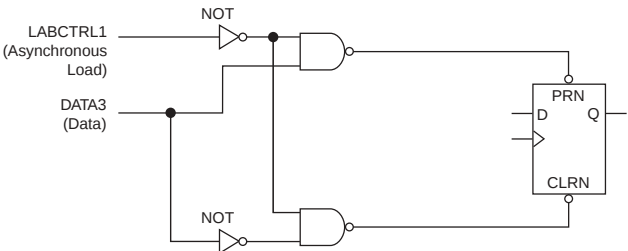
Asynchronous Load with Clear



Asynchronous Load with Preset



Asynchronous Load without Clear or Preset

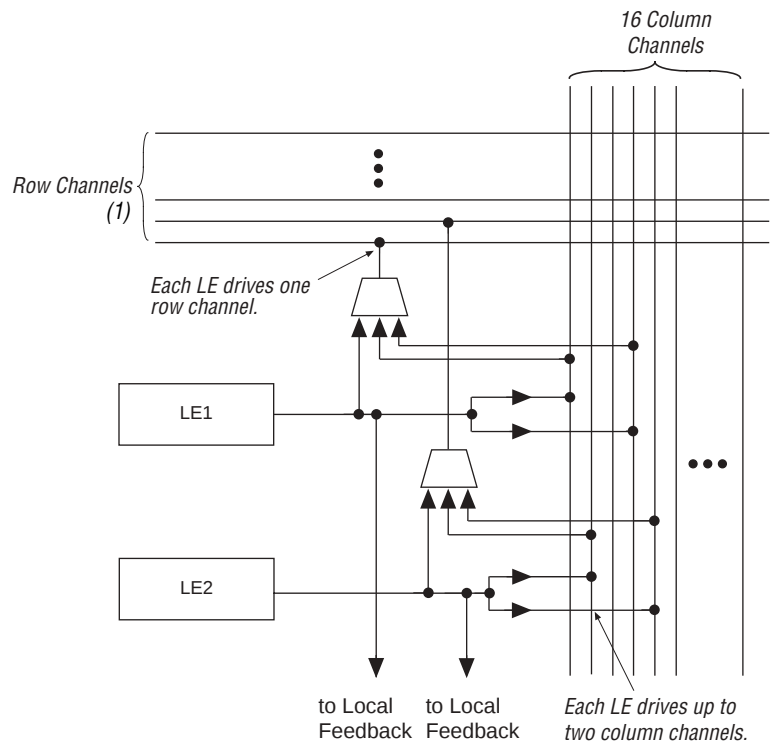


FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal (row) and vertical (column) routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing structure in FPGAs requires switch matrices to connect a variable number of routing paths, which increases the delays between logic resources and reduces performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. **Figure 8** shows how an LE drives the row and column interconnect.

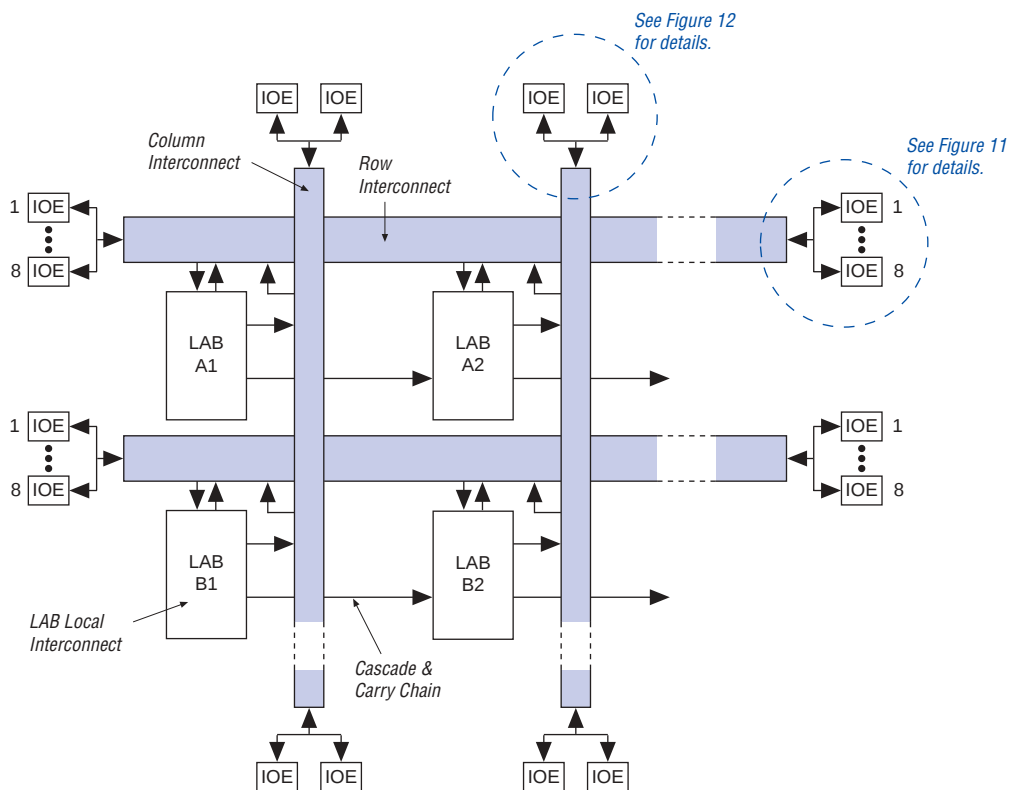
Figure 8. FLEX 8000 LAB Connections to Row & Column Interconnect



**Note:**  
(1) See [Table 4](#) for the number of row channels.

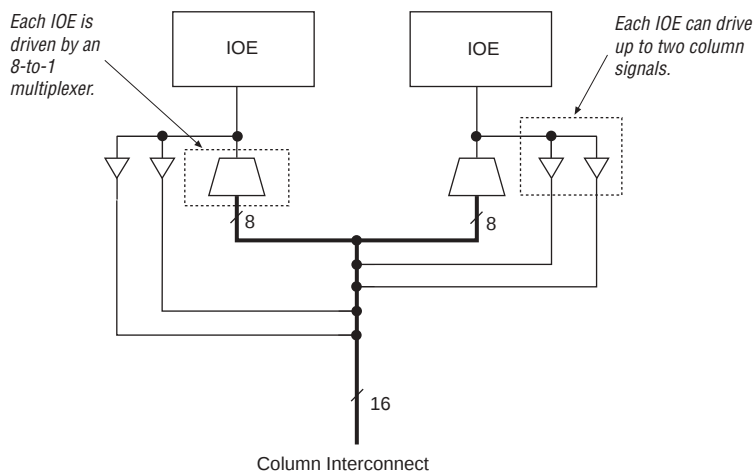
**Figure 9. FLEX 8000 Device Interconnect Resources**

Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. [Figure 10](#) shows the IOE block diagram.

**Figure 12. FLEX 8000 Column-to-IOE Connections**

In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This “peripheral bus” can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. [Figure 13 on page 22](#) shows how two output enable signals are shared with one clock and one clear signal.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

| <b>Table 5. Row Sources of FLEX 8000 Peripheral Control Signals</b> |                               |                 |                 |                 |                  |                  |
|---------------------------------------------------------------------|-------------------------------|-----------------|-----------------|-----------------|------------------|------------------|
| <b>Peripheral Control Signal</b>                                    | <b>EPF8282A<br/>EPF8282AV</b> | <b>EPF8452A</b> | <b>EPF8636A</b> | <b>EPF8820A</b> | <b>EPF81188A</b> | <b>EPF81500A</b> |
| CLK0                                                                | Row A                         | Row A           | Row A           | Row A           | Row E            | Row E            |
| CLK1/OE1                                                            | Row B                         | Row B           | Row C           | Row C           | Row B            | Row B            |
| CLR0                                                                | Row A                         | Row A           | Row B           | Row B           | Row F            | Row F            |
| CLR1/OE0                                                            | Row B                         | Row B           | Row C           | Row D           | Row C            | Row C            |
| OE2                                                                 | Row A                         | Row A           | Row A           | Row A           | Row D            | Row A            |
| OE3                                                                 | Row B                         | Row B           | Row B           | Row B           | Row A            | Row A            |
| OE4                                                                 | —                             | —               | —               | —               | —                | Row B            |
| OE5                                                                 | —                             | —               | —               | —               | —                | Row C            |
| OE6                                                                 | —                             | —               | —               | —               | —                | Row D            |
| OE7                                                                 | —                             | —               | —               | —               | —                | Row D            |
| OE8                                                                 | —                             | —               | —               | —               | —                | Row E            |
| OE9                                                                 | —                             | —               | —               | —               | —                | Row F            |

## Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

### Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.



For more information on high-speed system design, go to [Application Note 75 \(High-Speed Board Designs\)](#).

**Table 12. FLEX 8000 5.0-V Device Capacitance** *Note (8)*

| Symbol    | Parameter          | Conditions                                    | Min | Max | Unit |
|-----------|--------------------|-----------------------------------------------|-----|-----|------|
| $C_{IN}$  | Input capacitance  | $V_{IN} = 0\text{ V}$ , $f = 1.0\text{ MHz}$  |     | 10  | pF   |
| $C_{OUT}$ | Output capacitance | $V_{OUT} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ |     | 10  | pF   |

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is  $-0.5\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $7.0\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) The maximum  $V_{CC}$  rise time is  $100\text{ ms}$ .
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Typical values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5.0\text{ V}$ .
- (6) These values are specified in Table 10 on page 28.
- (7) The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current; the  $I_{OL}$  parameter refers to low-level TTL or CMOS output current.
- (8) Capacitance is sample-tested only.

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 3.3-V FLEX 8000 devices.

**Table 13. FLEX 8000 3.3-V Device Absolute Maximum Ratings** *Note (1)*

| Symbol    | Parameter                  | Conditions                   | Min    | Max | Unit             |
|-----------|----------------------------|------------------------------|--------|-----|------------------|
| $V_{CC}$  | Supply voltage             | With respect to ground (2)   | $-2.0$ | 5.3 | V                |
| $V_I$     | DC input voltage           |                              | $-2.0$ | 5.3 | V                |
| $I_{OUT}$ | DC output current, per pin |                              | $-25$  | 25  | mA               |
| $T_{STG}$ | Storage temperature        | No bias                      | $-65$  | 150 | $^\circ\text{C}$ |
| $T_{AMB}$ | Ambient temperature        | Under bias                   | $-65$  | 135 | $^\circ\text{C}$ |
| $T_J$     | Junction temperature       | Plastic packages, under bias |        | 135 | $^\circ\text{C}$ |

**Table 14. FLEX 8000 3.3-V Device Recommended Operating Conditions**

| Symbol   | Parameter             | Conditions         | Min    | Max            | Unit             |
|----------|-----------------------|--------------------|--------|----------------|------------------|
| $V_{CC}$ | Supply voltage        | (3)                | 3.0    | 3.6            | V                |
| $V_I$    | Input voltage         |                    | $-0.3$ | $V_{CC} + 0.3$ | V                |
| $V_O$    | Output voltage        |                    | 0      | $V_{CC}$       | V                |
| $T_A$    | Operating temperature | For commercial use | 0      | 70             | $^\circ\text{C}$ |
| $t_R$    | Input rise time       |                    |        | 40             | ns               |
| $t_F$    | Input fall time       |                    |        | 40             | ns               |

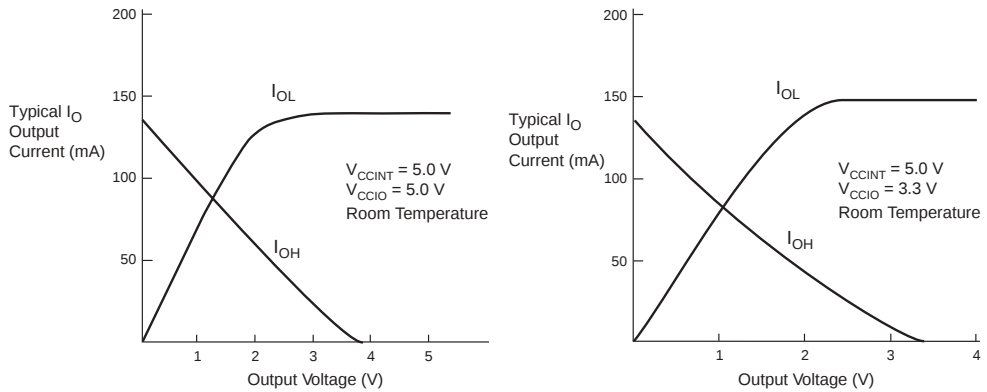
**Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)**

Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

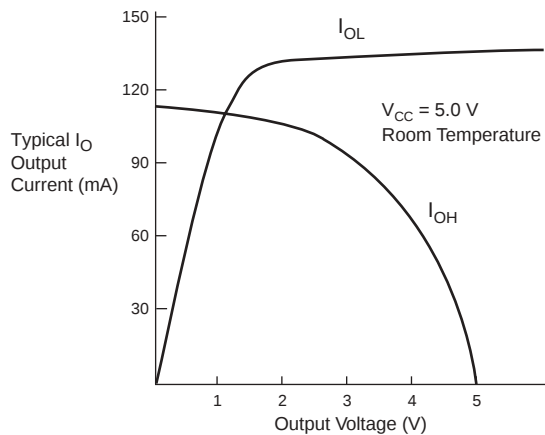
**Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V  $V_{CCIO}$** 

Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

**Table 23. EPF8282A Interconnect Timing Parameters**

| Symbol         | Speed Grade |     |     |     |     |     | Unit |
|----------------|-------------|-----|-----|-----|-----|-----|------|
|                | A-2         |     | A-3 |     | A-4 |     |      |
|                | Min         | Max | Min | Max | Min | Max |      |
| $t_{LABCASC}$  |             | 0.3 |     | 0.3 |     | 0.4 | ns   |
| $t_{LABCARRY}$ |             | 0.3 |     | 0.3 |     | 0.4 | ns   |
| $t_{LOCAL}$    |             | 0.5 |     | 0.6 |     | 0.8 | ns   |
| $t_{ROW}$      |             | 4.2 |     | 4.2 |     | 4.2 | ns   |
| $t_{COL}$      |             | 2.5 |     | 2.5 |     | 2.5 | ns   |
| $t_{DIN\_C}$   |             | 5.0 |     | 5.0 |     | 5.5 | ns   |
| $t_{DIN\_D}$   |             | 7.2 |     | 7.2 |     | 7.2 | ns   |
| $t_{DIN\_IO}$  |             | 5.0 |     | 5.0 |     | 5.5 | ns   |

**Table 24. EPF8282A LE Timing Parameters**

| Symbol      | Speed Grade |     |     |     |     |     | Unit |
|-------------|-------------|-----|-----|-----|-----|-----|------|
|             | A-2         |     | A-3 |     | A-4 |     |      |
|             | Min         | Max | Min | Max | Min | Max |      |
| $t_{LUT}$   |             | 2.0 |     | 2.5 |     | 3.2 | ns   |
| $t_{CLUT}$  |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
| $t_{RLUT}$  |             | 0.9 |     | 1.1 |     | 1.5 | ns   |
| $t_{GATE}$  |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
| $t_{CASC}$  |             | 0.6 |     | 0.7 |     | 0.9 | ns   |
| $t_{CICO}$  |             | 0.4 |     | 0.5 |     | 0.6 | ns   |
| $t_{CGEN}$  |             | 0.4 |     | 0.5 |     | 0.7 | ns   |
| $t_{CGENR}$ |             | 0.9 |     | 1.1 |     | 1.5 | ns   |
| $t_C$       |             | 1.6 |     | 2.0 |     | 2.5 | ns   |
| $t_{CH}$    | 4.0         |     | 4.0 |     | 4.0 |     | ns   |
| $t_{CL}$    | 4.0         |     | 4.0 |     | 4.0 |     | ns   |
| $t_{CO}$    |             | 0.4 |     | 0.5 |     | 0.6 | ns   |
| $t_{COMB}$  |             | 0.4 |     | 0.5 |     | 0.6 | ns   |
| $t_{SU}$    | 0.8         |     | 1.1 |     | 1.2 |     | ns   |
| $t_H$       | 0.9         |     | 1.1 |     | 1.5 |     | ns   |
| $t_{PRE}$   |             | 0.6 |     | 0.7 |     | 0.8 | ns   |
| $t_{CLR}$   |             | 0.6 |     | 0.7 |     | 0.8 | ns   |

**Table 25. EPF8282A External Timing Parameters**

| Symbol           | Speed Grade |      |     |      |     |      | Unit |
|------------------|-------------|------|-----|------|-----|------|------|
|                  | A-2         |      | A-3 |      | A-4 |      |      |
|                  | Min         | Max  | Min | Max  | Min | Max  |      |
| t <sub>DRR</sub> |             | 15.8 |     | 19.8 |     | 24.8 | ns   |
| t <sub>ODH</sub> | 1.0         |      | 1.0 |      | 1.0 |      | ns   |

**Table 28. EPF8282AV Logic Element Timing Parameters**

| Symbol      | Speed Grade |     |     |     | Unit |
|-------------|-------------|-----|-----|-----|------|
|             | A-3         |     | A-4 |     |      |
|             | Min         | Max | Min | Max |      |
| $t_{LUT}$   |             | 3.2 |     | 7.3 | ns   |
| $t_{CLUT}$  |             | 0.0 |     | 1.4 | ns   |
| $t_{RLUT}$  |             | 1.5 |     | 5.1 | ns   |
| $t_{GATE}$  |             | 0.0 |     | 0.0 | ns   |
| $t_{CASC}$  |             | 0.9 |     | 2.8 | ns   |
| $t_{CICO}$  |             | 0.6 |     | 1.5 | ns   |
| $t_{CGEN}$  |             | 0.7 |     | 2.2 | ns   |
| $t_{CGENR}$ |             | 1.5 |     | 3.7 | ns   |
| $t_C$       |             | 2.5 |     | 4.7 | ns   |
| $t_{CH}$    | 4.0         |     | 6.0 |     | ns   |
| $t_{CL}$    | 4.0         |     | 6.0 |     | ns   |
| $t_{CO}$    |             | 0.6 |     | 0.9 | ns   |
| $t_{COMB}$  |             | 0.6 |     | 0.9 | ns   |
| $t_{SU}$    | 1.2         |     | 2.4 |     | ns   |
| $t_H$       | 1.5         |     | 4.6 |     | ns   |
| $t_{PRE}$   |             | 0.8 |     | 1.3 | ns   |
| $t_{CLR}$   |             | 0.8 |     | 1.3 | ns   |

**Table 29. EPF8282AV External Timing Parameters**

| Symbol           | Speed Grade |      |     |      | Unit |
|------------------|-------------|------|-----|------|------|
|                  | A-3         |      | A-4 |      |      |
|                  | Min         | Max  | Min | Max  |      |
| t <sub>DDR</sub> |             | 24.8 |     | 50.1 | ns   |
| t <sub>ODH</sub> | 1.0         |      | 1.0 |      | ns   |

**Table 36. EPF8636A LE Timing Parameters**

| Symbol      | Speed Grade |     |     |     |     |     | Unit |
|-------------|-------------|-----|-----|-----|-----|-----|------|
|             | A-2         |     | A-3 |     | A-4 |     |      |
|             | Min         | Max | Min | Max | Min | Max |      |
| $t_{LUT}$   |             | 2.0 |     | 2.3 |     | 3.0 | ns   |
| $t_{CLUT}$  |             | 0.0 |     | 0.2 |     | 0.1 | ns   |
| $t_{RLUT}$  |             | 0.9 |     | 1.6 |     | 1.6 | ns   |
| $t_{GATE}$  |             | 0.0 |     | 0.0 |     | 0.0 | ns   |
| $t_{CASC}$  |             | 0.6 |     | 0.7 |     | 0.9 | ns   |
| $t_{CICO}$  |             | 0.4 |     | 0.5 |     | 0.6 | ns   |
| $t_{CGEN}$  |             | 0.4 |     | 0.9 |     | 0.8 | ns   |
| $t_{CGENR}$ |             | 0.9 |     | 1.4 |     | 1.5 | ns   |
| $t_C$       |             | 1.6 |     | 1.8 |     | 2.4 | ns   |
| $t_{CH}$    | 4.0         |     | 4.0 |     | 4.0 |     | ns   |
| $t_{CL}$    | 4.0         |     | 4.0 |     | 4.0 |     | ns   |
| $t_{CO}$    |             | 0.4 |     | 0.5 |     | 0.6 | ns   |
| $t_{COMB}$  |             | 0.4 |     | 0.5 |     | 0.6 | ns   |
| $t_{SU}$    | 0.8         |     | 1.0 |     | 1.1 |     | ns   |
| $t_H$       | 0.9         |     | 1.1 |     | 1.4 |     | ns   |
| $t_{PRE}$   |             | 0.6 |     | 0.7 |     | 0.8 | ns   |
| $t_{CLR}$   |             | 0.6 |     | 0.7 |     | 0.8 | ns   |

**Table 37. EPF8636A External Timing Parameters**

| Symbol           | Speed Grade |      |     |      |     |      | Unit |
|------------------|-------------|------|-----|------|-----|------|------|
|                  | A-2         |      | A-3 |      | A-4 |      |      |
|                  | Min         | Max  | Min | Max  | Min | Max  |      |
| t <sub>DRR</sub> |             | 16.0 |     | 20.0 |     | 25.0 | ns   |
| t <sub>ODH</sub> | 1.0         |      | 1.0 |      | 1.0 |      | ns   |

**Table 42. EPF81188A I/O Element Timing Parameters**

| Symbol       | Speed Grade |     |     |     |     |     | Unit |
|--------------|-------------|-----|-----|-----|-----|-----|------|
|              | A-2         |     | A-3 |     | A-4 |     |      |
|              | Min         | Max | Min | Max | Min | Max |      |
| $t_{IOD}$    |             | 0.7 |     | 0.8 |     | 0.9 | ns   |
| $t_{IOC}$    |             | 1.7 |     | 1.8 |     | 1.9 | ns   |
| $t_{IOE}$    |             | 1.7 |     | 1.8 |     | 1.9 | ns   |
| $t_{IOCO}$   |             | 1.0 |     | 1.0 |     | 1.0 | ns   |
| $t_{IOCOMB}$ |             | 0.3 |     | 0.2 |     | 0.1 | ns   |
| $t_{IOSU}$   | 1.4         |     | 1.6 |     | 1.8 |     | ns   |
| $t_{IOH}$    | 0.0         |     | 0.0 |     | 0.0 |     | ns   |
| $t_{IOCLR}$  |             | 1.2 |     | 1.2 |     | 1.2 | ns   |
| $t_{IN}$     |             | 1.5 |     | 1.6 |     | 1.7 | ns   |
| $t_{OD1}$    |             | 1.1 |     | 1.4 |     | 1.7 | ns   |
| $t_{OD2}$    |             | 1.6 |     | 1.9 |     | 2.2 | ns   |
| $t_{OD3}$    |             | 4.6 |     | 4.9 |     | 5.2 | ns   |
| $t_{XZ}$     |             | 1.4 |     | 1.6 |     | 1.8 | ns   |
| $t_{ZX1}$    |             | 1.4 |     | 1.6 |     | 1.8 | ns   |
| $t_{ZX2}$    |             | 1.9 |     | 2.1 |     | 2.3 | ns   |
| $t_{ZX3}$    |             | 4.9 |     | 5.1 |     | 5.3 | ns   |

**Table 43. EPF81188A Interconnect Timing Parameters**

| Symbol         | Speed Grade |     |     |     |     |     | Unit |
|----------------|-------------|-----|-----|-----|-----|-----|------|
|                | A-2         |     | A-3 |     | A-4 |     |      |
|                | Min         | Max | Min | Max | Min | Max |      |
| $t_{LABCASC}$  |             | 0.3 |     | 0.3 |     | 0.4 | ns   |
| $t_{LABCARRY}$ |             | 0.3 |     | 0.3 |     | 0.4 | ns   |
| $t_{LOCAL}$    |             | 0.5 |     | 0.6 |     | 0.8 | ns   |
| $t_{ROW}$      |             | 5.0 |     | 5.0 |     | 5.0 | ns   |
| $t_{COL}$      |             | 3.0 |     | 3.0 |     | 3.0 | ns   |
| $t_{DIN\_C}$   |             | 5.0 |     | 5.0 |     | 5.5 | ns   |
| $t_{DIN\_D}$   |             | 7.0 |     | 7.0 |     | 7.5 | ns   |
| $t_{DIN\_IO}$  |             | 5.0 |     | 5.0 |     | 5.5 | ns   |

## Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)**

| Pin Name      | 84-Pin<br>PLCC<br>EPF8282A | 84-Pin<br>PLCC<br>EPF8452A<br>EPF8636A | 100-Pin<br>TQFP<br>EPF8282A<br>EPF8282AV | 100-Pin<br>TQFP<br>EPF8452A | 144-Pin<br>TQFP<br>EPF8820A | 160-Pin<br>PGA<br>EPF8452A | 160-Pin<br>PQFP<br>EPF8820A<br>(1) |
|---------------|----------------------------|----------------------------------------|------------------------------------------|-----------------------------|-----------------------------|----------------------------|------------------------------------|
| nSP (2)       | 75                         | 75                                     | 75                                       | 76                          | 110                         | R1                         | 1                                  |
| MSEL0 (2)     | 74                         | 74                                     | 74                                       | 75                          | 109                         | P2                         | 2                                  |
| MSEL1 (2)     | 53                         | 53                                     | 51                                       | 51                          | 72                          | A1                         | 44                                 |
| nSTATUS (2)   | 32                         | 32                                     | 24                                       | 25                          | 37                          | C13                        | 82                                 |
| nCONFIG (2)   | 33                         | 33                                     | 25                                       | 26                          | 38                          | A15                        | 81                                 |
| DCLK (2)      | 10                         | 10                                     | 100                                      | 100                         | 143                         | P14                        | 125                                |
| CONF_DONE (2) | 11                         | 11                                     | 1                                        | 1                           | 144                         | N13                        | 124                                |
| nWS           | 30                         | 30                                     | 22                                       | 23                          | 33                          | F13                        | 87                                 |
| nRS           | 48                         | 48                                     | 42                                       | 45                          | 31                          | C6                         | 89                                 |
| RDCLK         | 49                         | 49                                     | 45                                       | 46                          | 12                          | B5                         | 110                                |
| nCS           | 29                         | 29                                     | 21                                       | 22                          | 4                           | D15                        | 118                                |
| CS            | 28                         | 28                                     | 19                                       | 21                          | 3                           | E15                        | 121                                |
| RDYnBUSY      | 77                         | 77                                     | 77                                       | 78                          | 20                          | P3                         | 100                                |
| CLKUSR        | 50                         | 50                                     | 47                                       | 47                          | 13                          | C5                         | 107                                |
| ADD17         | 51                         | 51                                     | 49                                       | 48                          | 75                          | B4                         | 40                                 |
| ADD16         | 36                         | 55                                     | 28                                       | 54                          | 76                          | E2                         | 39                                 |
| ADD15         | 56                         | 56                                     | 55                                       | 55                          | 77                          | D1                         | 38                                 |
| ADD14         | 57                         | 57                                     | 57                                       | 57                          | 78                          | E1                         | 37                                 |
| ADD13         | 58                         | 58                                     | 58                                       | 58                          | 79                          | F3                         | 36                                 |
| ADD12         | 60                         | 60                                     | 59                                       | 60                          | 83                          | F2                         | 32                                 |
| ADD11         | 61                         | 61                                     | 60                                       | 61                          | 85                          | F1                         | 30                                 |
| ADD10         | 62                         | 62                                     | 61                                       | 62                          | 87                          | G2                         | 28                                 |
| ADD9          | 63                         | 63                                     | 62                                       | 64                          | 89                          | G1                         | 26                                 |
| ADD8          | 64                         | 64                                     | 64                                       | 65                          | 92                          | H1                         | 22                                 |
| ADD7          | 65                         | 65                                     | 65                                       | 66                          | 94                          | H2                         | 20                                 |
| ADD6          | 66                         | 66                                     | 66                                       | 67                          | 95                          | J1                         | 18                                 |
| ADD5          | 67                         | 67                                     | 67                                       | 68                          | 97                          | J2                         | 16                                 |
| ADD4          | 69                         | 69                                     | 68                                       | 70                          | 102                         | K2                         | 11                                 |
| ADD3          | 70                         | 70                                     | 69                                       | 71                          | 103                         | K1                         | 10                                 |
| ADD2          | 71                         | 71                                     | 71                                       | 72                          | 104                         | K3                         | 8                                  |
| ADD1          | 76                         | 72                                     | 76                                       | 73                          | 105                         | M1                         | 7                                  |

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)**

| Pin Name                 | 84-Pin<br>PLCC<br>EPF8282A | 84-Pin<br>PLCC<br>EPF8452A<br>EPF8636A | 100-Pin<br>TQFP<br>EPF8282A<br>EPF8282AV | 100-Pin<br>TQFP<br>EPF8452A | 144-Pin<br>TQFP<br>EPF8820A                | 160-Pin<br>PGA<br>EPF8452A                                                                | 160-Pin<br>PQFP<br>EPF8820A<br>(1)                      |
|--------------------------|----------------------------|----------------------------------------|------------------------------------------|-----------------------------|--------------------------------------------|-------------------------------------------------------------------------------------------|---------------------------------------------------------|
| ADD0                     | 78                         | 76                                     | 78                                       | 77                          | 106                                        | N3                                                                                        | 6                                                       |
| DATA7                    | 3                          | 2                                      | 90                                       | 89                          | 131                                        | P8                                                                                        | 140                                                     |
| DATA6                    | 4                          | 4                                      | 91                                       | 91                          | 132                                        | P10                                                                                       | 139                                                     |
| DATA5                    | 6                          | 6                                      | 92                                       | 95                          | 133                                        | R12                                                                                       | 138                                                     |
| DATA4                    | 7                          | 7                                      | 95                                       | 96                          | 134                                        | R13                                                                                       | 136                                                     |
| DATA3                    | 8                          | 8                                      | 97                                       | 97                          | 135                                        | P13                                                                                       | 135                                                     |
| DATA2                    | 9                          | 9                                      | 99                                       | 98                          | 137                                        | R14                                                                                       | 133                                                     |
| DATA1                    | 13                         | 13                                     | 4                                        | 4                           | 138                                        | N15                                                                                       | 132                                                     |
| DATA0                    | 14                         | 14                                     | 5                                        | 5                           | 140                                        | K13                                                                                       | 129                                                     |
| SDOUT (3)                | 79                         | 78                                     | 79                                       | 79                          | 23                                         | P4                                                                                        | 97                                                      |
| TDI (4)                  | 55                         | 45 (5)                                 | 54                                       | —                           | 96                                         | —                                                                                         | 17                                                      |
| TD0 (4)                  | 27                         | 27 (5)                                 | 18                                       | —                           | 18                                         | —                                                                                         | 102                                                     |
| TCK (4), (6)             | 72                         | 44 (5)                                 | 72                                       | —                           | 88                                         | —                                                                                         | 27                                                      |
| TMS (4)                  | 20                         | 43 (5)                                 | 11                                       | —                           | 86                                         | —                                                                                         | 29                                                      |
| TRST (7)                 | 52                         | 52 (8)                                 | 50                                       | —                           | 71                                         | —                                                                                         | 45                                                      |
| Dedicated<br>Inputs (10) | 12, 31, 54,<br>73          | 12, 31, 54,<br>73                      | 3, 23, 53, 73                            | 3, 24, 53,<br>74            | 9, 26, 82,<br>99                           | C3, D14,<br>N2, R15                                                                       | 14, 33, 94,<br>113                                      |
| VCCINT                   | 17, 38, 59,<br>80          | 17, 38, 59,<br>80                      | 6, 20, 37, 56,<br>70, 87                 | 9, 32, 49,<br>59, 82        | 8, 28, 70,<br>90, 111                      | B2, C4, D3,<br>D8, D12,<br>G3, G12,<br>H4, H13,<br>J3, J12,<br>M4, M7,<br>M9, M13,<br>N12 | 3, 24, 46,<br>92, 114,<br>160                           |
| VCCIO                    | —                          | —                                      | —                                        | —                           | 16, 40, 60,<br>69, 91,<br>112, 122,<br>141 | —                                                                                         | 23, 47, 57,<br>69, 79,<br>104, 127,<br>137, 149,<br>159 |

**Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)**

| Pin Name                  | 225-Pin<br>BGA<br>EPF8820A                                                                                    | 232-Pin<br>PGA<br>EPF81188A                                      | 240-Pin<br>PQFP<br>EPF81188A                                   | 240-Pin<br>PQFP<br>EPF81500A                                        | 280-Pin<br>PGA<br>EPF81500A                                             | 304-Pin<br>RQFP<br>EPF81500A                                         |
|---------------------------|---------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|----------------------------------------------------------------|---------------------------------------------------------------------|-------------------------------------------------------------------------|----------------------------------------------------------------------|
| DATA4                     | A5                                                                                                            | C7                                                               | 198                                                            | 194                                                                 | W16                                                                     | 248                                                                  |
| DATA3                     | B5                                                                                                            | D7                                                               | 196                                                            | 193                                                                 | W17                                                                     | 246                                                                  |
| DATA2                     | E6                                                                                                            | B5                                                               | 194                                                            | 190                                                                 | V16                                                                     | 243                                                                  |
| DATA1                     | D5                                                                                                            | A3                                                               | 191                                                            | 189                                                                 | U16                                                                     | 241                                                                  |
| DATA0                     | C4                                                                                                            | A2                                                               | 189                                                            | 187                                                                 | V17                                                                     | 239                                                                  |
| SDOUT (3)                 | K1                                                                                                            | N2                                                               | 135                                                            | 136                                                                 | F19                                                                     | 169                                                                  |
| TDI                       | F15 (4)                                                                                                       | –                                                                | –                                                              | 63 (14)                                                             | B1 (14)                                                                 | 80 (14)                                                              |
| TDO                       | J2 (4)                                                                                                        | –                                                                | –                                                              | 117                                                                 | C17                                                                     | 149                                                                  |
| TCK (6)                   | J14 (4)                                                                                                       | –                                                                | –                                                              | 116 (14)                                                            | A19 (14)                                                                | 148 (14)                                                             |
| TMS                       | J12 (4)                                                                                                       | –                                                                | –                                                              | 64 (14)                                                             | C2 (14)                                                                 | 81 (14)                                                              |
| TRST (7)                  | P14                                                                                                           | –                                                                | –                                                              | 115 (14)                                                            | A18 (14)                                                                | 145 (14)                                                             |
| Dedicated Inputs<br>(10)  | F4, L1, K12,<br>E15                                                                                           | C1, C17, R1,<br>R17                                              | 10, 51, 130,<br>171                                            | 8, 49, 131,<br>172                                                  | F1, F16, P3,<br>P19                                                     | 12, 64, 164,<br>217                                                  |
| VCCINT<br>(5.0 V)         | F5, F10, E1,<br>L2, K4, M12,<br>P15, H13,<br>H14, B15,<br>C13                                                 | E4, H4, L4,<br>P12, L14,<br>H14, E14,<br>R14, U1                 | 20, 42, 64, 66,<br>114, 128, 150,<br>172, 236                  | 18, 40, 60, 62,<br>91, 114, 129,<br>151, 173, 209,<br>236           | B17, D3, D15,<br>E8, E10, E12,<br>E14, R7, R9,<br>R11, R13,<br>R14, T14 | 24, 54, 77,<br>144, 79, 115,<br>162, 191, 218,<br>266, 301           |
| VCCIO<br>(5.0 V or 3.3 V) | H3, H2, P6,<br>R6, P10, N10,<br>R14, N13,<br>H15, H12,<br>D12, A14,<br>B10, A10, B6,<br>C6, A2, C3,<br>M4, R2 | N10, M13,<br>M5, K13, K5,<br>H13, H5, F5,<br>E10, E8, N8,<br>F13 | 19, 41, 65, 81,<br>99, 116, 140,<br>162, 186, 202,<br>220, 235 | 17, 39, 61, 78,<br>94, 108, 130,<br>152, 174, 191,<br>205, 221, 235 | D14, E7, E9,<br>E11, E13, R6,<br>R8, R10, R12,<br>T13, T15              | 22, 53, 78, 99,<br>119, 137, 163,<br>193, 220, 244,<br>262, 282, 300 |