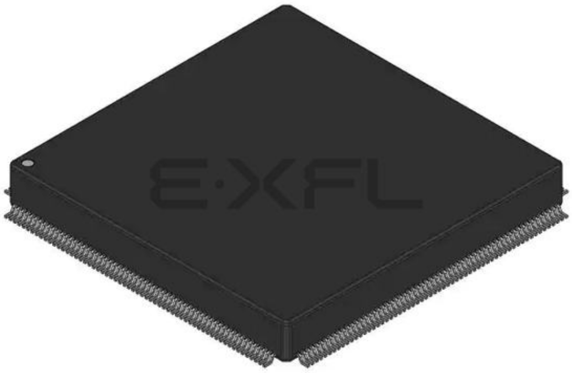


| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 126 |
| Number of Logic Elements/Cells | 1008 |
| Total RAM Bits | - |
| Number of I/O | 184 |
| Number of Gates | 12000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 240-BFQFP |
| Supplier Device Package | 240-RQFP (32x32) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf81188arc240-4 |

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide-data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 3 shows FLEX 8000 performance and LE requirements for typical applications.

*Table 3. FLEX 8000 Performance*

| Application | LEs Used | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | A-2 | A-3 | A-4 | |
| 16-bit loadable counter | 16 | 125 | 95 | 83 | MHz |
| 16-bit up/down counter | 16 | 125 | 95 | 83 | MHz |
| 24-bit accumulator | 24 | 87 | 67 | 58 | MHz |
| 16-bit address decode | 4 | 4.2 | 4.9 | 6.3 | ns |
| 16-to-1 multiplexer | 10 | 6.6 | 7.9 | 9.5 | ns |

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial configuration devices, or with data provided by a system controller. Altera offers the EPC1, EPC1213, EPC1064, and EPC1441 configuration devices, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32 K × 8 bit or larger configuration device, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation. For information on how to configure FLEX 8000 devices, go to the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 8000 architecture.

For more information on the MAX+PLUS II software, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

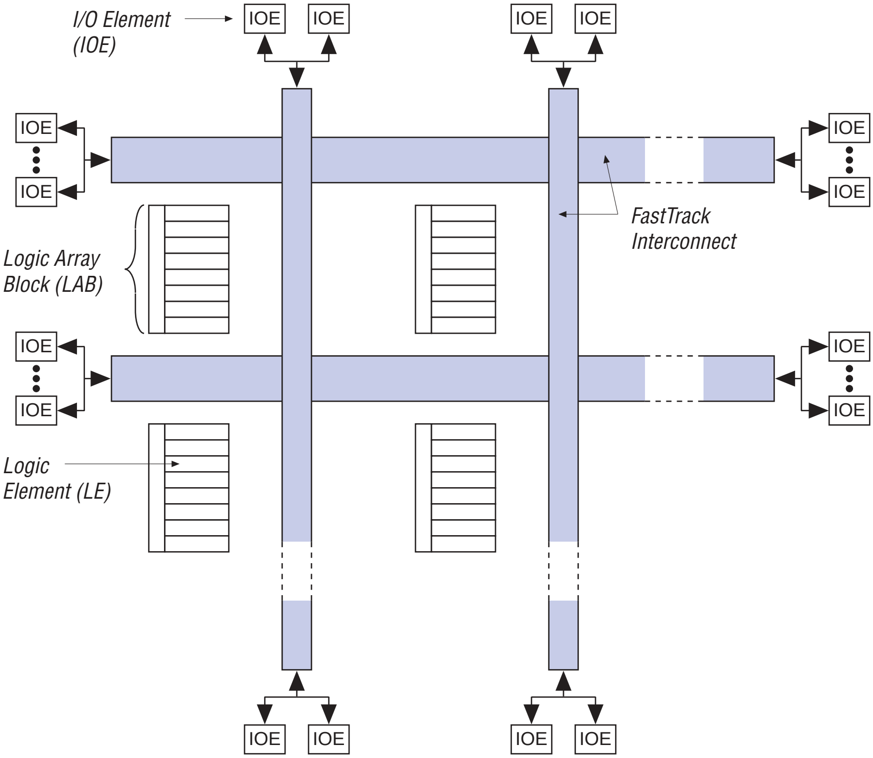
## Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

***Figure 1. FLEX 8000 Device Block Diagram***

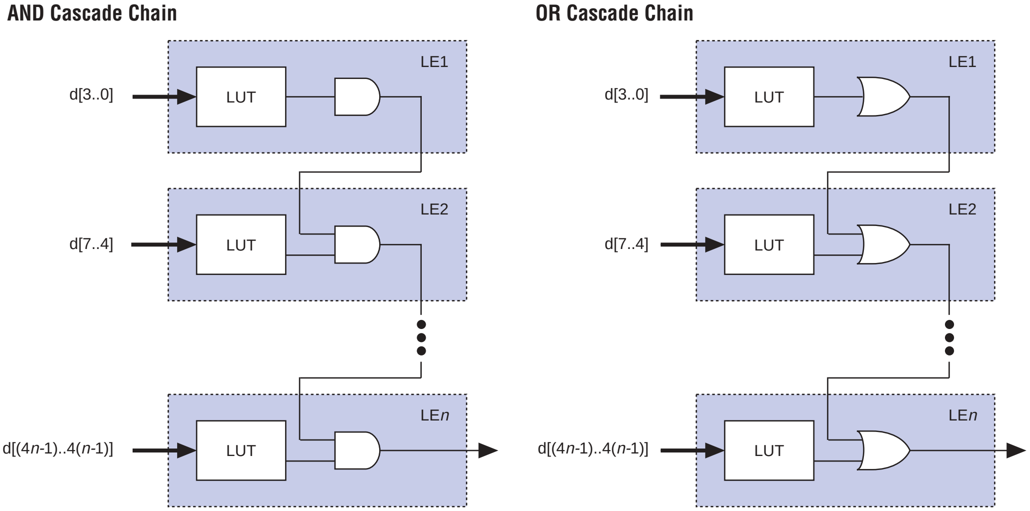


Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

*Figure 5. FLEX 8000 Cascade Chain Operation*



### LE Operating Modes

The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the `DATA3`, `LABCTRL1`, and `LABCTRL2` inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that `LABCTRL1` implements an asynchronous load. The data to be loaded is driven to `DATA3`; when `LABCTRL1` is asserted, `DATA3` is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

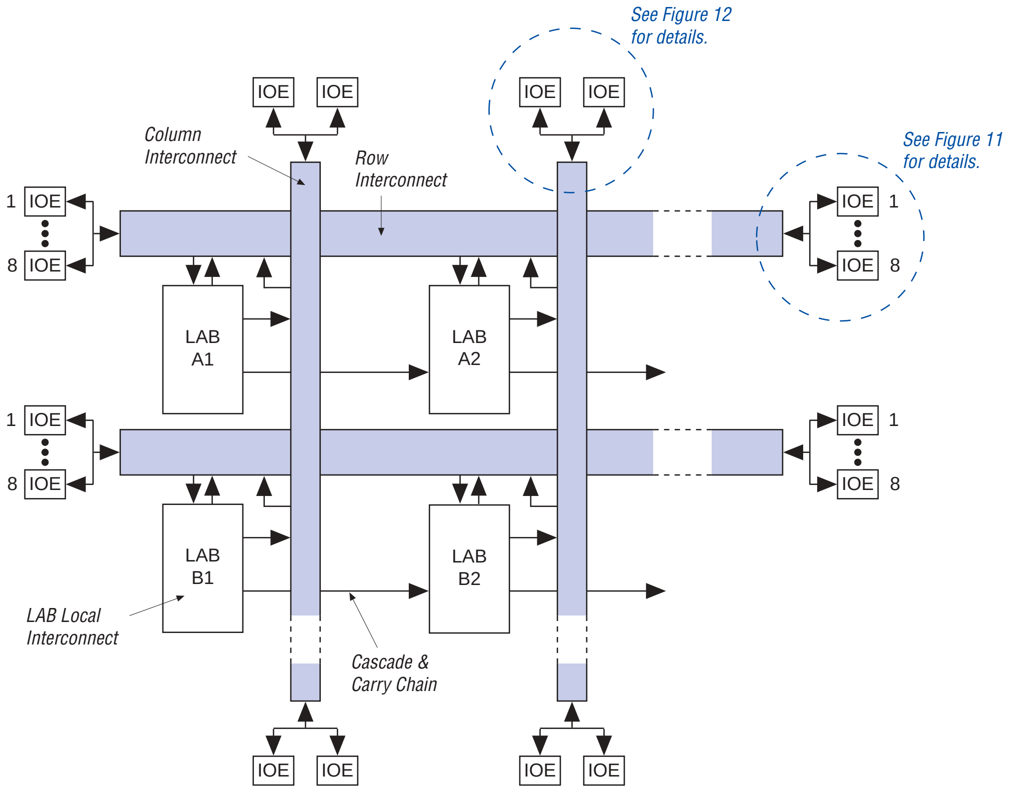
*Table 4. FLEX 8000 FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF8282A<br>EPF8282AV | 2 | 168 | 13 | 16 |
| EPF8452A | 2 | 168 | 21 | 16 |
| EPF8636A | 3 | 168 | 21 | 16 |
| EPF8820A | 4 | 168 | 21 | 16 |
| EPF81188A | 6 | 168 | 21 | 16 |
| EPF81500A | 6 | 216 | 27 | 16 |

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

*Figure 9. FLEX 8000 Device Interconnect Resources*

*Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.*

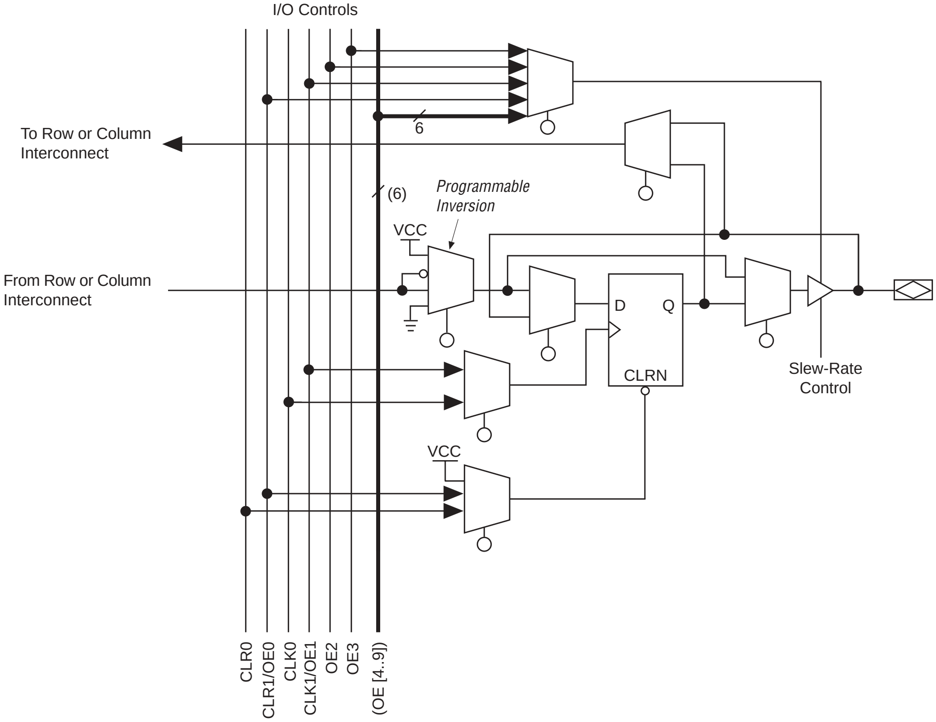


## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 10 shows the IOE block diagram.

**Figure 10. FLEX 8000 IOE**

*Numbers in parentheses are for EPF81500A devices only.*

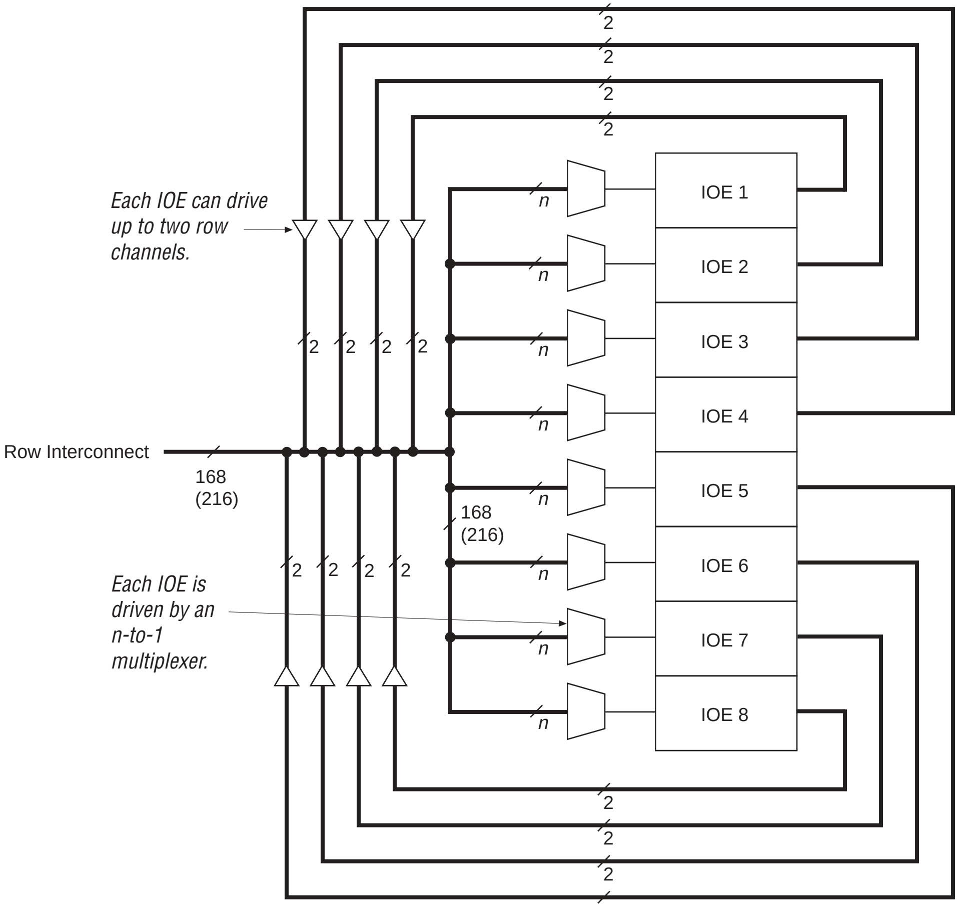


## *Row-to-IOE Connections*

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

*Figure 11. FLEX 8000 Row-to-IOE Connections*

*Numbers in parentheses are for EPF81500A devices. See Note (1).*



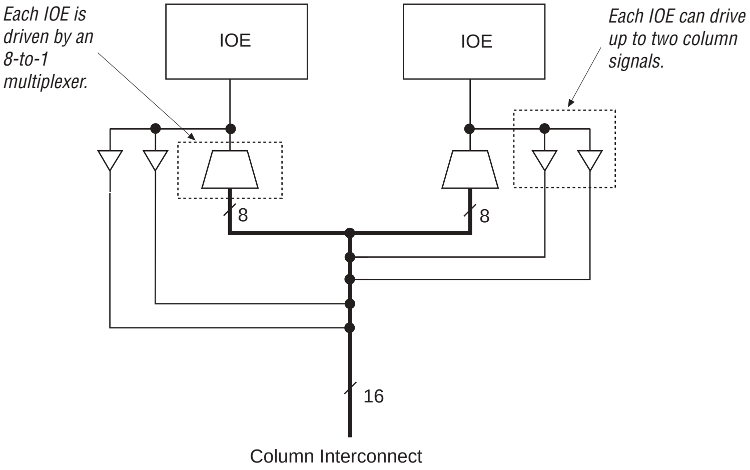
**Note:**

(1) $n$ = 13 for EPF8282A and EPF8282AV devices.
$n$ = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
$n$ = 27 for EPF81500A devices.

## *Column-to-IOE Connections*

Two IOEs are located at the top and bottom of the column channels (see Figure 12). When an IOE is used as an input, it can drive up to two separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

*Figure 12. FLEX 8000 Column-to-IOE Connections*



In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. Figure 13 on page 22 shows how two output enable signals are shared with one clock and one clear signal.

## MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCINT` pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The `VCCIO` pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$. See Table 8 on page 26.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

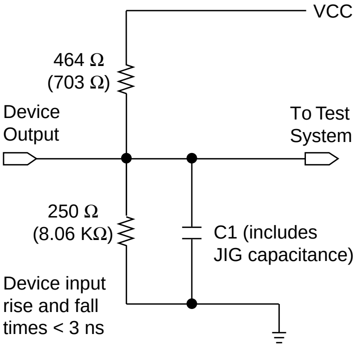
The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in Table 6.

*Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. |

*Figure 15. FLEX 8000 AC Test Conditions*

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices or outputs. Numbers without parentheses are for 5.0-V devices or outputs.*



## Operating Conditions

Tables 9 through 12 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V FLEX 8000 devices.

*Table 9. FLEX 8000 5.0-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage |  | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin |  | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias |  | 150 | ° C |
|  |  | PQFP and RQFP, under bias |  | 135 | ° C |

*Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)*

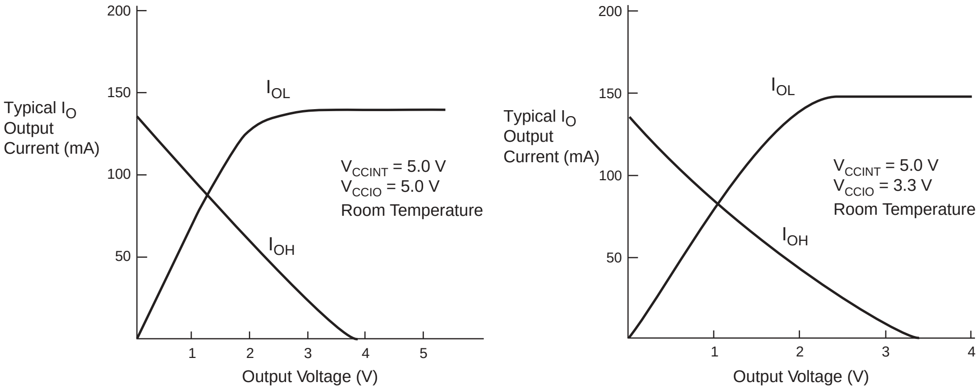


Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

*Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V $V_{CCIO}$*

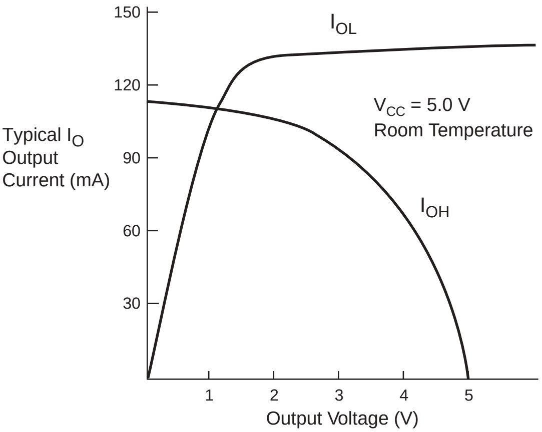
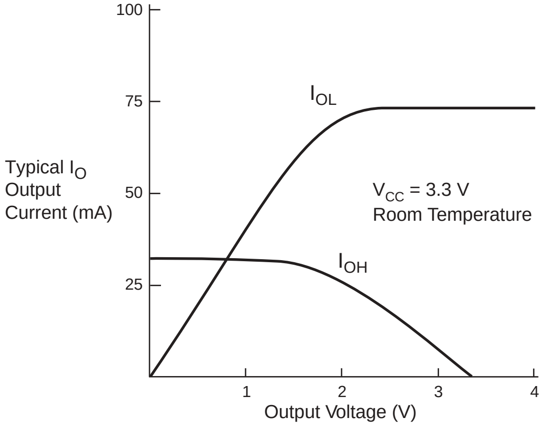


Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

*Figure 18. Output Drive Characteristics of EPF8282AV Devices*



## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

| Table 21. FLEX 8000 Timing Model Interconnect Paths | | |
|---|---|---|
| **Source** | **Destination** | **Total Delay** |
| LE-Out | LE in same LAB | $t_{LOCAL}$ |
| LE-Out | LE in same row, different LAB | $t_{ROW} + t_{LOCAL}$ |
| LE-Out | LE in different row | $t_{COL} + t_{ROW} + t_{LOCAL}$ |
| LE-Out | IOE on column | $t_{COL}$ |
| LE-Out | IOE on row | $t_{ROW}$ |
| IOE on row | LE in same row | $t_{ROW} + t_{LOCAL}$ |
| IOE on column | Any LE | $t_{COL} + t_{ROW} + t_{LOCAL}$ |

Tables 22 through 49 show the FLEX 8000 internal and external timing parameters.

| Table 22. EPF8282A Internal I/O Element Timing Parameters | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **A-2** | | **A-3** | | **A-4** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | – | | – | | – | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | – | | – | | – | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 26. EPF8282AV I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.9 | | 2.2 | ns |
| $t_{IOC}$ | | 1.9 | | 2.0 | ns |
| $t_{IOE}$ | | 1.9 | | 2.0 | ns |
| $t_{IOCO}$ | | 1.0 | | 2.0 | ns |
| $t_{IOCOMB}$ | | 0.1 | | 0.0 | ns |
| $t_{IOSU}$ | 1.8 | | 2.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.2 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 2.3 | ns |
| $t_{IN}$ | | 1.7 | | 3.4 | ns |
| $t_{OD1}$ | | 1.7 | | 4.1 | ns |
| $t_{OD2}$ | | – | | – | ns |
| $t_{OD3}$ | | 5.2 | | 7.1 | ns |
| $t_{XZ}$ | | 1.8 | | 4.3 | ns |
| $t_{ZX1}$ | | 1.8 | | 4.3 | ns |
| $t_{ZX2}$ | | – | | – | ns |
| $t_{ZX3}$ | | 5.3 | | 8.3 | ns |

*Table 27. EPF8282AV Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.4 | | 1.3 | ns |
| $t_{LABCARRY}$ | | 0.4 | | 0.8 | ns |
| $t_{LOCAL}$ | | 0.8 | | 1.5 | ns |
| $t_{ROW}$ | | 4.2 | | 6.3 | ns |
| $t_{COL}$ | | 2.5 | | 3.8 | ns |
| $t_{DIN\_C}$ | | 5.5 | | 8.0 | ns |
| $t_{DIN\_D}$ | | 7.2 | | 10.8 | ns |
| $t_{DIN\_IO}$ | | 5.5 | | 9.0 | ns |

*Table 28. EPF8282AV Logic Element Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{LUT}$ | | 3.2 | | 7.3 | ns |
| $t_{CLUT}$ | | 0.0 | | 1.4 | ns |
| $t_{RLUT}$ | | 1.5 | | 5.1 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.9 | | 2.8 | ns |
| $t_{CICO}$ | | 0.6 | | 1.5 | ns |
| $t_{CGEN}$ | | 0.7 | | 2.2 | ns |
| $t_{CGENR}$ | | 1.5 | | 3.7 | ns |
| $t_{C}$ | | 2.5 | | 4.7 | ns |
| $t_{CH}$ | 4.0 | | 6.0 | | ns |
| $t_{CL}$ | 4.0 | | 6.0 | | ns |
| $t_{CO}$ | | 0.6 | | 0.9 | ns |
| $t_{COMB}$ | | 0.6 | | 0.9 | ns |
| $t_{SU}$ | 1.2 | | 2.4 | | ns |
| $t_{H}$ | 1.5 | | 4.6 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.3 | ns |
| $t_{CLR}$ | | 0.8 | | 1.3 | ns |

*Table 29. EPF8282AV External Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{DRR}$ | | 24.8 | | 50.1 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | ns |

### *Table 30. EPF8452A I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | – | | – | | – | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | – | | – | | – | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

### *Table 31. EPF8452A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{ROW}$ | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 48. EPF81500A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 49. EPF81500A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{DRR}}$ | | 16.1 | | 20.1 | | 25.1 | ns |
| $\mathbf{t_{ODH}}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 225-Pin BGA EPF8820A | 232-Pin PGA EPF81188A | 240-Pin PQFP EPF81188A | 240-Pin PQFP EPF81500A | 280-Pin PGA EPF81500A | 304-Pin RQFP EPF81500A |
|---|---|---|---|---|---|---|
| `DATA4` | A5 | C7 | 198 | 194 | W16 | 248 |
| `DATA3` | B5 | D7 | 196 | 193 | W17 | 246 |
| `DATA2` | E6 | B5 | 194 | 190 | V16 | 243 |
| `DATA1` | D5 | A3 | 191 | 189 | U16 | 241 |
| `DATA0` | C4 | A2 | 189 | 187 | V17 | 239 |
| `SDOUT` *(3)* | K1 | N2 | 135 | 136 | F19 | 169 |
| `TDI` | F15 *(4)* | – | – | 63 *(14)* | B1 *(14)* | 80 *(14)* |
| `TDO` | J2 *(4)* | – | – | 117 | C17 | 149 |
| `TCK` *(6)* | J14 *(4)* | – | – | 116 *(14)* | A19 *(14)* | 148 *(14)* |
| `TMS` | J12 *(4)* | – | – | 64 *(14)* | C2 *(14)* | 81 *(14)* |
| `TRST` *(7)* | P14 | – | – | 115 *(14)* | A18 *(14)* | 145 *(14)* |
| Dedicated Inputs *(10)* | F4, L1, K12, E15 | C1, C17, R1, R17 | 10, 51, 130, 171 | 8, 49, 131, 172 | F1, F16, P3, P19 | 12, 64, 164, 217 |
| `VCCINT` (5.0 V) | F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13 | E4, H4, L4, P12, L14, H14, E14, R14, U1 | 20, 42, 64, 66, 114, 128, 150, 172, 236 | 18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236 | B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14 | 24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301 |
| `VCCIO` (5.0 V or 3.3 V) | H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2 | N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13 | 19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235 | 17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235 | D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15 | 22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300 |