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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

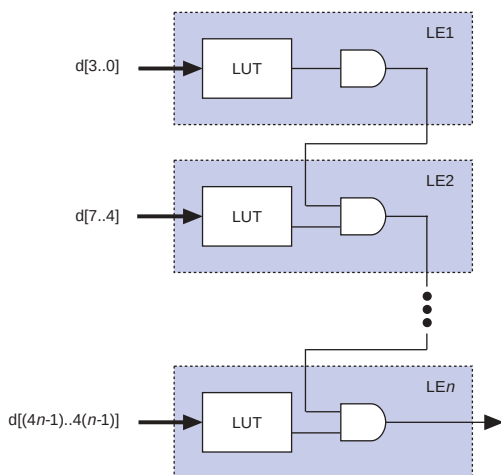
Product Status	Obsolete
Number of LABs/CLBs	126
Number of Logic Elements/Cells	1008
Total RAM Bits	-
Number of I/O	184
Number of Gates	12000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf81188arc240-4aa

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

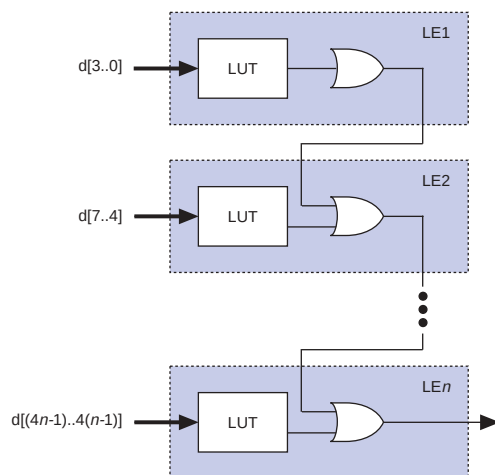
Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 5. FLEX 8000 Cascade Chain Operation

AND Cascade Chain



OR Cascade Chain

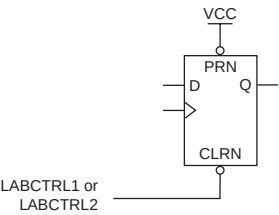


LE Operating Modes

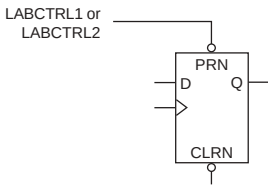
The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes

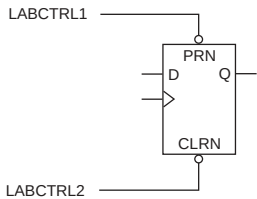
Asynchronous Clear



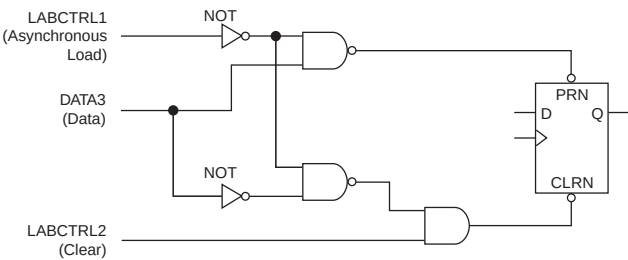
Asynchronous Preset



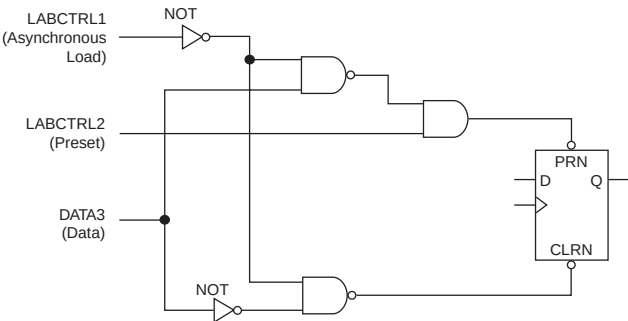
Asynchronous Clear & Preset



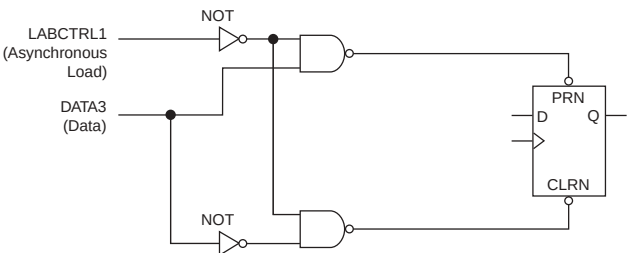
Asynchronous Load with Clear



Asynchronous Load with Preset



Asynchronous Load without Clear or Preset



Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

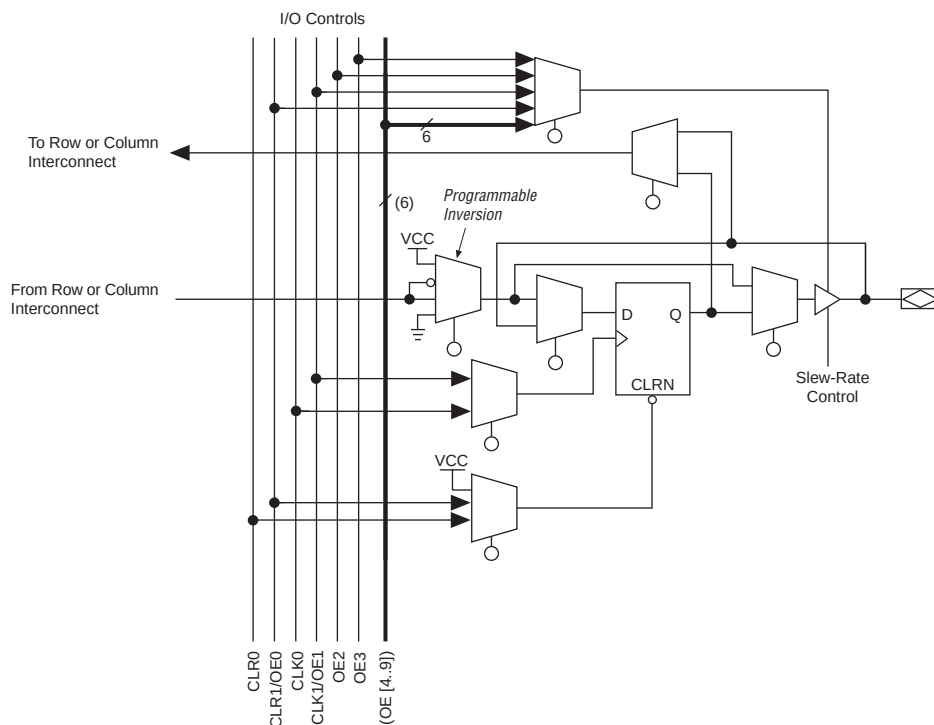
Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. [Table 4](#) summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

Table 4. FLEX 8000 FastTrack Interconnect Resources				
Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282A EPF8282AV	2	168	13	16
EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820A	4	168	21	16
EPF81188A	6	168	21	16
EPF81500A	6	216	27	16

[Figure 9](#) shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 10. FLEX 8000 IOE

Numbers in parentheses are for EPF81500A devices only.



Row-to-IOE Connections

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an n -to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

Table 10. FLEX 8000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation	(3), (4)	3.00 (3.00)	3.60 (3.60)	V
V_I	Input voltage		-0.5	$V_{CCINT} + 0.5$	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
		For industrial use	-40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 11. FLEX 8000 5.0-V Device DC Operating Conditions Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC (7) $V_{CCIO} = 4.75$ V	2.4			V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC (7) $V_{CCIO} = 3.00$ V	2.4			V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC (7) $V_{CCIO} = 3.00$ V	$V_{CCIO} - 0.2$			V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC (7) $V_{CCIO} = 4.75$ V			0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC (7) $V_{CCIO} = 3.00$ V			0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC (7) $V_{CCIO} = 3.00$ V			0.2	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	-10		10	μA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	-40		40	μA
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load		0.5	10	mA

Table 12. FLEX 8000 5.0-V Device Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		10	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) The maximum V_{CC} rise time is 100 ms.
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
- (6) These values are specified in Table 10 on page 28.
- (7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL or CMOS output current.
- (8) Capacitance is sample-tested only.

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 3.3-V FLEX 8000 devices.

Table 13. FLEX 8000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	With respect to ground (2)	-2.0	5.3	V
V _I	DC input voltage		-2.0	5.3	V
I _{OUT}	DC output current, per pin		-25	25	mA
T _{STG}	Storage temperature	No bias	-65	150	° C
T _{AMB}	Ambient temperature	Under bias	-65	135	° C
T _J	Junction temperature	Plastic packages, under bias		135	° C

Table 14. FLEX 8000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	(3)	3.0	3.6	V
V _I	Input voltage		-0.3	V _{CC} + 0.3	V
V _O	Output voltage		0	V _{CC}	V
T _A	Operating temperature	For commercial use	0	70	° C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

Table 15. FLEX 8000 3.3-V Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level output voltage	$I_{OH} = -0.1$ mA DC (5)	$V_{CC} - 0.2$			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA DC (5)			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	-10		10	μ A
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	-40		40	μ A
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load (6)		0.3	10	mA

Table 16. FLEX 8000 3.3-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) The maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
- (4) These values are specified in [Table 14 on page 29](#).
- (5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
- (6) Typical values are for $T_A = 25^\circ$ C and $V_{CC} = 3.3$ V.
- (7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

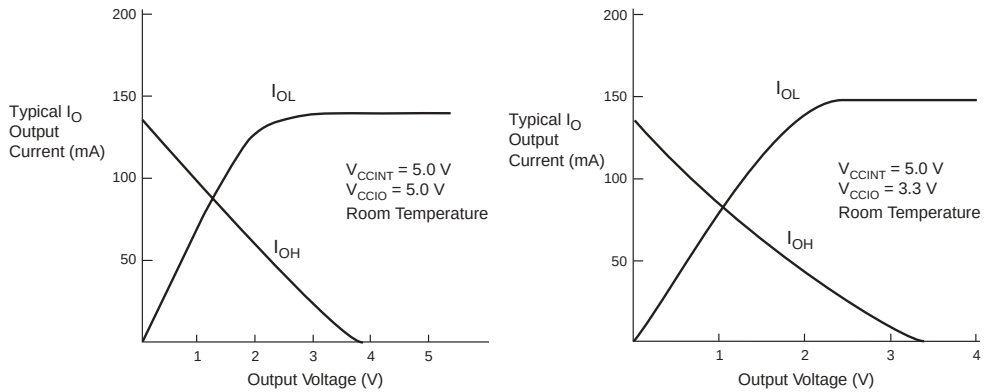
Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)

Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

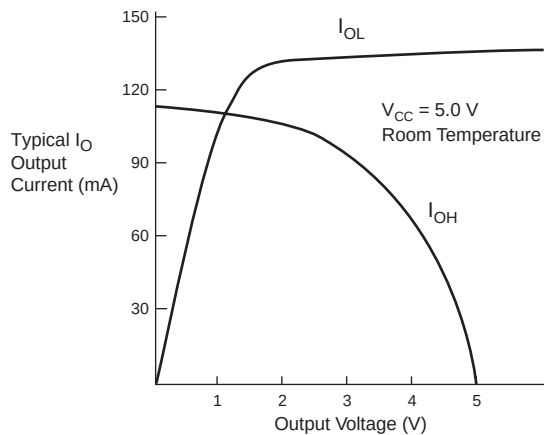
Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V V_{CCIO} 

Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

Table 24. EPF8282A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 25. EPF8282A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DDR}		15.8		19.8		24.8	ns
t _{ODH}	1.0		1.0		1.0		ns

Table 38. EPF8820A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 39. EPF8820A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 42. EPF81188A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 43. EPF81188A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 44. EPF81188A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 45. EPF81188A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DRR}		16.0		20.0		25.0	ns
t _{ODH}	1.0		1.0		1.0		ns

Table 46. EPF81500A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 47. EPF81500A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Power Consumption

The supply power (P) for FLEX 8000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = [(I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC}] + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in Table 11 on page 28 and Table 15 on page 30. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#). The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{\text{MHz} \times \text{LE}}$$

The parameters in this equation are shown below:

- f_{MAX} = Maximum operating frequency in MHz
- N = Total number of logic cells used in the device
- tog_{LC} = Average percentage of logic cells toggling at each clock
- K = Constant, shown in [Table 50](#)

Table 50. Values for Constant K

Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

[Figure 20](#) shows the relationship between I_{CC} and operating frequency for several LE utilization values.

Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
nSP (2)	75	75	75	76	110	R1	1
MSEL0 (2)	74	74	74	75	109	P2	2
MSEL1 (2)	53	53	51	51	72	A1	44
nSTATUS (2)	32	32	24	25	37	C13	82
nCONFIG (2)	33	33	25	26	38	A15	81
DCLK (2)	10	10	100	100	143	P14	125
CONF_DONE (2)	11	11	1	1	144	N13	124
nWS	30	30	22	23	33	F13	87
nRS	48	48	42	45	31	C6	89
RDCLK	49	49	45	46	12	B5	110
nCS	29	29	21	22	4	D15	118
CS	28	28	19	21	3	E15	121
RDYnBUSY	77	77	77	78	20	P3	100
CLKUSR	50	50	47	47	13	C5	107
ADD17	51	51	49	48	75	B4	40
ADD16	36	55	28	54	76	E2	39
ADD15	56	56	55	55	77	D1	38
ADD14	57	57	57	57	78	E1	37
ADD13	58	58	58	58	79	F3	36
ADD12	60	60	59	60	83	F2	32
ADD11	61	61	60	61	85	F1	30
ADD10	62	62	61	62	87	G2	28
ADD9	63	63	62	64	89	G1	26
ADD8	64	64	64	65	92	H1	22
ADD7	65	65	65	66	94	H2	20
ADD6	66	66	66	67	95	J1	18
ADD5	67	67	67	68	97	J2	16
ADD4	69	69	68	70	102	K2	11
ADD3	70	70	69	71	103	K1	10
ADD2	71	71	71	72	104	K3	8
ADD1	76	72	76	73	105	M1	7

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
ADD0	78	76	78	77	106	N3	6
DATA7	3	2	90	89	131	P8	140
DATA6	4	4	91	91	132	P10	139
DATA5	6	6	92	95	133	R12	138
DATA4	7	7	95	96	134	R13	136
DATA3	8	8	97	97	135	P13	135
DATA2	9	9	99	98	137	R14	133
DATA1	13	13	4	4	138	N15	132
DATA0	14	14	5	5	140	K13	129
SDOUT (3)	79	78	79	79	23	P4	97
TDI (4)	55	45 (5)	54	—	96	—	17
TD0 (4)	27	27 (5)	18	—	18	—	102
TCK (4), (6)	72	44 (5)	72	—	88	—	27
TMS (4)	20	43 (5)	11	—	86	—	29
TRST (7)	52	52 (8)	50	—	71	—	45
Dedicated Inputs (10)	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
VCCIO	—	—	—	—	16, 40, 60, 69, 91, 112, 122, 141	—	23, 47, 57, 69, 79, 104, 127, 137, 149, 159

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	19, 44, 69, 94	7, 17, 27, 39, 54, 80, 81, 100, 101, 128, 142	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155
No Connect (N.C.)	—	—	—	2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99	—	—	—
Total User I/O Pins (9)	64	64	74	64	108	116	116

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A (1)	208-Pin PQFP EPF8820A (1)	208-Pin PQFP EPF81188A (1)
nSP (2)	120	1	R15	207	207	5
MSEL0 (2)	117	3	T15	4	4	21
MSEL1 (2)	84	38	T3	49	49	33
nSTATUS (2)	37	83	B3	108	108	124
nCONFIG (2)	40	81	C3	103	103	107
DCLK (2)	1	120	C15	158	158	154
CONF_DONE (2)	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A (1)	208-Pin PQFP EPF8820A (1)	208-Pin PQFP EPF81188A (1)
DATA4	154	127	E17	165	172	170
DATA3	157	124	G15	162	171	168
DATA2	159	122	F15	160	167	166
DATA1	11	115	E16	149	165	163
DATA0	12	113	C16	147	162	161
SDOUT (3)	128	152	C7 (11)	198	124	119
TDI (4)	—	55	R11	72	20	—
TD0 (4)	—	95	B9	120	129	—
TCK (4), (6)	—	57	U8	74	30	—
TMS (4)	—	59	U7	76	32	—
TRST (7)	—	40	R3	54	54	—
Dedicated Inputs (10)	5, 36, 85, 116	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146
VCCINT (5.0 V)	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147
VCCIO (5.0 V or 3.3 V)	—	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192
GND	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201
No Connect (N.C.)	2, 3, 38, 39, 70, 82, 83, 118, 119, 148	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4 (12)	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208
Total User I/O Pins (9)	116	114	132, 148 (13)	132	148	144

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
GND	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
No Connect (N.C.)	—	—	61, 62, 119, 120, 181, 182, 239, 240	—	—	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins (9)	148	180	180	177	204	204