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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

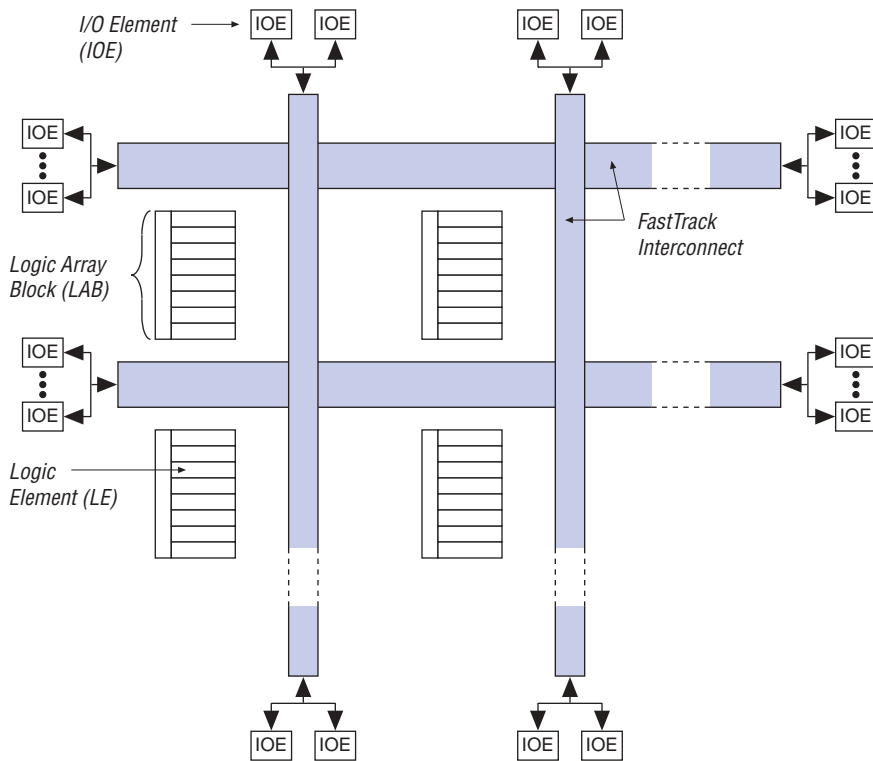
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	126
Number of Logic Elements/Cells	1008
Total RAM Bits	-
Number of I/O	184
Number of Gates	12000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-RQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf81188ari240-4

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram



Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block

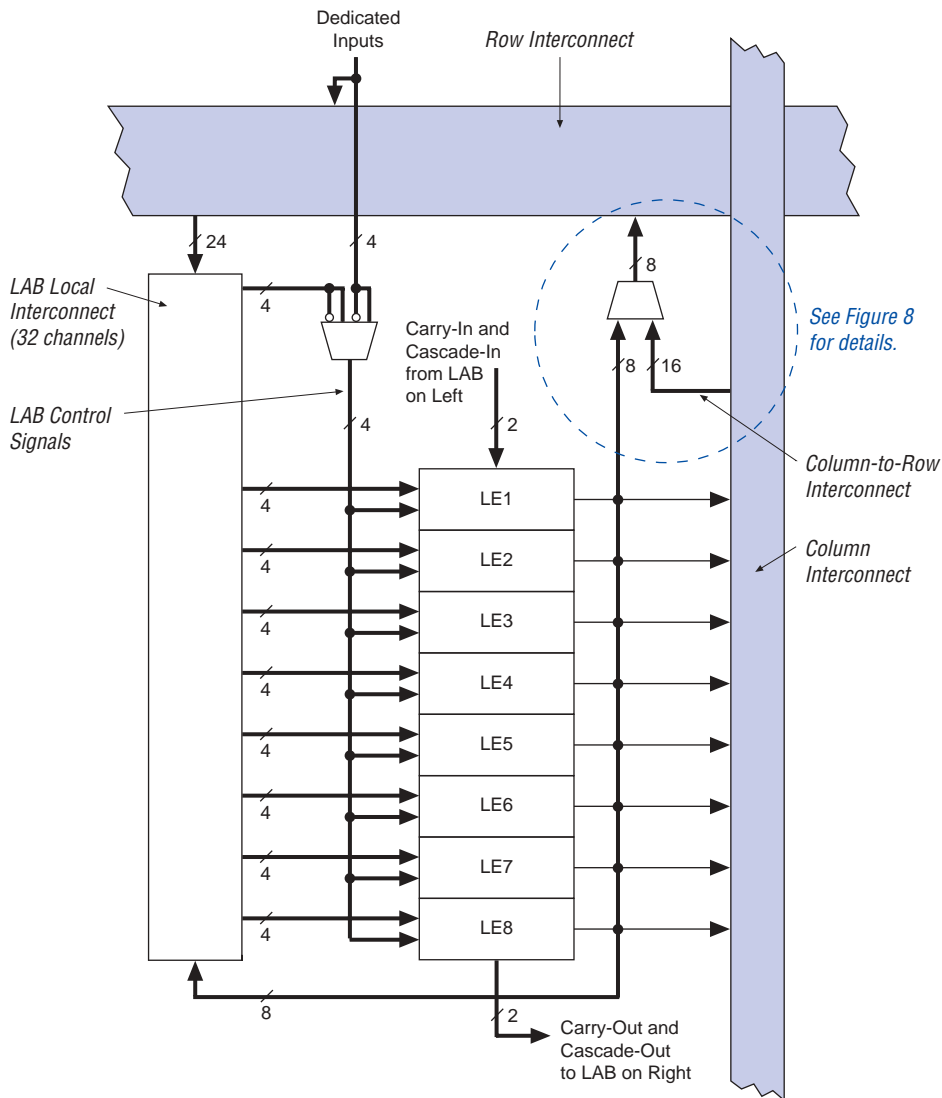
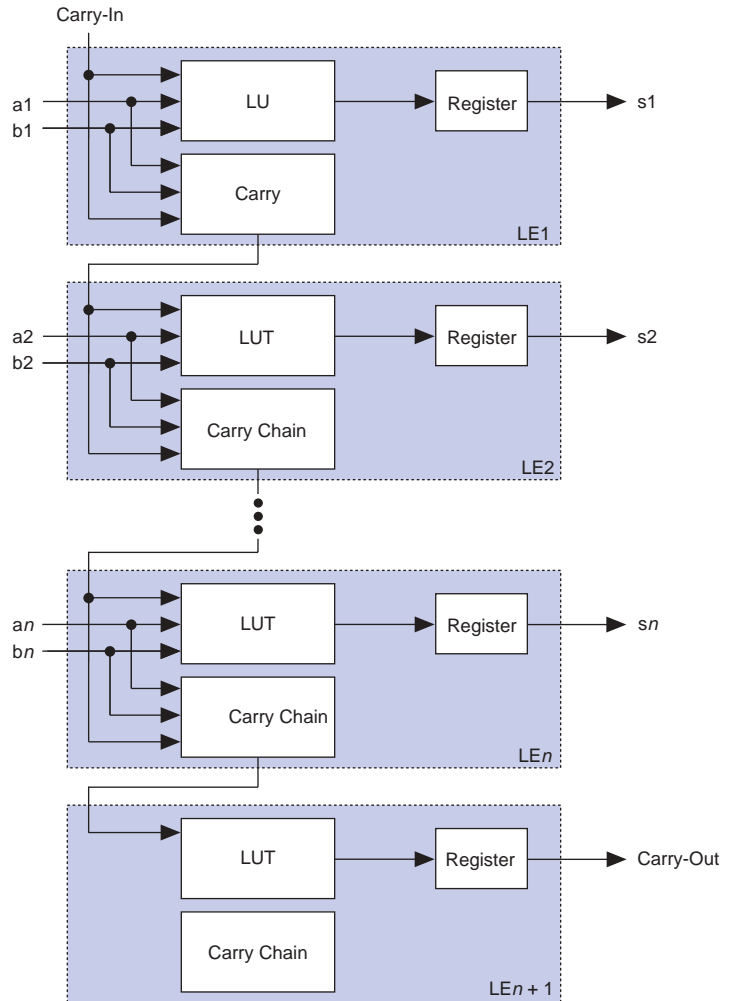


Figure 4. FLEX 8000 Carry Chain Operation

Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.6 ns per LE.

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

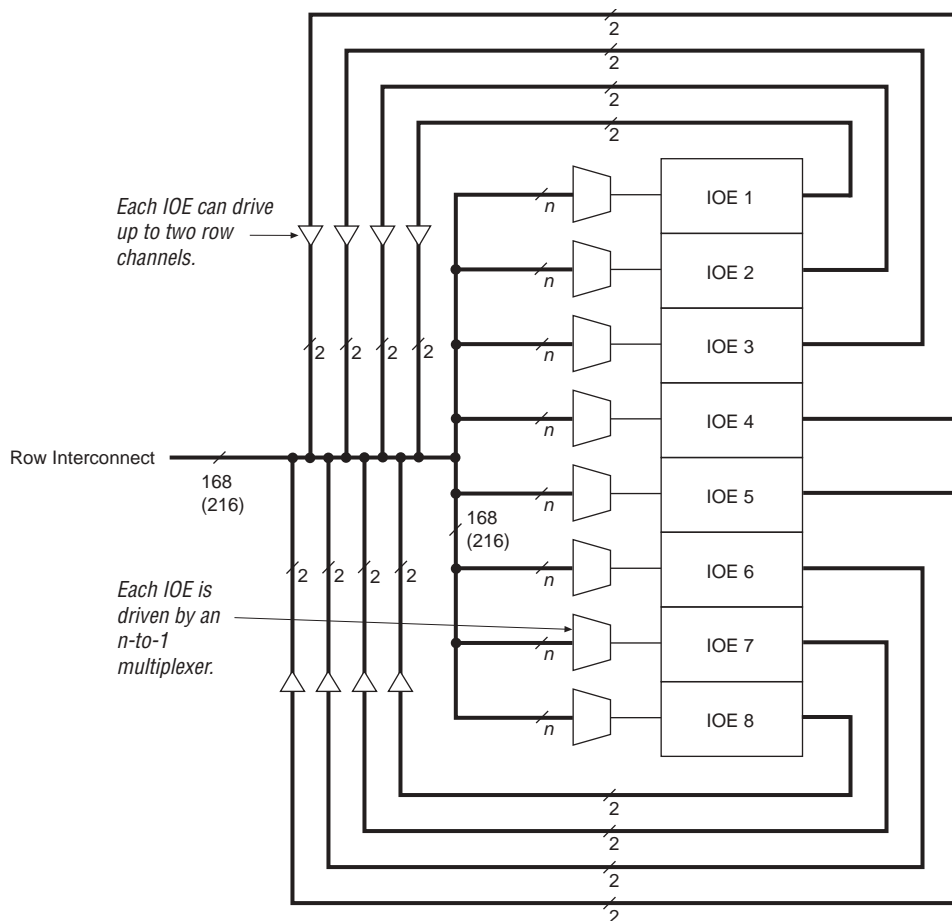
Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. [Table 4](#) summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

Table 4. FLEX 8000 FastTrack Interconnect Resources				
Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282A EPF8282AV	2	168	13	16
EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820A	4	168	21	16
EPF81188A	6	168	21	16
EPF81500A	6	216	27	16

[Figure 9](#) shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 11. FLEX 8000 Row-to-IOE Connections

Numbers in parentheses are for EPF81500A devices. See [Note \(1\)](#).



Note:

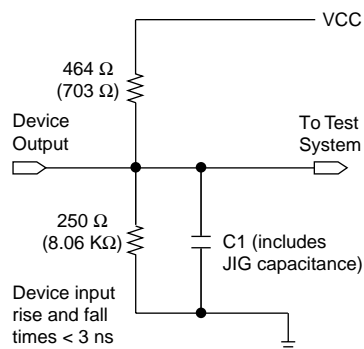
- (1) $n = 13$ for EPF8282A and EPF8282AV devices.
- $n = 21$ for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
- $n = 27$ for EPF81500A devices.

Column-to-IOE Connections

Two IOEs are located at the top and bottom of the column channels (see [Figure 12](#)). When an IOE is used as an input, it can drive up to two separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

Figure 15. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices or outputs. Numbers without parentheses are for 5.0-V devices or outputs.



Operating Conditions

Tables 9 through 12 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V FLEX 8000 devices.

Table 9. FLEX 8000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	-2.0	7.0	V
V_I	DC input voltage		-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	° C
T_{AMB}	Ambient temperature	Under bias	-65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP, under bias		135	° C

Table 12. FLEX 8000 5.0-V Device Capacitance *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C _{IN}	Input capacitance	V _{IN} = 0 V, f = 1.0 MHz		10	pF
C _{OUT}	Output capacitance	V _{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) The maximum V_{CC} rise time is 100 ms.
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
- (6) These values are specified in Table 10 on page 28.
- (7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL or CMOS output current.
- (8) Capacitance is sample-tested only.

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 3.3-V FLEX 8000 devices.

Table 13. FLEX 8000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	With respect to ground (2)	-2.0	5.3	V
V _I	DC input voltage		-2.0	5.3	V
I _{OUT}	DC output current, per pin		-25	25	mA
T _{STG}	Storage temperature	No bias	-65	150	° C
T _{AMB}	Ambient temperature	Under bias	-65	135	° C
T _J	Junction temperature	Plastic packages, under bias		135	° C

Table 14. FLEX 8000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply voltage	(3)	3.0	3.6	V
V _I	Input voltage		-0.3	V _{CC} + 0.3	V
V _O	Output voltage		0	V _{CC}	V
T _A	Operating temperature	For commercial use	0	70	° C
t _R	Input rise time			40	ns
t _F	Input fall time			40	ns

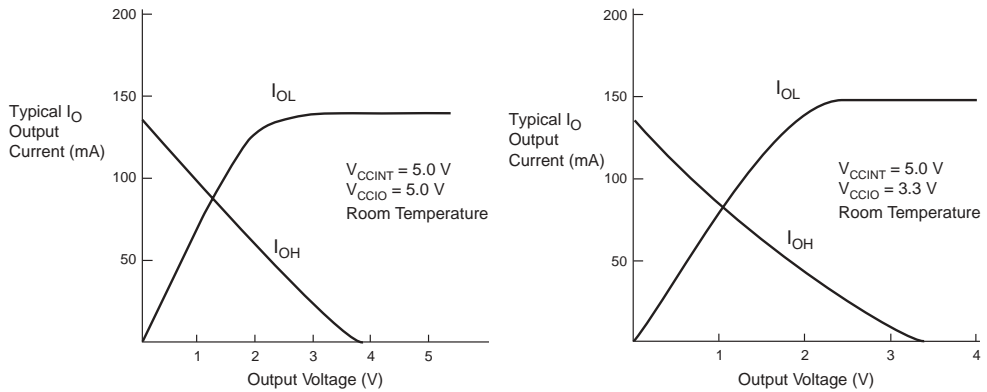
Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)

Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

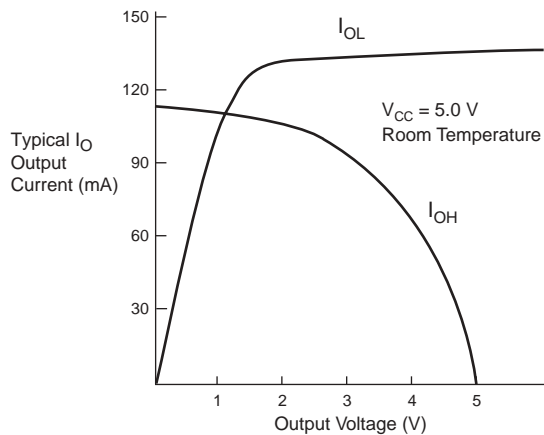
Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V V_{CCIO} 

Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

Table 17. FLEX 8000 Internal Timing Parameters *Note (1)*

Symbol	Parameter
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock; IOE register recovery time after asynchronous clear
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 5.0\text{ V}$, $C1 = 35\text{ pF}$ (2)
t_{OD2}	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$, $C1 = 35\text{ pF}$ (2)
t_{OD3}	Output buffer and pad delay, slow slew rate = on, $C1 = 35\text{ pF}$ (3)
t_{XZ}	Output buffer disable delay, $C1 = 5\text{ pF}$
t_{ZX1}	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = 5.0\text{ V}$, $C1 = 35\text{ pF}$ (2)
t_{ZX2}	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$, $C1 = 35\text{ pF}$ (2)
t_{ZX3}	Output buffer enable delay, slow slew rate = on, $C1 = 35\text{ pF}$ (3)

Table 18. FLEX 8000 LE Timing Parameters *Note (1)*

Symbol	Parameter
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_C	LE register control signal delay
t_{CH}	LE register clock high time
t_{CL}	LE register clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load
t_H	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 23. EPF8282A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.2		7.2		7.2	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 24. EPF8282A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 25. EPF8282A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DRR}		15.8		19.8		24.8	ns
t _{ODH}	1.0		1.0		1.0		ns

Table 26. EPF8282AV I/O Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{IOD}		0.9		2.2	ns
t_{IOC}		1.9		2.0	ns
t_{IOE}		1.9		2.0	ns
t_{IOCO}		1.0		2.0	ns
t_{IOCOMB}		0.1		0.0	ns
t_{IOSU}	1.8		2.8		ns
t_{IOH}	0.0		0.2		ns
t_{IOCLR}		1.2		2.3	ns
t_{IN}		1.7		3.4	ns
t_{OD1}		1.7		4.1	ns
t_{OD2}		—		—	ns
t_{OD3}		5.2		7.1	ns
t_{XZ}		1.8		4.3	ns
t_{ZX1}		1.8		4.3	ns
t_{ZX2}		—		—	ns
t_{ZX3}		5.3		8.3	ns

Table 27. EPF8282AV Interconnect Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
$t_{LABCASC}$		0.4		1.3	ns
$t_{LABCARRY}$		0.4		0.8	ns
t_{LOCAL}		0.8		1.5	ns
t_{ROW}		4.2		6.3	ns
t_{COL}		2.5		3.8	ns
t_{DIN_C}		5.5		8.0	ns
t_{DIN_D}		7.2		10.8	ns
t_{DIN_IO}		5.5		9.0	ns

Table 32. EPF8452A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_C		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_H	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 33. EPF8452A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DDR}		16.0		20.0		25.0	ns
t _{ODH}	1.0		1.0		1.0		ns

Table 40. EPF8820A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 41. EPF8820A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DRR}		16.0		20.0		25.0	ns
t _{ODH}	1.0		1.0		1.0		ns

Table 46. EPF81500A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 47. EPF81500A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Power Consumption

The supply power (P) for FLEX 8000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = [(I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC}] + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in Table 11 on page 28 and Table 15 on page 30. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#). The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{\text{MHz} \times \text{LE}}$$

The parameters in this equation are shown below:

- f_{MAX} = Maximum operating frequency in MHz
- N = Total number of logic cells used in the device
- tog_{LC} = Average percentage of logic cells toggling at each clock
- K = Constant, shown in [Table 50](#)

Table 50. Values for Constant K

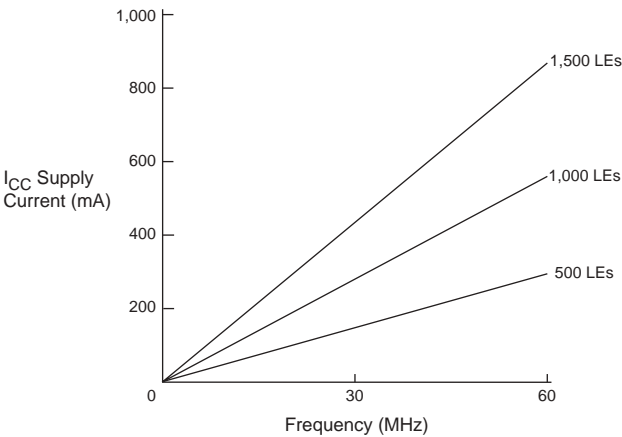
Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

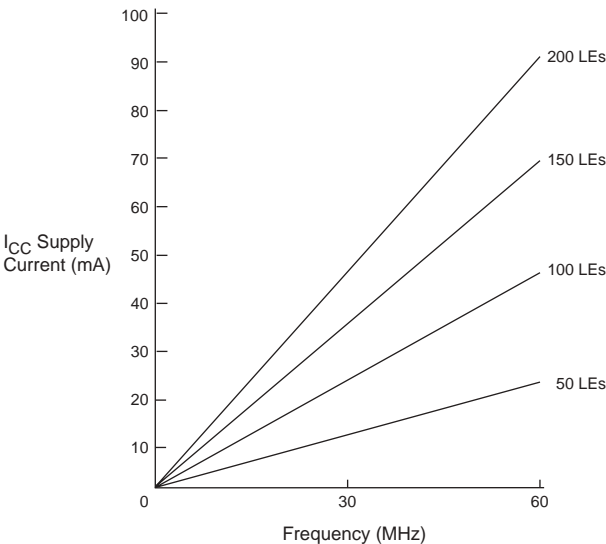
[Figure 20](#) shows the relationship between I_{CC} and operating frequency for several LE utilization values.

Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices



3.3-V FLEX 8000 Devices



Configuration & Operation



The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to [Application Note 33 \(Configuring FLEX 8000 Devices\)](#) and [Application Note 38 \(Configuring Multiple FLEX 8000 Devices\)](#).

Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. [Table 51](#) shows the data source for each of the six configuration schemes.

Table 51. Data Source for Configuration		
Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera configuration device
Active parallel up	APU	Parallel configuration device
Active parallel down	APD	Parallel configuration device
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
ADD0	78	76	78	77	106	N3	6
DATA7	3	2	90	89	131	P8	140
DATA6	4	4	91	91	132	P10	139
DATA5	6	6	92	95	133	R12	138
DATA4	7	7	95	96	134	R13	136
DATA3	8	8	97	97	135	P13	135
DATA2	9	9	99	98	137	R14	133
DATA1	13	13	4	4	138	N15	132
DATA0	14	14	5	5	140	K13	129
SDOUT (3)	79	78	79	79	23	P4	97
TDI (4)	55	45 (5)	54	—	96	—	17
TDO (4)	27	27 (5)	18	—	18	—	102
TCK (4), (6)	72	44 (5)	72	—	88	—	27
TMS (4)	20	43 (5)	11	—	86	—	29
TRST (7)	52	52 (8)	50	—	71	—	45
Dedicated Inputs (10)	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
VCCIO	—	—	—	—	16, 40, 60, 69, 91, 112, 122, 141	—	23, 47, 57, 69, 79, 104, 127, 137, 149, 159

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
GND	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
No Connect (N.C.)	—	—	61, 62, 119, 120, 181, 182, 239, 240	—	—	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins (9)	148	180	180	177	204	204