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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	162
Number of Logic Elements/Cells	1296
Total RAM Bits	-
Number of I/O	181
Number of Gates	16000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf81500aqc240-4

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes
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...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see [Table 2](#))
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

Table 2. FLEX 8000 Package Options & I/O Pin Count *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

Note:

- (1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce routing flexibility. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

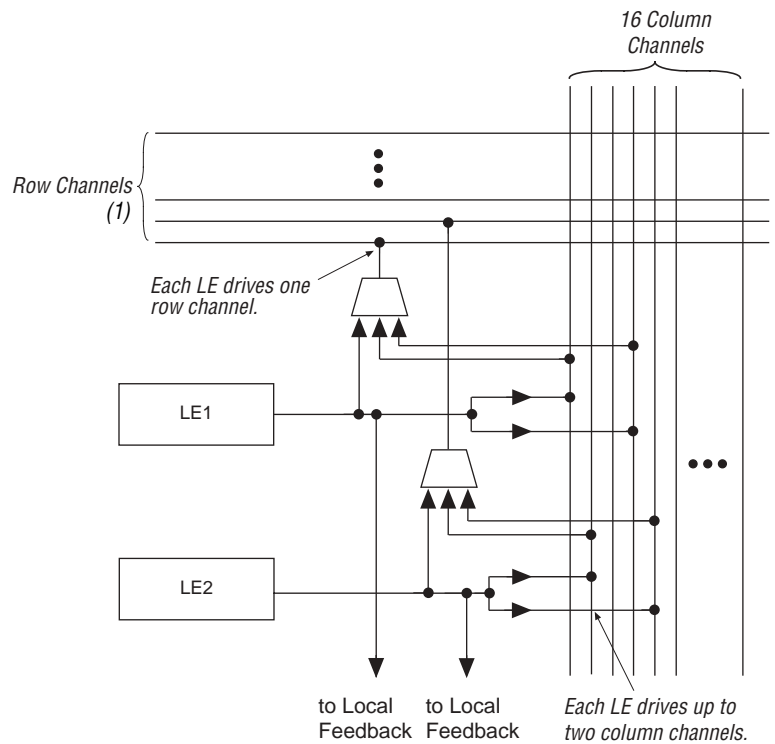
Figure 4 shows how an n -bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to another LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal (row) and vertical (column) routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing structure in FPGAs requires switch matrices to connect a variable number of routing paths, which increases the delays between logic resources and reduces performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. **Figure 8** shows how an LE drives the row and column interconnect.

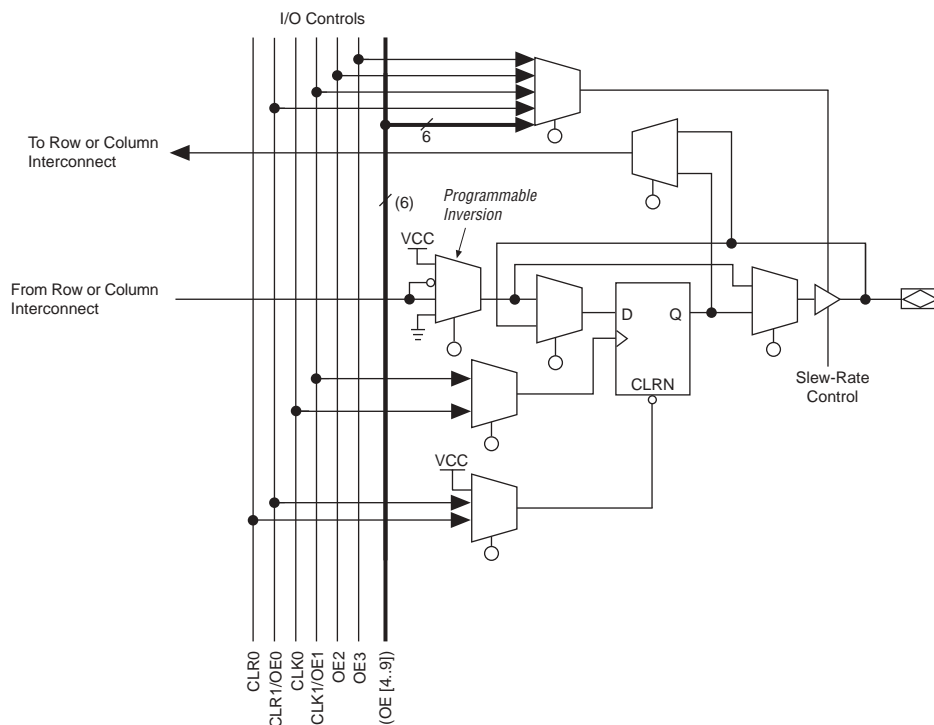
Figure 8. FLEX 8000 LAB Connections to Row & Column Interconnect



Note:
(1) See Table 4 for the number of row channels.

Figure 10. FLEX 8000 IOE

Numbers in parentheses are for EPF81500A devices only.



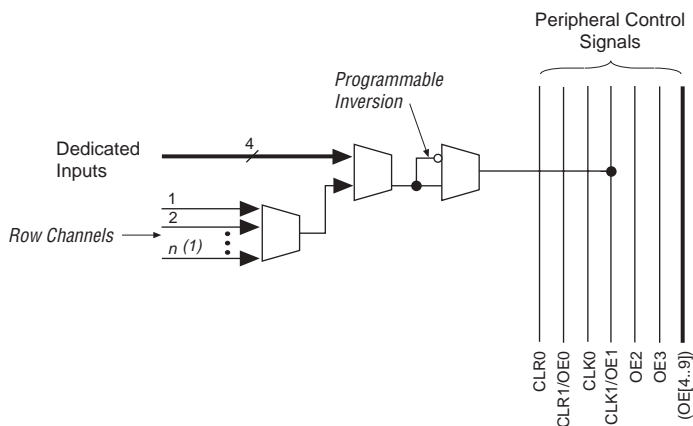
Row-to-IOE Connections

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an n -to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

Figure 13. FLEX 8000 Peripheral Bus

Numbers in parentheses are for EPF81500A devices.



Note:

- (1) $n = 13$ for EPF8282A and EPF8282AV devices.
- $n = 21$ for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
- $n = 27$ for EPF81500A devices.

MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1} . See [Table 8 on page 26](#).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

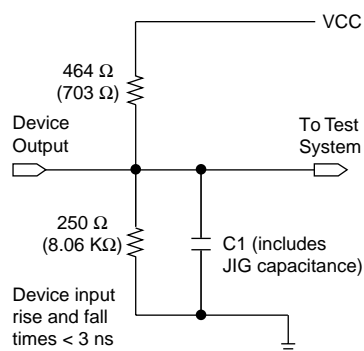
The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in [Table 6](#).

Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

Figure 15. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices or outputs. Numbers without parentheses are for 5.0-V devices or outputs.



Operating Conditions

Tables 9 through 12 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V FLEX 8000 devices.

Table 9. FLEX 8000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	-2.0	7.0	V
V_I	DC input voltage		-2.0	7.0	V
I_{OUT}	DC output current, per pin		-25	25	mA
T_{STG}	Storage temperature	No bias	-65	150	° C
T_{AMB}	Ambient temperature	Under bias	-65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP, under bias		135	° C

Table 15. FLEX 8000 3.3-V Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	High-level output voltage	$I_{OH} = -0.1$ mA DC (5)	$V_{CC} - 0.2$			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA DC (5)			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	-10		10	μ A
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	-40		40	μ A
I_{CC0}	V_{CC} supply current (standby)	$V_I =$ ground, no load (6)		0.3	10	mA

Table 16. FLEX 8000 3.3-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) The maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
- (4) These values are specified in [Table 14 on page 29](#).
- (5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
- (6) Typical values are for $T_A = 25^\circ$ C and $V_{CC} = 3.3$ V.
- (7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

Table 23. EPF8282A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.2		7.2		7.2	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 28. EPF8282AV Logic Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{LUT}		3.2		7.3	ns
t_{CLUT}		0.0		1.4	ns
t_{RLUT}		1.5		5.1	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		0.9		2.8	ns
t_{CICO}		0.6		1.5	ns
t_{CGEN}		0.7		2.2	ns
t_{CGENR}		1.5		3.7	ns
t_C		2.5		4.7	ns
t_{CH}	4.0		6.0		ns
t_{CL}	4.0		6.0		ns
t_{CO}		0.6		0.9	ns
t_{COMB}		0.6		0.9	ns
t_{SU}	1.2		2.4		ns
t_H	1.5		4.6		ns
t_{PRE}		0.8		1.3	ns
t_{CLR}		0.8		1.3	ns

Table 29. EPF8282AV External Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t _{DRR}		24.8		50.1	ns
t _{ODH}	1.0		1.0		ns

Table 30. EPF8452A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		—		—		—	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		—		—		—	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 31. EPF8452A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 40. EPF8820A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 41. EPF8820A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DRR}		16.0		20.0		25.0	ns
t _{ODH}	1.0		1.0		1.0		ns

Table 42. EPF81188A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 43. EPF81188A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 44. EPF81188A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_C		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_H	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 45. EPF81188A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t _{DRR}		16.0		20.0		25.0	ns
t _{ODH}	1.0		1.0		1.0		ns

Power Consumption

The supply power (P) for FLEX 8000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = [(I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC}] + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in Table 11 on page 28 and Table 15 on page 30. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#). The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times f_{MAX} \times N \times \text{tog}_{LC} \times \frac{\mu A}{\text{MHz} \times \text{LE}}$$

The parameters in this equation are shown below:

- f_{MAX} = Maximum operating frequency in MHz
- N = Total number of logic cells used in the device
- tog_{LC} = Average percentage of logic cells toggling at each clock
- K = Constant, shown in [Table 50](#)

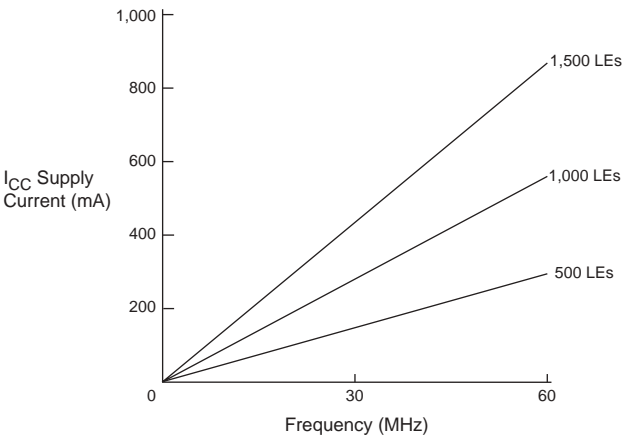
Table 50. Values for Constant K	
Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

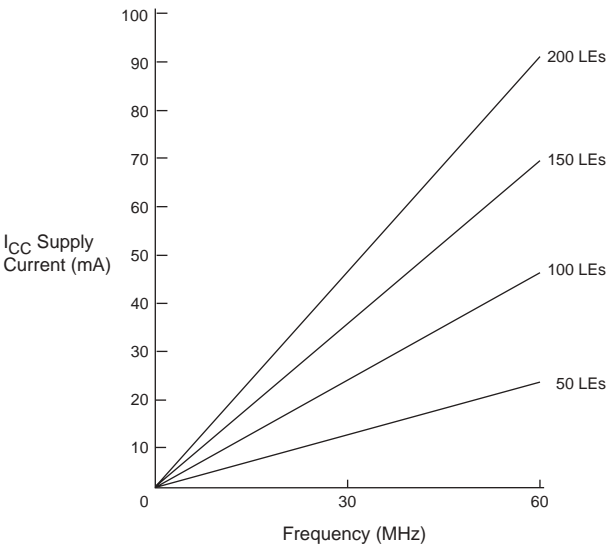
[Figure 20](#) shows the relationship between I_{CC} and operating frequency for several LE utilization values.

Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices



3.3-V FLEX 8000 Devices



Configuration & Operation



The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to [Application Note 33 \(Configuring FLEX 8000 Devices\)](#) and [Application Note 38 \(Configuring Multiple FLEX 8000 Devices\)](#).

Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. [Table 51](#) shows the data source for each of the six configuration schemes.

Table 51. Data Source for Configuration		
Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera configuration device
Active parallel up	APU	Parallel configuration device
Active parallel down	APD	Parallel configuration device
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP (2)	A15	C14	237	237	W1	304
MSEL0 (2)	B14	G15	21	19	N1	26
MSEL1 (2)	R15	L15	40	38	H3	51
nSTATUS (2)	P2	L3	141	142	G19	178
nCONFIG (2)	R1	R4	117	120	B18	152
DCLK (2)	B2	C4	184	183	U18	230
CONF_DONE (2)	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDynBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
DATA4	A5	C7	198	194	W16	248
DATA3	B5	D7	196	193	W17	246
DATA2	E6	B5	194	190	V16	243
DATA1	D5	A3	191	189	U16	241
DATA0	C4	A2	189	187	V17	239
SDOUT (3)	K1	N2	135	136	F19	169
TDI	F15 (4)	–	–	63 (14)	B1 (14)	80 (14)
TDO	J2 (4)	–	–	117	C17	149
TCK (6)	J14 (4)	–	–	116 (14)	A19 (14)	148 (14)
TMS	J12 (4)	–	–	64 (14)	C2 (14)	81 (14)
TRST (7)	P14	–	–	115 (14)	A18 (14)	145 (14)
Dedicated Inputs (10)	F4, L1, K12, E15	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
VCCINT (5.0 V)	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO (5.0 V or 3.3 V)	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
GND	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
No Connect (N.C.)	—	—	61, 62, 119, 120, 181, 182, 239, 240	—	—	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins (9)	148	180	180	177	204	204