Altera - EPF81500ARC304-4 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	162
Number of Logic Elements/Cells	1296
Total RAM Bits	-
Number of I/O	208
Number of Gates	16000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	304-BFQFP
Supplier Device Package	304-RQFP (40x40)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf81500arc304-4

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes

...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

Table 2. FLEX 8000 Package Options & I/O Pin Count *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

Note:

(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide-data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 3 shows FLEX 8000 performance and LE requirements for typical applications.

Table 3. FLEX 8000 Performance

Application	LEs Used	Speed Grade			Units
		A-2	A-3	A-4	
16-bit loadable counter	16	125	95	83	MHz
16-bit up/down counter	16	125	95	83	MHz
24-bit accumulator	24	87	67	58	MHz
16-bit address decode	4	4.2	4.9	6.3	ns
16-to-1 multiplexer	10	6.6	7.9	9.5	ns

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial configuration devices, or with data provided by a system controller. Altera offers the EPC1, EPC1213, EPC1064, and EPC1441 configuration devices, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32 K × 8 bit or larger configuration device, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation. For information on how to configure FLEX 8000 devices, go to the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 8000 architecture.

For more information on the MAX+PLUS II software, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

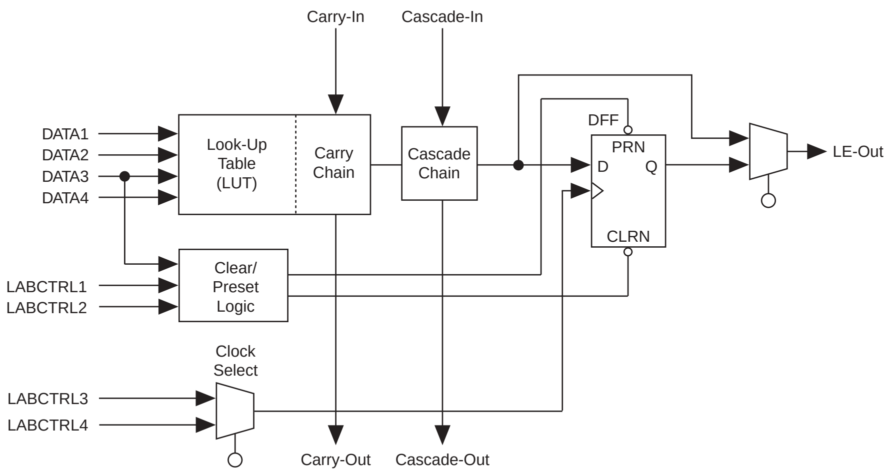
Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

Figure 3. FLEX 8000 LE

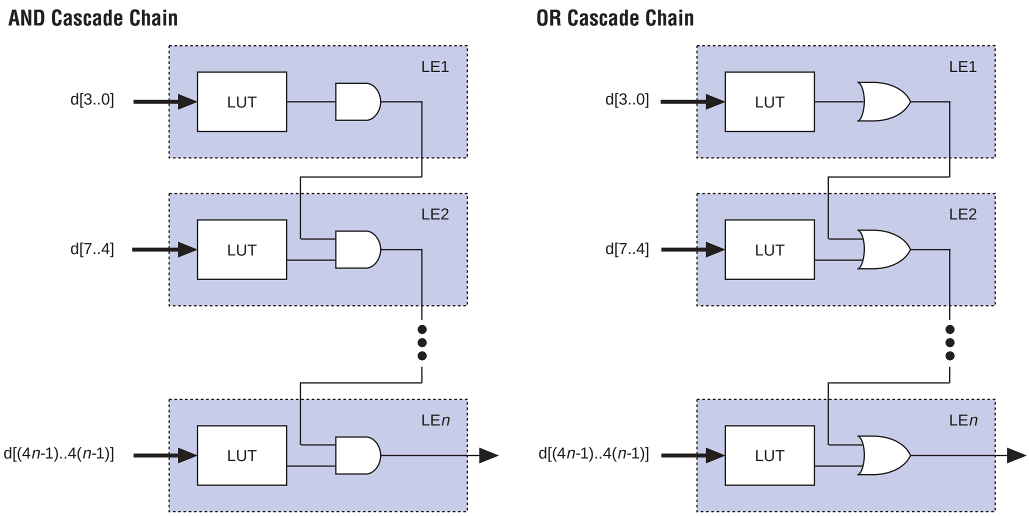


The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

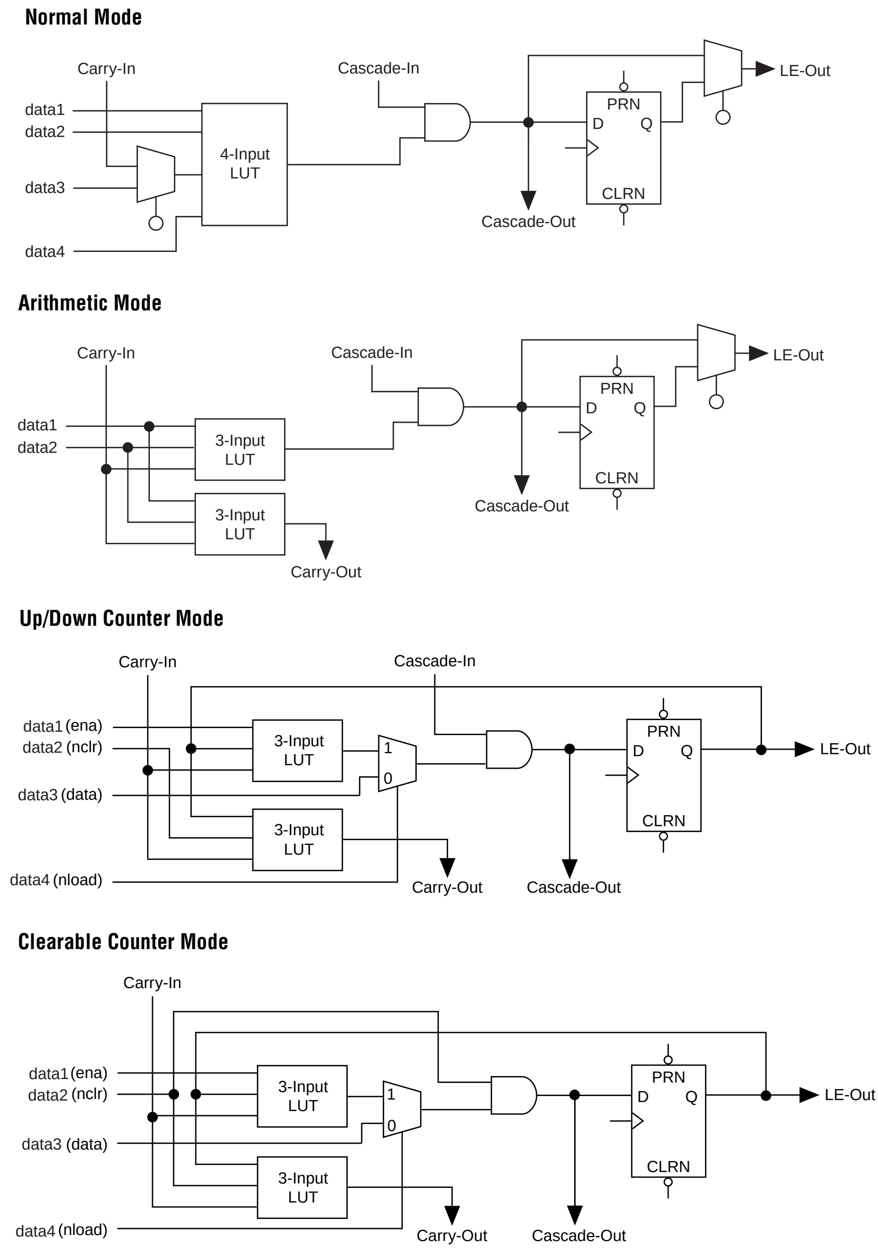
Figure 5. FLEX 8000 Cascade Chain Operation



LE Operating Modes

The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Figure 6. FLEX 8000 LE Operating Modes



Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the `DATA3`, `LABCTRL1`, and `LABCTRL2` inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that `LABCTRL1` implements an asynchronous load. The data to be loaded is driven to `DATA3`; when `LABCTRL1` is asserted, `DATA3` is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

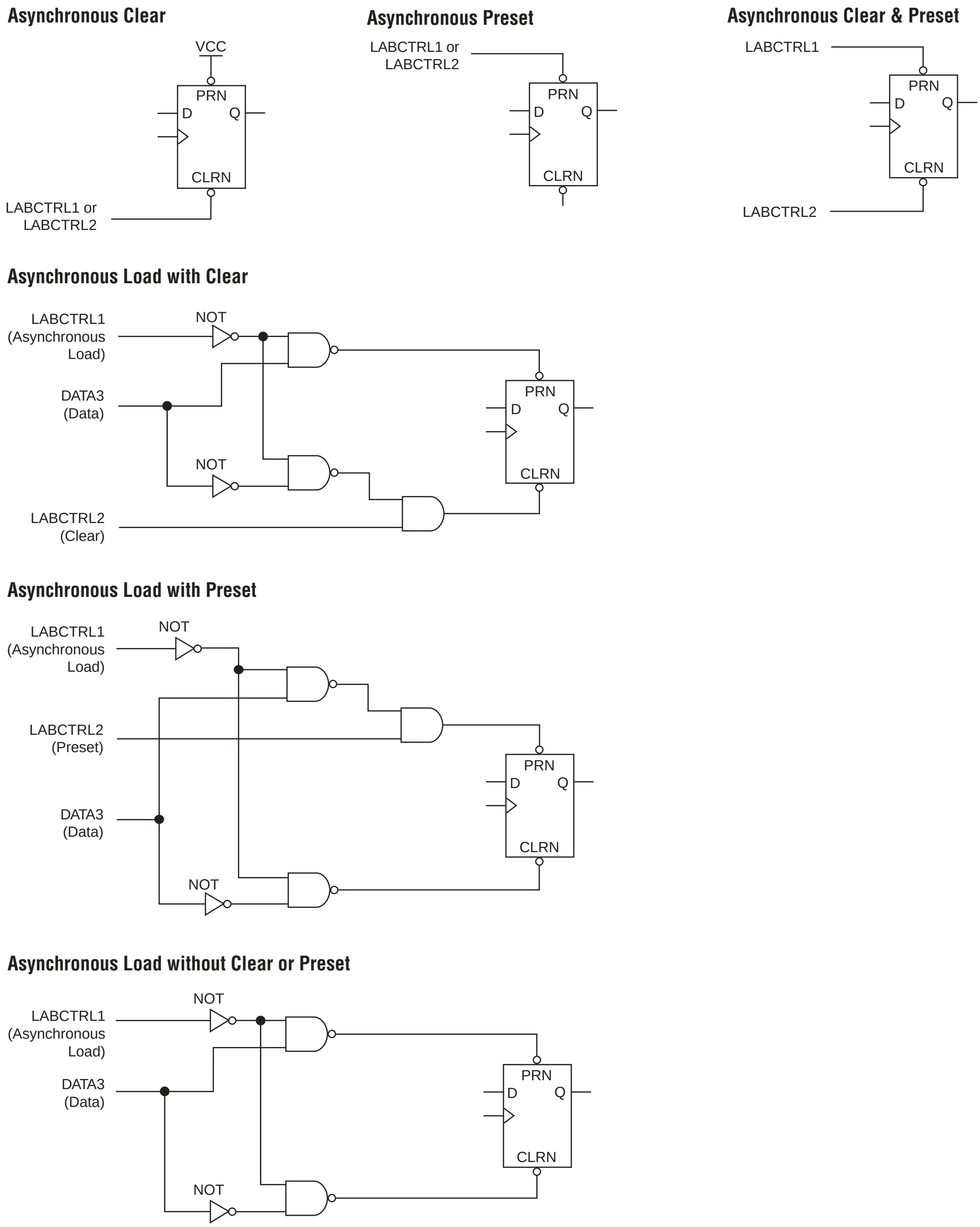


Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

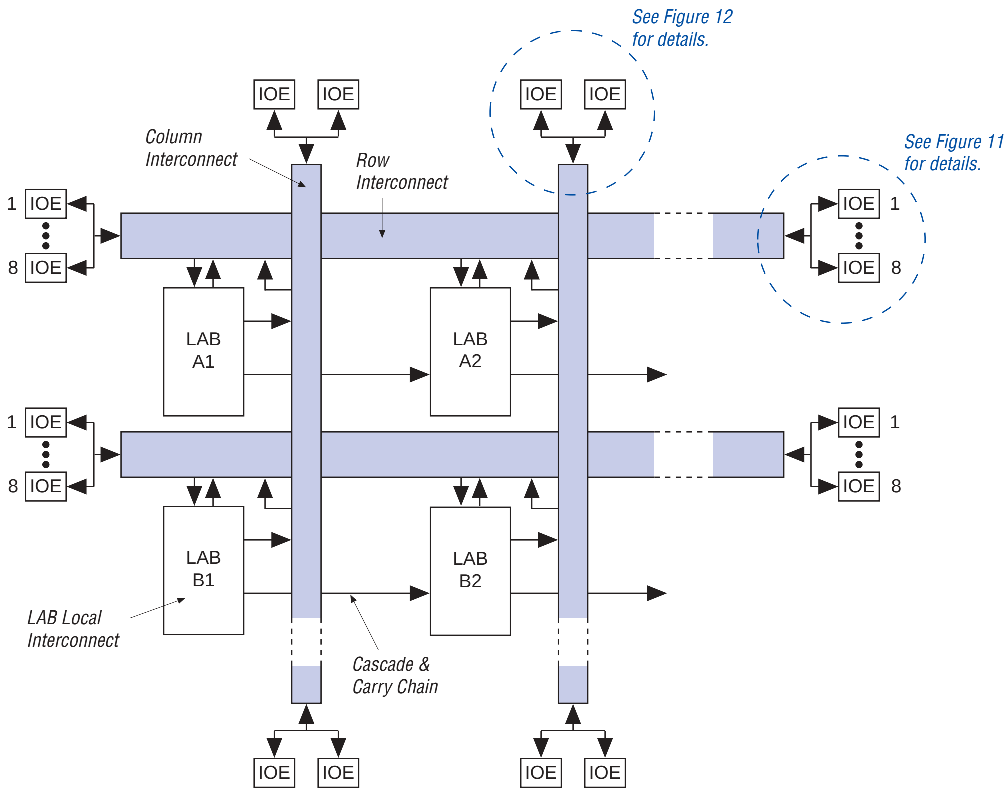
Table 4. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282A EPF8282AV	2	168	13	16
EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820A	4	168	21	16
EPF81188A	6	168	21	16
EPF81500A	6	216	27	16

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 9. FLEX 8000 Device Interconnect Resources

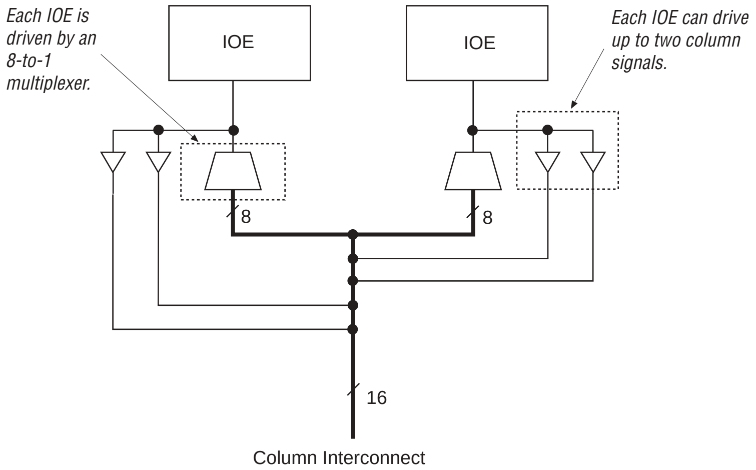
Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 10 shows the IOE block diagram.

Figure 12. FLEX 8000 Column-to-IOE Connections



In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. Figure 13 on page 22 shows how two output enable signals are shared with one clock and one clear signal.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 5. Row Sources of FLEX 8000 Peripheral Control Signals

Peripheral Control Signal	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	–	–	–	–	–	Row B
OE5	–	–	–	–	–	Row C
OE6	–	–	–	–	–	Row D
OE7	–	–	–	–	–	Row D
OE8	–	–	–	–	–	Row E
OE9	–	–	–	–	–	Row F

Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

For more information on high-speed system design, go to *Application Note 75 (High-Speed Board Designs)*.

Table 17. FLEX 8000 Internal Timing Parameters *Note (1)*

Symbol	Parameter
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock; IOE register recovery time after asynchronous clear
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V C1 = 35 pF *(2)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF *(2)*
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF *(2)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)*

Table 18. FLEX 8000 LE Timing Parameters *Note (1)*

Symbol	Parameter
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	LE register clock high time
t_{CL}	LE register clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 19. FLEX 8000 Interconnect Timing Parameters *Note (1)*	
Symbol	**Parameter**
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay *(4)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay *(4)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 20. FLEX 8000 External Reference Timing Characteristics *Note (5)*	
Symbol	**Parameter**
$\mathbf{t_{DRR}}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)*
$\mathbf{t_{ODH}}$	Output data hold time after clock *(7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.
(4) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76* (*Understanding FLEX 8000 Timing*).
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

Table 28. EPF8282AV Logic Element Timing Parameters					
Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{LUT}		3.2		7.3	ns
t_{CLUT}		0.0		1.4	ns
t_{RLUT}		1.5		5.1	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		0.9		2.8	ns
t_{CICO}		0.6		1.5	ns
t_{CGEN}		0.7		2.2	ns
t_{CGENR}		1.5		3.7	ns
t_{C}		2.5		4.7	ns
t_{CH}	4.0		6.0		ns
t_{CL}	4.0		6.0		ns
t_{CO}		0.6		0.9	ns
t_{COMB}		0.6		0.9	ns
t_{SU}	1.2		2.4		ns
t_{H}	1.5		4.6		ns
t_{PRE}		0.8		1.3	ns
t_{CLR}		0.8		1.3	ns

Table 29. EPF8282AV External Timing Parameters					
Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{DRR}		24.8		50.1	ns
t_{ODH}	1.0		1.0		ns

Table 38. EPF8820A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 39. EPF8820A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 42. EPF81188A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 43. EPF81188A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
DATA4	154	127	E17	165	172	170
DATA3	157	124	G15	162	171	168
DATA2	159	122	F15	160	167	166
DATA1	11	115	E16	149	165	163
DATA0	12	113	C16	147	162	161
SDOUT *(3)*	128	152	C7 *(11)*	198	124	119
TDI *(4)*	–	55	R11	72	20	–
TDO *(4)*	–	95	B9	120	129	–
TCK *(4)*, *(6)*	–	57	U8	74	30	–
TMS *(4)*	–	59	U7	76	32	–
TRST *(7)*	–	40	R3	54	54	–
Dedicated Inputs *(10)*	5, 36, 85, 116	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146
VCCINT (5.0 V)	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147
VCCIO (5.0 V or 3.3 V)	–	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192
GND	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201
No Connect (N.C.)	2, 3, 38, 39, 70, 82, 83, 118, 119, 148	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4 *(12)*	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208
Total User I/O Pins *(9)*	116	114	132, 148 *(13)*	132	148	144

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)						
Pin Name	**225-Pin BGA EPF8820A**	**232-Pin PGA EPF81188A**	**240-Pin PQFP EPF81188A**	**240-Pin PQFP EPF81500A**	**280-Pin PGA EPF81500A**	**304-Pin RQFP EPF81500A**
GND	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
No Connect (N.C.)	–	–	61, 62, 119, 120, 181, 182, 239, 240	–	–	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins *(9)*	148	180	180	177	204	204

Notes to tables:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a V_{CC} pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) SDOUT does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.