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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	26
Number of Logic Elements/Cells	208
Total RAM Bits	-
Number of I/O	68
Number of Gates	2500
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf8282alc84-3">https://www.e-xfl.com/product-detail/intel/epf8282alc84-3</a>

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes
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## ...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see [Table 2](#))
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

**Table 2. FLEX 8000 Package Options & I/O Pin Count** *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

**Note:**

- (1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

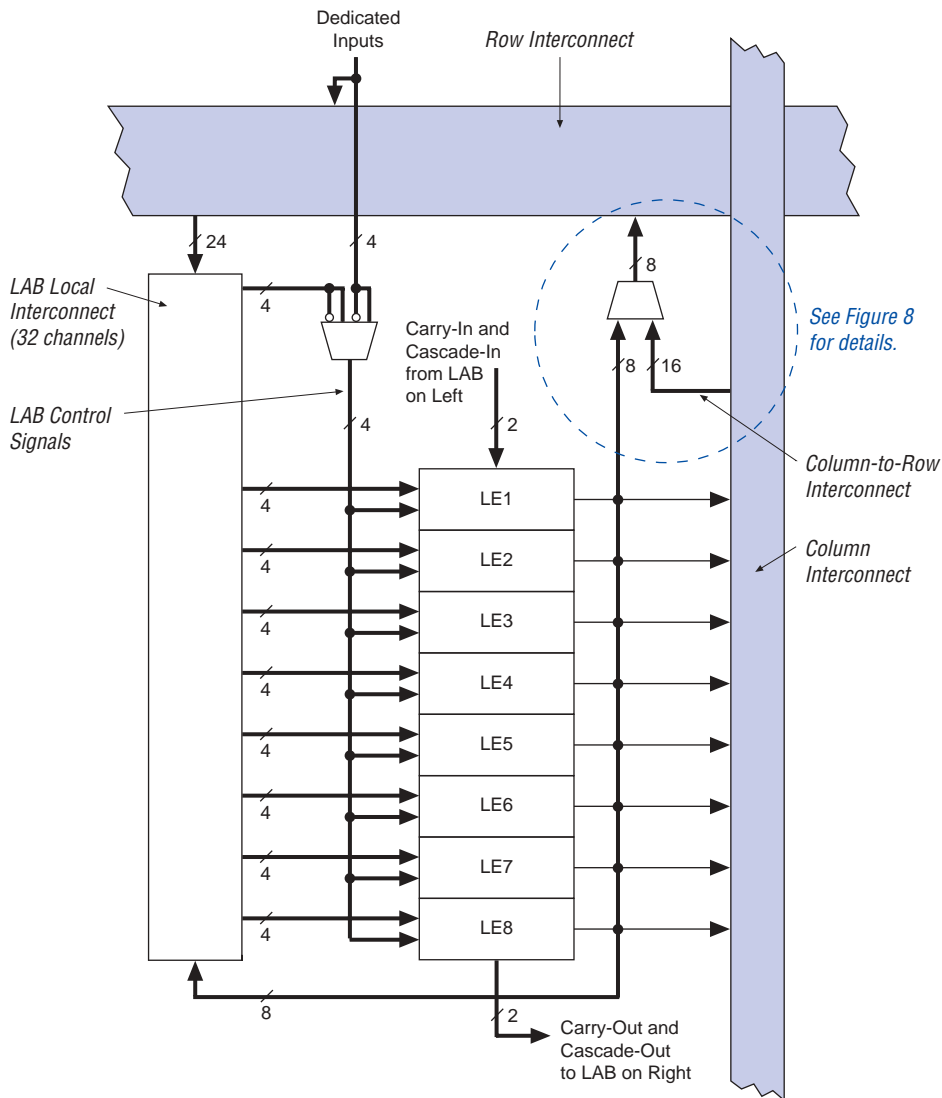
## General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block



### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in signal are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-Out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data output (Q) of the programmable register.

### Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 6, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three bits: a, b, and the carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports a cascade chain.

### Up/Down Counter Mode

The up/down counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control; the clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, and the output of this multiplexer is ANDed with a synchronous clear.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

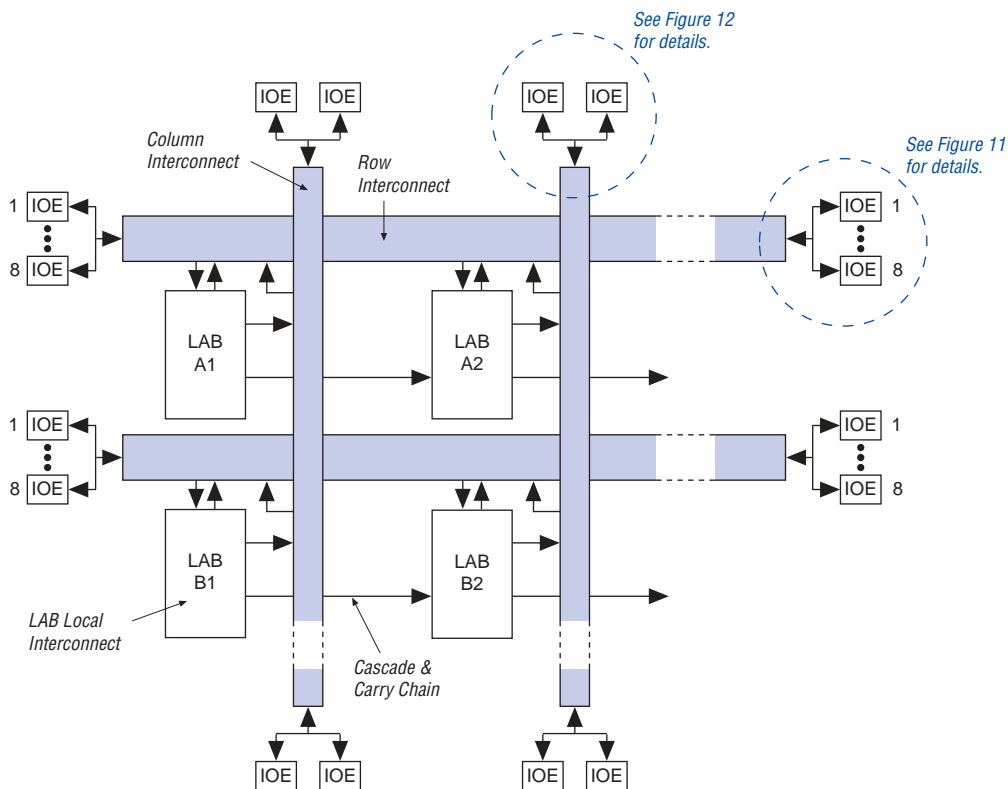
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See [Figure 7](#).

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

**Figure 9. FLEX 8000 Device Interconnect Resources**

Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.

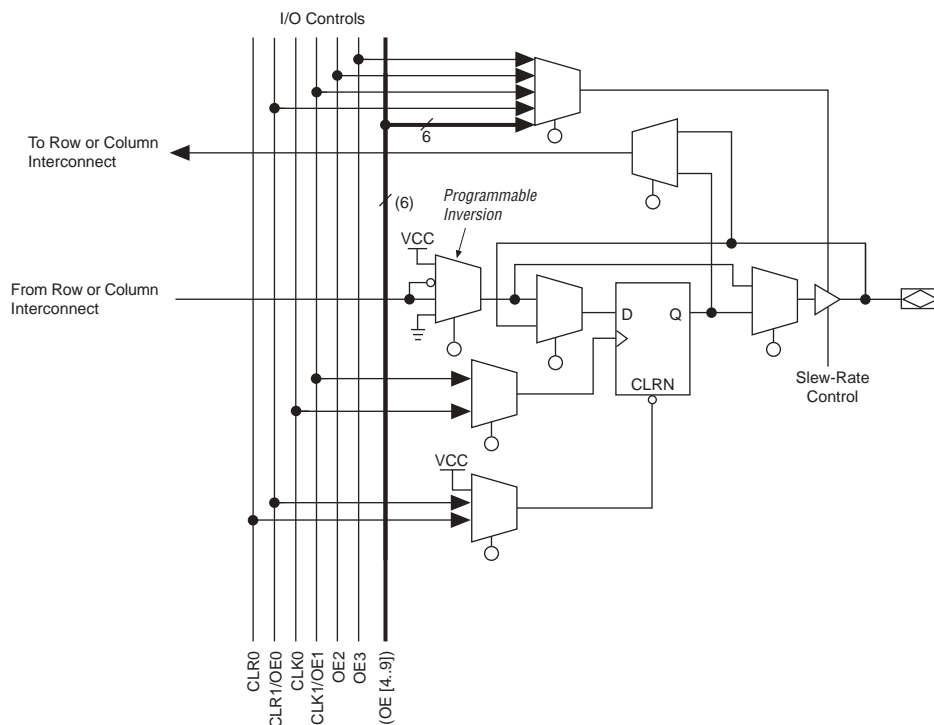


## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. [Figure 10](#) shows the IOE block diagram.

**Figure 10. FLEX 8000 IOE**

Numbers in parentheses are for EPF81500A devices only.



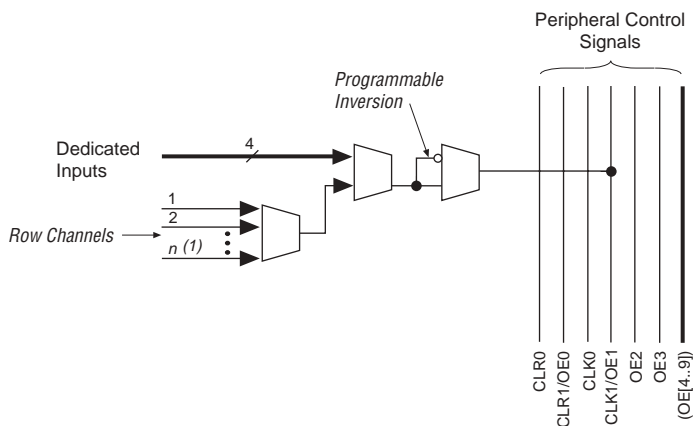
### Row-to-IOE Connections

Figure 11 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an  $n$ -to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500A devices use a 27-to-1 multiplexer; EPF81188A, EPF8820A, EPF8636A, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282A and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

**Figure 13. FLEX 8000 Peripheral Bus**

*Numbers in parentheses are for EPF81500A devices.*



**Note:**

- (1)  $n = 13$  for EPF8282A and EPF8282AV devices.
- $n = 21$  for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
- $n = 27$  for EPF81500A devices.



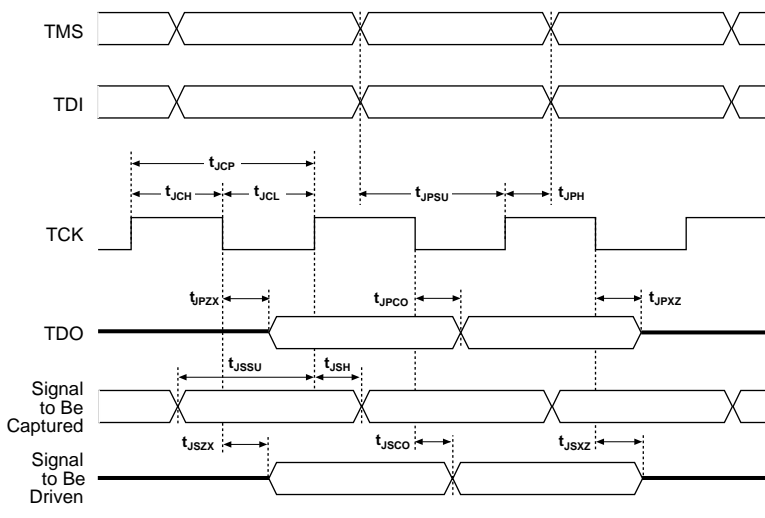
The instruction register length for FLEX 8000 devices is three bits. [Table 7](#) shows the boundary-scan register length for FLEX 8000 devices.

**Table 7. FLEX 8000 Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPF8282A, EPF8282AV	273
EPF8636A	417
EPF8820A	465
EPF81500A	645

FLEX 8000 devices that support JTAG include weak pull-ups on the JTAG pins. [Figure 14](#) shows the timing requirements for the JTAG signals.

**Figure 14. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Waveforms**



[Table 8](#) shows the timing parameters and values for EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices.

**Table 8. JTAG Timing Parameters & Values**

Symbol	Parameter	EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A		Unit
		Min	Max	
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high-impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high-impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high-impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high-impedance		35	ns



For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in *Figure 15*. Designers can use multiple test patterns to configure devices during all stages of the production flow.

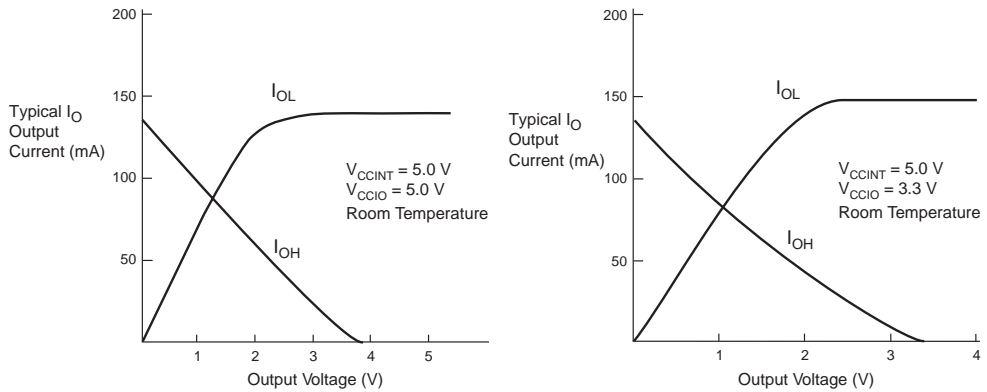
**Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)**

Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

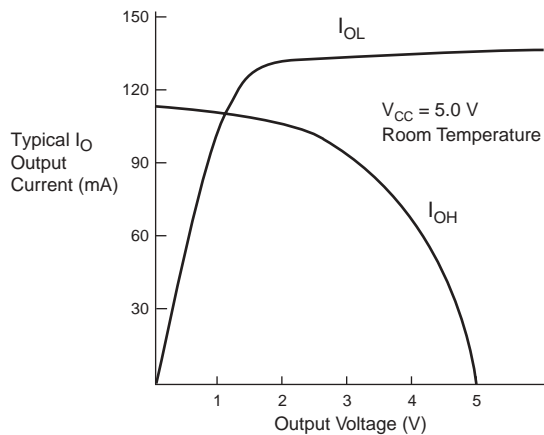
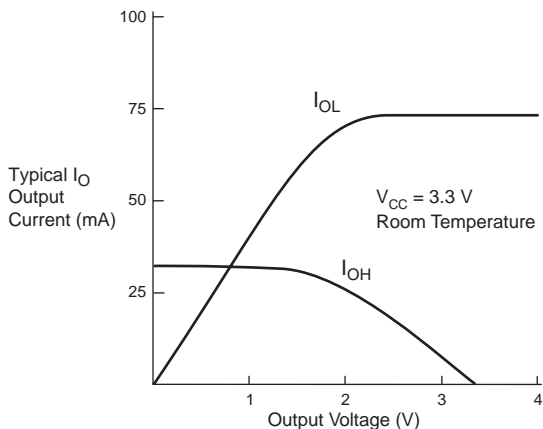
**Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V  $V_{CCIO}$** 

Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

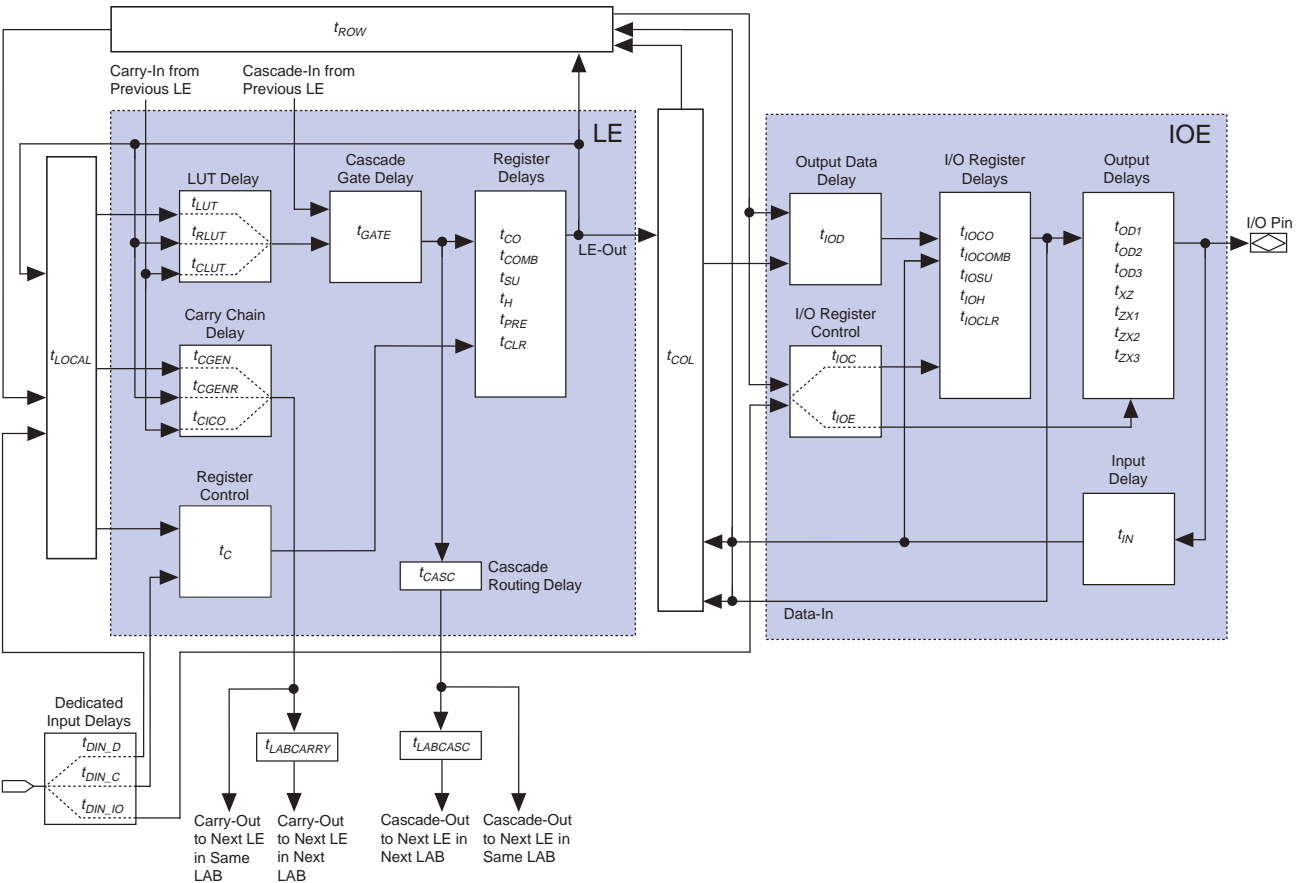
**Figure 18. Output Drive Characteristics of EPF8282AV Devices**

## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

Figure 19. FLEX 8000 Timing Model



**Table 24. EPF8282A LE Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		2.0		2.5		3.2	ns
$t_{CLUT}$		0.0		0.0		0.0	ns
$t_{RLUT}$		0.9		1.1		1.5	ns
$t_{GATE}$		0.0		0.0		0.0	ns
$t_{CASC}$		0.6		0.7		0.9	ns
$t_{CICO}$		0.4		0.5		0.6	ns
$t_{CGEN}$		0.4		0.5		0.7	ns
$t_{CGENR}$		0.9		1.1		1.5	ns
$t_C$		1.6		2.0		2.5	ns
$t_{CH}$	4.0		4.0		4.0		ns
$t_{CL}$	4.0		4.0		4.0		ns
$t_{CO}$		0.4		0.5		0.6	ns
$t_{COMB}$		0.4		0.5		0.6	ns
$t_{SU}$	0.8		1.1		1.2		ns
$t_H$	0.9		1.1		1.5		ns
$t_{PRE}$		0.6		0.7		0.8	ns
$t_{CLR}$		0.6		0.7		0.8	ns

**Table 25. EPF8282A External Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t <sub>DRR</sub>		15.8		19.8		24.8	ns
t <sub>ODH</sub>	1.0		1.0		1.0		ns

**Table 32. EPF8452A LE Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		2.0		2.3		3.0	ns
$t_{CLUT}$		0.0		0.2		0.1	ns
$t_{RLUT}$		0.9		1.6		1.6	ns
$t_{GATE}$		0.0		0.0		0.0	ns
$t_{CASC}$		0.6		0.7		0.9	ns
$t_{CICO}$		0.4		0.5		0.6	ns
$t_{CGEN}$		0.4		0.9		0.8	ns
$t_{CGENR}$		0.9		1.4		1.5	ns
$t_C$		1.6		1.8		2.4	ns
$t_{CH}$	4.0		4.0		4.0		ns
$t_{CL}$	4.0		4.0		4.0		ns
$t_{CO}$		0.4		0.5		0.6	ns
$t_{COMB}$		0.4		0.5		0.6	ns
$t_{SU}$	0.8		1.0		1.1		ns
$t_H$	0.9		1.1		1.4		ns
$t_{PRE}$		0.6		0.7		0.8	ns
$t_{CLR}$		0.6		0.7		0.8	ns

**Table 33. EPF8452A External Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t <sub>DRR</sub>		16.0		20.0		25.0	ns
t <sub>ODH</sub>	1.0		1.0		1.0		ns

**Table 34. EPF8636A I/O Element Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		0.7		0.8		0.9	ns
$t_{IOC}$		1.7		1.8		1.9	ns
$t_{IOE}$		1.7		1.8		1.9	ns
$t_{IOCO}$		1.0		1.0		1.0	ns
$t_{IOCOMB}$		0.3		0.2		0.1	ns
$t_{IOSU}$	1.4		1.6		1.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.2		1.2		1.2	ns
$t_{IN}$		1.5		1.6		1.7	ns
$t_{OD1}$		1.1		1.4		1.7	ns
$t_{OD2}$		1.6		1.9		2.2	ns
$t_{OD3}$		4.6		4.9		5.2	ns
$t_{XZ}$		1.4		1.6		1.8	ns
$t_{ZX1}$		1.4		1.6		1.8	ns
$t_{ZX2}$		1.9		2.1		2.3	ns
$t_{ZX3}$		4.9		5.1		5.3	ns

**Table 35. EPF8636A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
$t_{LOCAL}$		0.5		0.5		0.7	ns
$t_{ROW}$		5.0		5.0		5.0	ns
$t_{COL}$		3.0		3.0		3.0	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		7.0		7.0		7.5	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns



**Table 46. EPF81500A I/O Element Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		0.7		0.8		0.9	ns
$t_{IOC}$		1.7		1.8		1.9	ns
$t_{IOE}$		1.7		1.8		1.9	ns
$t_{IOCO}$		1.0		1.0		1.0	ns
$t_{IOCOMB}$		0.3		0.2		0.1	ns
$t_{IOSU}$	1.4		1.6		1.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.2		1.2		1.2	ns
$t_{IN}$		1.5		1.6		1.7	ns
$t_{OD1}$		1.1		1.4		1.7	ns
$t_{OD2}$		1.6		1.9		2.2	ns
$t_{OD3}$		4.6		4.9		5.2	ns
$t_{XZ}$		1.4		1.6		1.8	ns
$t_{ZX1}$		1.4		1.6		1.8	ns
$t_{ZX2}$		1.9		2.1		2.3	ns
$t_{ZX3}$		4.9		5.1		5.3	ns

**Table 47. EPF81500A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
$t_{LOCAL}$		0.5		0.6		0.8	ns
$t_{ROW}$		6.2		6.2		6.2	ns
$t_{COL}$		3.0		3.0		3.0	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		8.2		8.2		8.7	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns

## Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

## Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. [Table 51](#) shows the data source for each of the six configuration schemes.

<b>Table 51. Data Source for Configuration</b>		
<b>Configuration Scheme</b>	<b>Acronym</b>	<b>Data Source</b>
Active serial	AS	Altera configuration device
Active parallel up	APU	Parallel configuration device
Active parallel down	APD	Parallel configuration device
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

## Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)**

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
nSP (2)	75	75	75	76	110	R1	1
MSEL0 (2)	74	74	74	75	109	P2	2
MSEL1 (2)	53	53	51	51	72	A1	44
nSTATUS (2)	32	32	24	25	37	C13	82
nCONFIG (2)	33	33	25	26	38	A15	81
DCLK (2)	10	10	100	100	143	P14	125
CONF_DONE (2)	11	11	1	1	144	N13	124
nWS	30	30	22	23	33	F13	87
nRS	48	48	42	45	31	C6	89
RDCLK	49	49	45	46	12	B5	110
nCS	29	29	21	22	4	D15	118
CS	28	28	19	21	3	E15	121
RDYnBUSY	77	77	77	78	20	P3	100
CLKUSR	50	50	47	47	13	C5	107
ADD17	51	51	49	48	75	B4	40
ADD16	36	55	28	54	76	E2	39
ADD15	56	56	55	55	77	D1	38
ADD14	57	57	57	57	78	E1	37
ADD13	58	58	58	58	79	F3	36
ADD12	60	60	59	60	83	F2	32
ADD11	61	61	60	61	85	F1	30
ADD10	62	62	61	62	87	G2	28
ADD9	63	63	62	64	89	G1	26
ADD8	64	64	64	65	92	H1	22
ADD7	65	65	65	66	94	H2	20
ADD6	66	66	66	67	95	J1	18
ADD5	67	67	67	68	97	J2	16
ADD4	69	69	68	70	102	K2	11
ADD3	70	70	69	71	103	K1	10
ADD2	71	71	71	72	104	K3	8
ADD1	76	72	76	73	105	M1	7

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 3 of 3)**

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	19, 44, 69, 94	7, 17, 27, 39, 54, 80, 81, 100, 101, 128, 142	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155
No Connect (N.C.)	—	—	—	2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99	—	—	—
Total User I/O Pins (9)	64	64	74	64	108	116	116

**Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)**

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
DATA4	A5	C7	198	194	W16	248
DATA3	B5	D7	196	193	W17	246
DATA2	E6	B5	194	190	V16	243
DATA1	D5	A3	191	189	U16	241
DATA0	C4	A2	189	187	V17	239
SDOUT (3)	K1	N2	135	136	F19	169
TDI	F15 (4)	–	–	63 (14)	B1 (14)	80 (14)
TDO	J2 (4)	–	–	117	C17	149
TCK (6)	J14 (4)	–	–	116 (14)	A19 (14)	148 (14)
TMS	J12 (4)	–	–	64 (14)	C2 (14)	81 (14)
TRST (7)	P14	–	–	115 (14)	A18 (14)	145 (14)
Dedicated Inputs (10)	F4, L1, K12, E15	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
VCCINT (5.0 V)	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO (5.0 V or 3.3 V)	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300