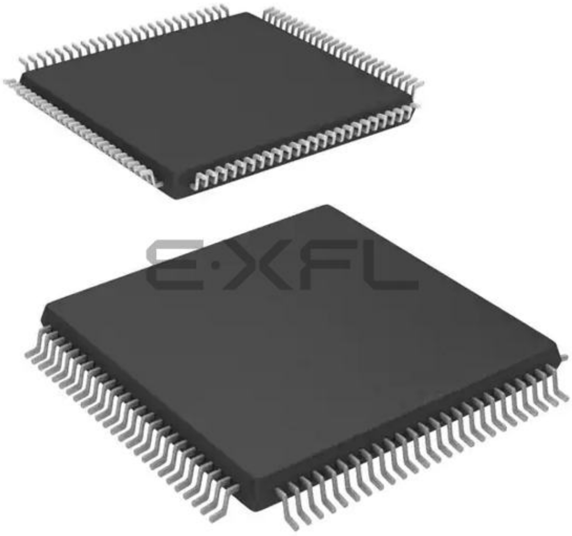

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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

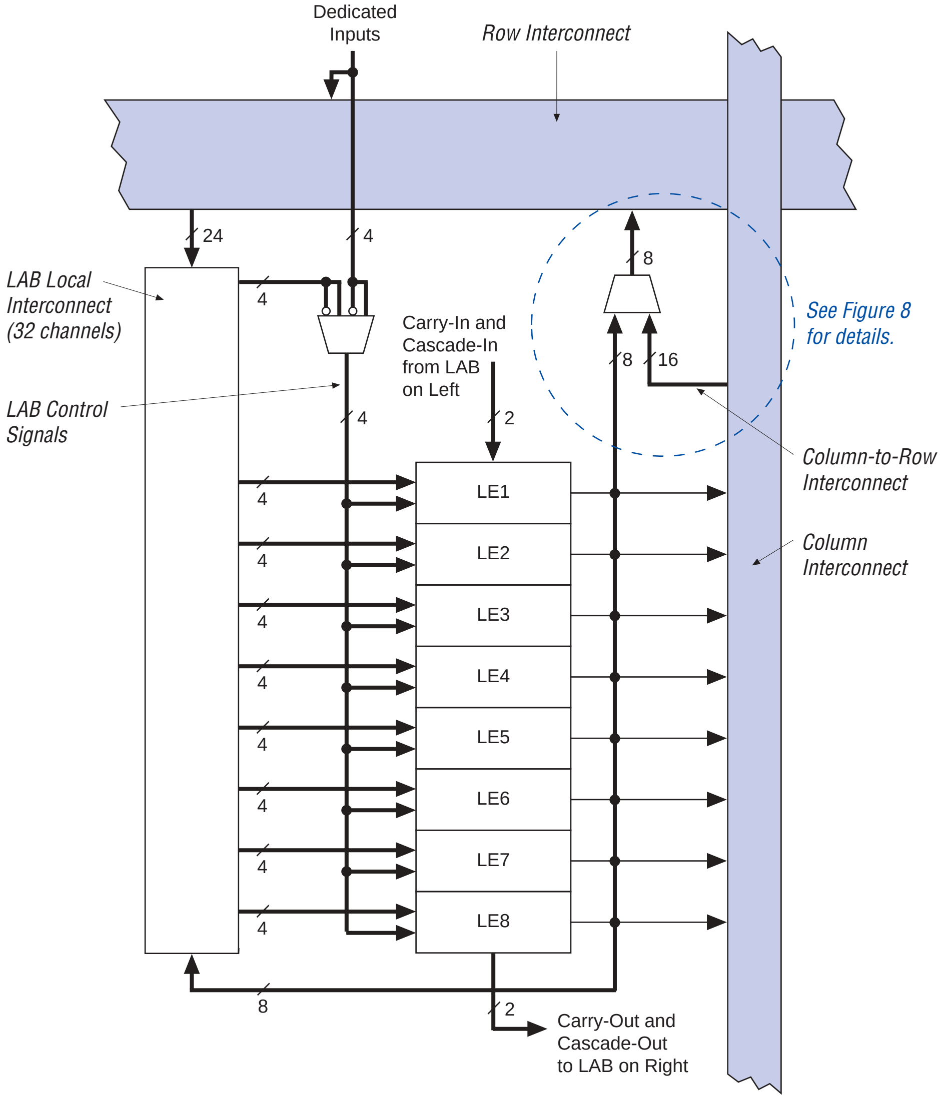
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 26 |
| Number of Logic Elements/Cells | 208 |
| Total RAM Bits | - |
| Number of I/O | 78 |
| Number of Gates | 2500 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf8282atc100-3 |

## Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

***Figure 2. FLEX 8000 Logic Array Block***

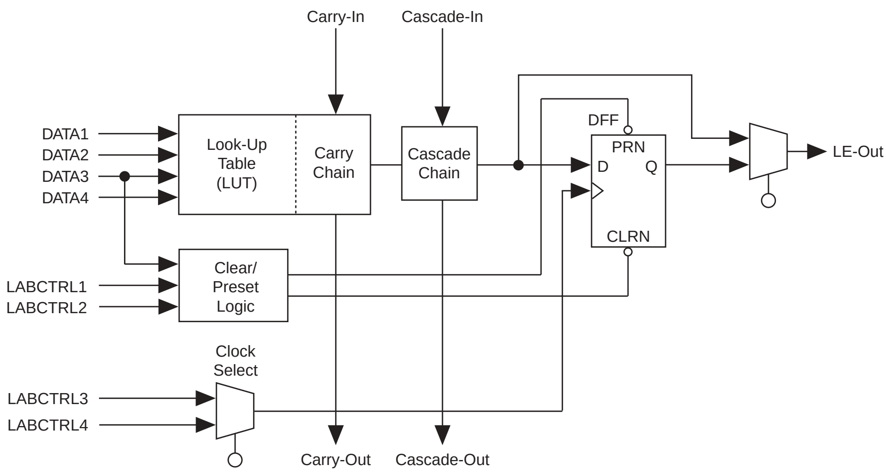


Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

## Logic Element

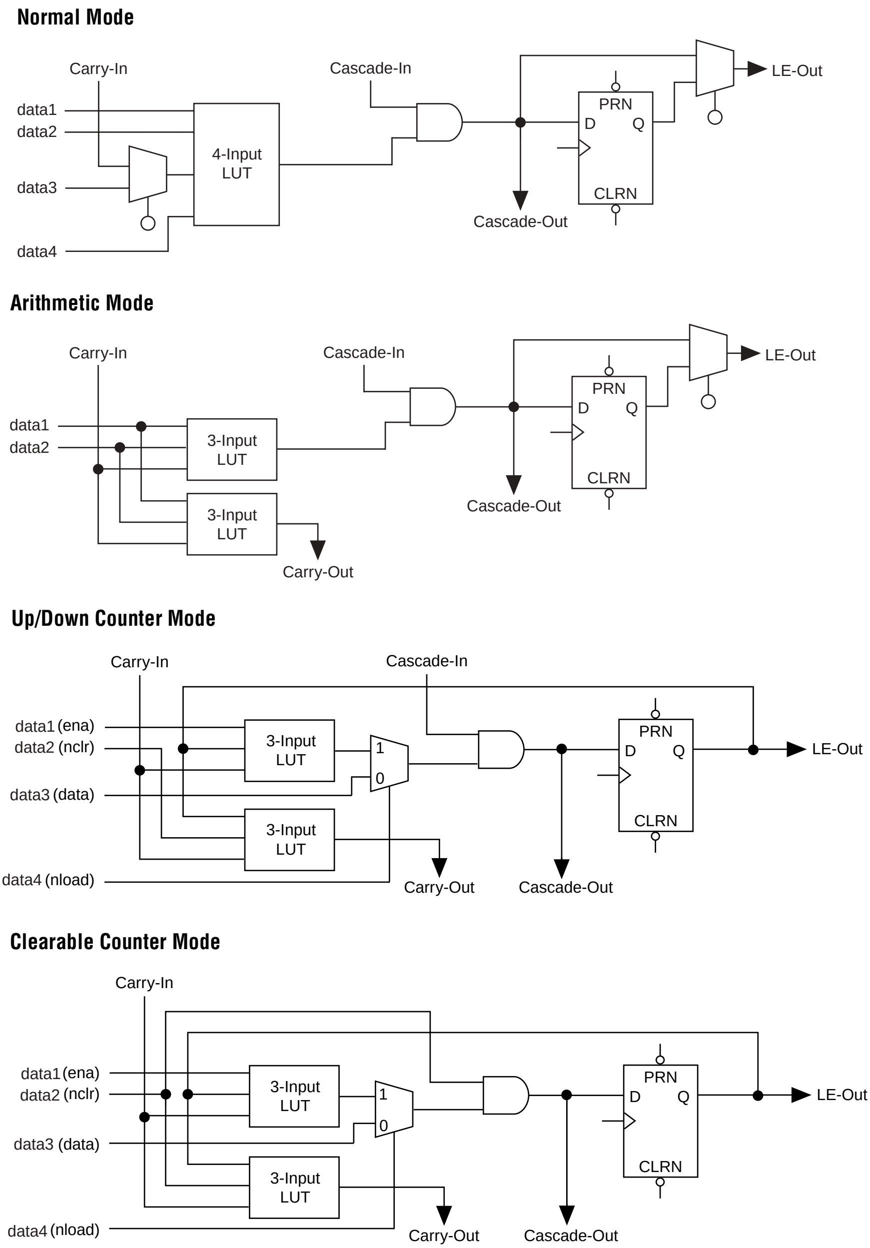
The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

*Figure 3. FLEX 8000 LE*




The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

*Figure 6. FLEX 8000 LE Operating Modes*



### Asynchronous Clear

A register is cleared by one of the two LABCTRL signals. When the CLRn port receives a low signal, the register is set to zero.

### Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load or an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRLl asynchronously loads a 1 into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### Asynchronous Clear & Preset

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. The DATA3 input is tied to VCC; therefore, asserting LABCTRL1 asynchronously loads a 1 into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### Asynchronous Load with Clear

When implementing an asynchronous load with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear.

### Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 clears the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives the DATA3 signal to account for the inversion of the register's output.

### Asynchronous Load without Clear or Preset

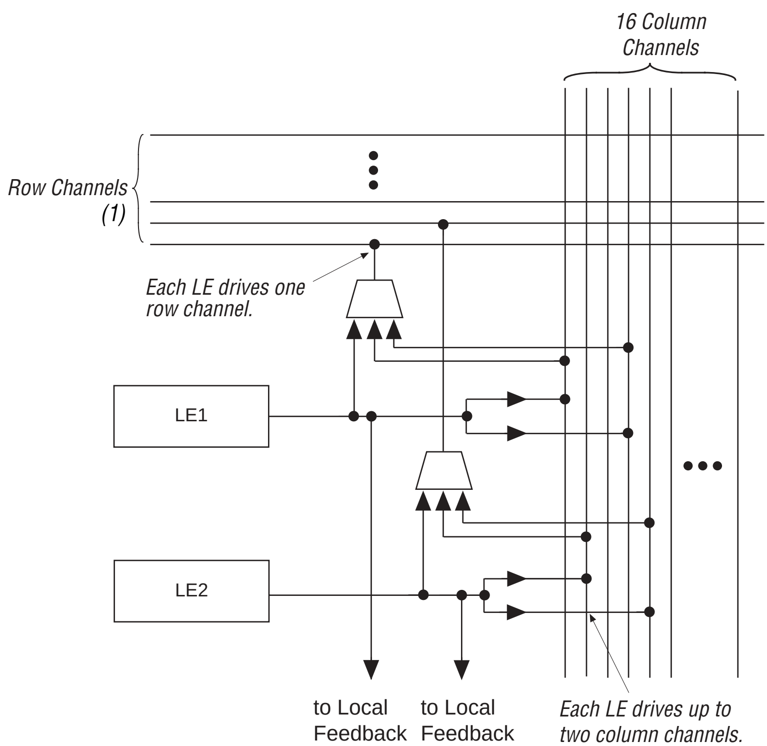
When implementing an asynchronous load without the clear or preset, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

## FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal (row) and vertical (column) routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing structure in FPGAs requires switch matrices to connect a variable number of routing paths, which increases the delays between logic resources and reduces performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Figure 8 shows how an LE drives the row and column interconnect.

*Figure 8. FLEX 8000 LAB Connections to Row & Column Interconnect*




***Note:***
(1) See Table 4 for the number of row channels.

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

***Table 4. FLEX 8000 FastTrack Interconnect Resources***

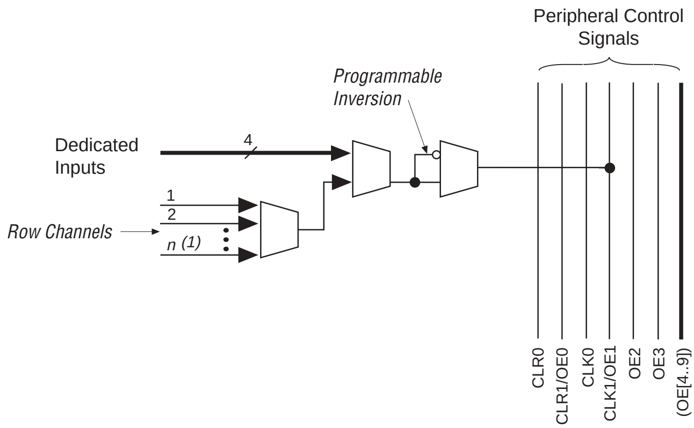
| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF8282A<br>EPF8282AV | 2 | 168 | 13 | 16 |
| EPF8452A | 2 | 168 | 21 | 16 |
| EPF8636A | 3 | 168 | 21 | 16 |
| EPF8820A | 4 | 168 | 21 | 16 |
| EPF81188A | 6 | 168 | 21 | 16 |
| EPF81500A | 6 | 216 | 27 | 16 |

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

***Figure 13. FLEX 8000 Peripheral Bus***

*Numbers in parentheses are for EPF81500A devices.*




***Note:***

(1) $n$ = 13 for EPF8282A and EPF8282AV devices.
$n$ = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
$n$ = 27 for EPF81500A devices.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

*Table 5. Row Sources of FLEX 8000 Peripheral Control Signals*

| Peripheral Control Signal | EPF8282A EPF8282AV | EPF8452A | EPF8636A | EPF8820A | EPF81188A | EPF81500A |
|---|---|---|---|---|---|---|
| CLK0 | Row A | Row A | Row A | Row A | Row E | Row E |
| CLK1/OE1 | Row B | Row B | Row C | Row C | Row B | Row B |
| CLR0 | Row A | Row A | Row B | Row B | Row F | Row F |
| CLR1/OE0 | Row B | Row B | Row C | Row D | Row C | Row C |
| OE2 | Row A | Row A | Row A | Row A | Row D | Row A |
| OE3 | Row B | Row B | Row B | Row B | Row A | Row A |
| OE4 | – | – | – | – | – | Row B |
| OE5 | – | – | – | – | – | Row C |
| OE6 | – | – | – | – | – | Row D |
| OE7 | – | – | – | – | – | Row D |
| OE8 | – | – | – | – | – | Row E |
| OE9 | – | – | – | – | – | Row F |

# Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

## Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

For more information on high-speed system design, go to *Application Note 75 (High-Speed Board Designs)*.

| *Table 10. FLEX 8000 5.0-V Device Recommended Operating Conditions* | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

| *Table 11. FLEX 8000 5.0-V Device DC Operating Conditions* *Notes (5), (6)* | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CCINT}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC *(7)* $V_{CCIO}$ = 4.75 V | 2.4 | | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC *(7)* $V_{CCIO}$ = 3.00 V | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC *(7)* $V_{CCIO}$ = 3.00 V | $V_{CCIO}$ – 0.2 | | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC *(7)* $V_{CCIO}$ = 4.75 V | | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC *(7)* $V_{CCIO}$ = 3.00 V | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC *(7)* $V_{CCIO}$ = 3.00 V | | | 0.2 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or ground | –10 | | 10 | $\mu A$ |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or ground | –40 | | 40 | $\mu A$ |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load | | 0.5 | 10 | mA |

**Table 15. FLEX 8000 3.3-V Device DC Operating Conditions** *Note (4)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –0.1 mA DC *(5)* | $V_{CC}$ – 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA DC *(5)* | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or ground | –10 | | 10 | μA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O = V_{CC}$ or ground | –40 | | 40 | μA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load *(6)* | | 0.3 | 10 | mA |

**Table 16. FLEX 8000 3.3-V Device Capacitance** *Note (7)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

***Notes to tables:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum $V_{CC}$ rise time is 100 ms. $V_{CC}$ must rise monotonically.
(4) These values are specified in Table 14 on page 29.
(5) The $I_{OH}$ parameter refers to high-level TTL output current; the $I_{OL}$ parameter refers to low-level TTL output current.
(6) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 3.3 V.
(7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

**Table 17. FLEX 8000 Internal Timing Parameters** *Note (1)*

| Symbol | Parameter |
|---|---|
| $t_{IOD}$ | IOE register data delay |
| $t_{IOC}$ | IOE register control signal delay |
| $t_{IOE}$ | Output enable delay |
| $t_{IOCO}$ | IOE register clock-to-output delay |
| $t_{IOCOMB}$ | IOE combinatorial delay |
| $t_{IOSU}$ | IOE register setup time before clock; IOE register recovery time after asynchronous clear |
| $t_{IOH}$ | IOE register hold time after clock |
| $t_{IOCLR}$ | IOE register clear delay |
| $t_{IN}$ | Input pad and buffer delay |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 5.0 V C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V C1 = 35 pF *(2)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)* |
| $t_{XZ}$ | Output buffer disable delay, C1 = 5 pF |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 5.0 V, C1 = 35 pF *(2)* |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V, C1 = 35 pF *(2)* |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)* |

**Table 18. FLEX 8000 LE Timing Parameters** *Note (1)*

| Symbol | Parameter |
|---|---|
| $t_{LUT}$ | LUT delay for data-in |
| $t_{CLUT}$ | LUT delay for carry-in |
| $t_{RLUT}$ | LUT delay for LE register feedback |
| $t_{GATE}$ | Cascade gate delay |
| $t_{CASC}$ | Cascade chain routing delay |
| $t_{CICO}$ | Carry-in to carry-out delay |
| $t_{CGEN}$ | Data-in to carry-out delay |
| $t_{CGENR}$ | LE register feedback to carry-out delay |
| $t_{C}$ | LE register control signal delay |
| $t_{CH}$ | LE register clock high time |
| $t_{CL}$ | LE register clock low time |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{COMB}$ | Combinatorial delay |
| $t_{SU}$ | LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load |
| $t_{H}$ | LE register hold time after clock |
| $t_{PRE}$ | LE register preset delay |
| $t_{CLR}$ | LE register clear delay |

| *Table 19. FLEX 8000 Interconnect Timing Parameters Note (1)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs |
| $t_{LOCAL}$ | LAB local interconnect delay |
| $t_{ROW}$ | Row interconnect routing delay *(4)* |
| $t_{COL}$ | Column interconnect routing delay |
| $t_{DIN\_C}$ | Dedicated input to LE control delay |
| $t_{DIN\_D}$ | Dedicated input to LE data delay *(4)* |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay |

| *Table 20. FLEX 8000 External Reference Timing Characteristics Note (5)* | |
|---|---|
| **Symbol** | **Parameter** |
| $\mathbf{t_{DRR}}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)* |
| $\mathbf{t_{ODH}}$ | Output data hold time after clock *(7)* |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the $t_{OD3}$ and $t_{ZX3}$ parameters, $V_{CCIO}$ = 3.3 V or 5.0 V.
(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

**Table 21. FLEX 8000 Timing Model Interconnect Paths**

| Source | Destination | Total Delay |
|---|---|---|
| LE-Out | LE in same LAB | $t_{LOCAL}$ |
| LE-Out | LE in same row, different LAB | $t_{ROW} + t_{LOCAL}$ |
| LE-Out | LE in different row | $t_{COL} + t_{ROW} + t_{LOCAL}$ |
| LE-Out | IOE on column | $t_{COL}$ |
| LE-Out | IOE on row | $t_{ROW}$ |
| IOE on row | LE in same row | $t_{ROW} + t_{LOCAL}$ |
| IOE on column | Any LE | $t_{COL} + t_{ROW} + t_{LOCAL}$ |

Tables 22 through 49 show the FLEX 8000 internal and external timing parameters.

**Table 22. EPF8282A Internal I/O Element Timing Parameters**

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | – | | – | | – | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | – | | – | | – | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

| *Table 23. EPF8282A Interconnect Timing Parameters* | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Speed Grade** | | | | | | **Unit** |
| | **A-2** | | **A-3** | | **A-4** | | |
| | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 4.2 | | 4.2 | | 4.2 | ns |
| $t_{COL}$ | | 2.5 | | 2.5 | | 2.5 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.2 | | 7.2 | | 7.2 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 42. EPF81188A I/O Element Timing Parameters*

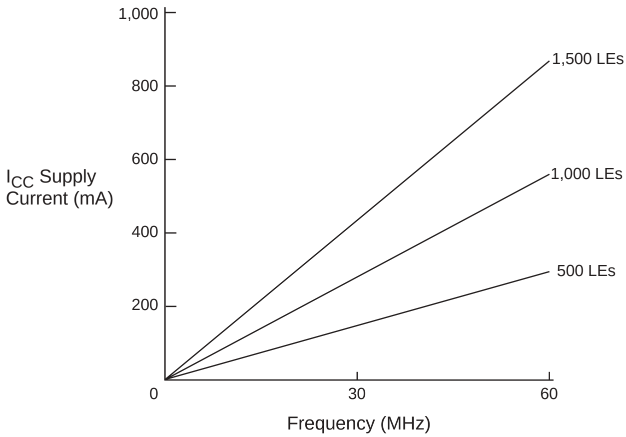
| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | 1.6 | | 1.9 | | 2.2 | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | 1.9 | | 2.1 | | 2.3 | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 43. EPF81188A Interconnect Timing Parameters*

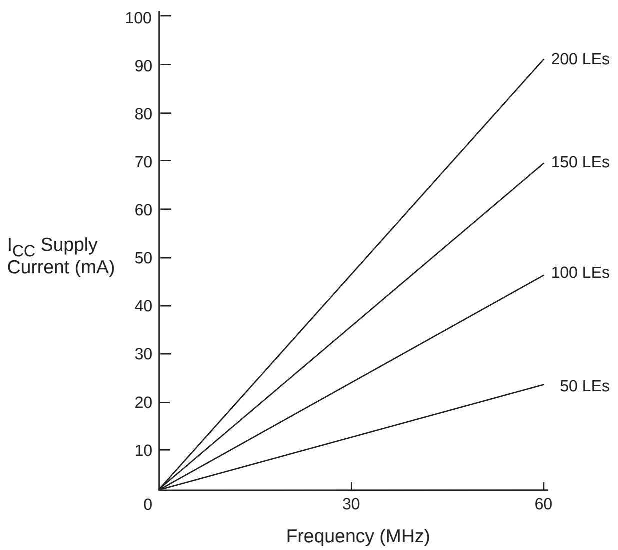
| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency*

**5.0-V FLEX 8000 Devices**




**3.3-V FLEX 8000 Devices**




## Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

## Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

*Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)*

| Pin Name | 84-Pin PLCC EPF8282A | 84-Pin PLCC EPF8452A EPF8636A | 100-Pin TQFP EPF8282A EPF8282AV | 100-Pin TQFP EPF8452A | 144-Pin TQFP EPF8820A | 160-Pin PGA EPF8452A | 160-Pin PQFP EPF8820A *(1)* |
|---|---|---|---|---|---|---|---|
| nSP *(2)* | 75 | 75 | 75 | 76 | 110 | R1 | 1 |
| MSEL0 *(2)* | 74 | 74 | 74 | 75 | 109 | P2 | 2 |
| MSEL1 *(2)* | 53 | 53 | 51 | 51 | 72 | A1 | 44 |
| nSTATUS *(2)* | 32 | 32 | 24 | 25 | 37 | C13 | 82 |
| nCONFIG *(2)* | 33 | 33 | 25 | 26 | 38 | A15 | 81 |
| DCLK *(2)* | 10 | 10 | 100 | 100 | 143 | P14 | 125 |
| CONF_DONE *(2)* | 11 | 11 | 1 | 1 | 144 | N13 | 124 |
| nWS | 30 | 30 | 22 | 23 | 33 | F13 | 87 |
| nRS | 48 | 48 | 42 | 45 | 31 | C6 | 89 |
| RDCLK | 49 | 49 | 45 | 46 | 12 | B5 | 110 |
| nCS | 29 | 29 | 21 | 22 | 4 | D15 | 118 |
| CS | 28 | 28 | 19 | 21 | 3 | E15 | 121 |
| RDYnBUSY | 77 | 77 | 77 | 78 | 20 | P3 | 100 |
| CLKUSR | 50 | 50 | 47 | 47 | 13 | C5 | 107 |
| ADD17 | 51 | 51 | 49 | 48 | 75 | B4 | 40 |
| ADD16 | 36 | 55 | 28 | 54 | 76 | E2 | 39 |
| ADD15 | 56 | 56 | 55 | 55 | 77 | D1 | 38 |
| ADD14 | 57 | 57 | 57 | 57 | 78 | E1 | 37 |
| ADD13 | 58 | 58 | 58 | 58 | 79 | F3 | 36 |
| ADD12 | 60 | 60 | 59 | 60 | 83 | F2 | 32 |
| ADD11 | 61 | 61 | 60 | 61 | 85 | F1 | 30 |
| ADD10 | 62 | 62 | 61 | 62 | 87 | G2 | 28 |
| ADD9 | 63 | 63 | 62 | 64 | 89 | G1 | 26 |
| ADD8 | 64 | 64 | 64 | 65 | 92 | H1 | 22 |
| ADD7 | 65 | 65 | 65 | 66 | 94 | H2 | 20 |
| ADD6 | 66 | 66 | 66 | 67 | 95 | J1 | 18 |
| ADD5 | 67 | 67 | 67 | 68 | 97 | J2 | 16 |
| ADD4 | 69 | 69 | 68 | 70 | 102 | K2 | 11 |
| ADD3 | 70 | 70 | 69 | 71 | 103 | K1 | 10 |
| ADD2 | 71 | 71 | 71 | 72 | 104 | K3 | 8 |
| ADD1 | 76 | 72 | 76 | 73 | 105 | M1 | 7 |

*Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)*

| Pin Name | 160-Pin PQFP EPF8452A | 160-Pin PQFP EPF8636A | 192-Pin PGA EPF8636A EPF8820A | 208-Pin PQFP EPF8636A *(1)* | 208-Pin PQFP EPF8820A *(1)* | 208-Pin PQFP EPF81188A *(1)* |
|---|---|---|---|---|---|---|
| nSP *(2)* | 120 | 1 | R15 | 207 | 207 | 5 |
| MSEL0 *(2)* | 117 | 3 | T15 | 4 | 4 | 21 |
| MSEL1 *(2)* | 84 | 38 | T3 | 49 | 49 | 33 |
| nSTATUS *(2)* | 37 | 83 | B3 | 108 | 108 | 124 |
| nCONFIG *(2)* | 40 | 81 | C3 | 103 | 103 | 107 |
| DCLK *(2)* | 1 | 120 | C15 | 158 | 158 | 154 |
| CONF_DONE *(2)* | 4 | 118 | B15 | 153 | 153 | 138 |
| nWS | 30 | 89 | C5 | 114 | 114 | 118 |
| nRS | 71 | 50 | B5 | 66 | 116 | 121 |
| RDCLK | 73 | 48 | C11 | 64 | 137 | 137 |
| nCS | 29 | 91 | B13 | 116 | 145 | 142 |
| CS | 27 | 93 | A16 | 118 | 148 | 144 |
| RDYnBUSY | 125 | 155 | A8 | 201 | 127 | 128 |
| CLKUSR | 76 | 44 | A10 | 59 | 134 | 134 |
| ADD17 | 78 | 43 | R5 | 57 | 43 | 46 |
| ADD16 | 91 | 33 | U3 | 43 | 42 | 45 |
| ADD15 | 92 | 31 | T5 | 41 | 41 | 44 |
| ADD14 | 94 | 29 | U4 | 39 | 40 | 39 |
| ADD13 | 95 | 27 | R6 | 37 | 39 | 37 |
| ADD12 | 96 | 24 | T6 | 31 | 35 | 36 |
| ADD11 | 97 | 23 | R7 | 30 | 33 | 31 |
| ADD10 | 98 | 22 | T7 | 29 | 31 | 30 |
| ADD9 | 99 | 21 | T8 | 28 | 29 | 29 |
| ADD8 | 101 | 20 | U9 | 24 | 25 | 26 |
| ADD7 | 102 | 19 | U10 | 23 | 23 | 25 |
| ADD6 | 103 | 18 | U11 | 22 | 21 | 24 |
| ADD5 | 104 | 17 | U12 | 21 | 19 | 18 |
| ADD4 | 105 | 13 | R12 | 14 | 14 | 17 |
| ADD3 | 106 | 11 | U14 | 12 | 13 | 16 |
| ADD2 | 109 | 9 | U15 | 10 | 11 | 10 |
| ADD1 | 110 | 7 | R13 | 8 | 10 | 9 |
| ADD0 | 123 | 157 | U16 | 203 | 9 | 8 |
| DATA7 | 144 | 137 | H17 | 178 | 178 | 177 |
| DATA6 | 150 | 132 | G17 | 172 | 176 | 175 |
| DATA5 | 152 | 129 | F17 | 169 | 174 | 172 |

| *Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 2 of 2)* | | | | | | |
|---|---|---|---|---|---|---|
| **Pin Name** | **160-Pin PQFP EPF8452A** | **160-Pin PQFP EPF8636A** | **192-Pin PGA EPF8636A EPF8820A** | **208-Pin PQFP EPF8636A** *(1)* | **208-Pin PQFP EPF8820A** *(1)* | **208-Pin PQFP EPF81188A** *(1)* |
| DATA4 | 154 | 127 | E17 | 165 | 172 | 170 |
| DATA3 | 157 | 124 | G15 | 162 | 171 | 168 |
| DATA2 | 159 | 122 | F15 | 160 | 167 | 166 |
| DATA1 | 11 | 115 | E16 | 149 | 165 | 163 |
| DATA0 | 12 | 113 | C16 | 147 | 162 | 161 |
| SDOUT *(3)* | 128 | 152 | C7 *(11)* | 198 | 124 | 119 |
| TDI *(4)* | – | 55 | R11 | 72 | 20 | – |
| TDO *(4)* | – | 95 | B9 | 120 | 129 | – |
| TCK *(4)*, *(6)* | – | 57 | U8 | 74 | 30 | – |
| TMS *(4)* | – | 59 | U7 | 76 | 32 | – |
| TRST *(7)* | – | 40 | R3 | 54 | 54 | – |
| Dedicated Inputs *(10)* | 5, 36, 85, 116 | 6, 35, 87, 116 | A5, U5, U13, A13 | 7, 45, 112, 150 | 17, 36, 121, 140 | 13, 41, 116, 146 |
| VCCINT (5.0 V) | 21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160 | 4, 5, 26, 85, 106 | C8, C9, C10, R8, R9, R10, R14 | 5, 6, 33, 110, 137 | 5, 6, 27, 48, 119, 141 | 4, 20, 35, 48, 50, 102, 114, 131, 147 |
| VCCIO (5.0 V or 3.3 V) | – | 25, 41, 60, 70, 80, 107, 121, 140, 149, 160 | D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14 | 32, 55, 78, 91, 102, 138, 159, 182, 193, 206 | 26, 55, 69, 87, 102, 131, 159, 173, 191, 206 | 3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192 |
| GND | 13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155 | 15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154 | C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11 | 19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200 | 15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200 | 11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201 |
| No Connect (N.C.) | 2, 3, 38, 39, 70, 82, 83, 118, 119, 148 | 2, 39, 82, 119 | C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4 *(12)* | 1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208 | 1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208 | 1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208 |
| Total User I/O Pins *(9)* | 116 | 114 | 132, 148 *(13)* | 132 | 148 | 144 |

*Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 225-Pin BGA EPF8820A | 232-Pin PGA EPF81188A | 240-Pin PQFP EPF81188A | 240-Pin PQFP EPF81500A | 280-Pin PGA EPF81500A | 304-Pin RQFP EPF81500A |
|---|---|---|---|---|---|---|
| DATA4 | A5 | C7 | 198 | 194 | W16 | 248 |
| DATA3 | B5 | D7 | 196 | 193 | W17 | 246 |
| DATA2 | E6 | B5 | 194 | 190 | V16 | 243 |
| DATA1 | D5 | A3 | 191 | 189 | U16 | 241 |
| DATA0 | C4 | A2 | 189 | 187 | V17 | 239 |
| SDOUT *(3)* | K1 | N2 | 135 | 136 | F19 | 169 |
| TDI | F15 *(4)* | – | – | 63 *(14)* | B1 *(14)* | 80 *(14)* |
| TDO | J2 *(4)* | – | – | 117 | C17 | 149 |
| TCK *(6)* | J14 *(4)* | – | – | 116 *(14)* | A19 *(14)* | 148 *(14)* |
| TMS | J12 *(4)* | – | – | 64 *(14)* | C2 *(14)* | 81 *(14)* |
| TRST *(7)* | P14 | – | – | 115 *(14)* | A18 *(14)* | 145 *(14)* |
| Dedicated Inputs *(10)* | F4, L1, K12, E15 | C1, C17, R1, R17 | 10, 51, 130, 171 | 8, 49, 131, 172 | F1, F16, P3, P19 | 12, 64, 164, 217 |
| VCCINT (5.0 V) | F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13 | E4, H4, L4, P12, L14, H14, E14, R14, U1 | 20, 42, 64, 66, 114, 128, 150, 172, 236 | 18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236 | B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14 | 24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301 |
| VCCIO (5.0 V or 3.3 V) | H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2 | N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13 | 19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235 | 17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235 | D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15 | 22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300 |