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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 63 |
| Number of Logic Elements/Cells | 504 |
| Total RAM Bits | - |
| Number of I/O | 68 |
| Number of Gates | 6000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epf8636ali84-4 |

| | | | | | | |
|---|---|---|---|---|---|---|
| JTAG BST circuitry | Yes | No | Yes | Yes | No | Yes |

## ...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

*Table 2. FLEX 8000 Package Options & I/O Pin Count* *Note (1)*

| Device | 84-Pin PLCC | 100-Pin TQFP | 144-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 225-Pin BGA | 232-Pin PGA | 240-Pin PQFP | 280-Pin PGA | 304-Pin RQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPF8282A | 68 | 78 | | | | | | | | | | |
| EPF8282AV | | 78 | | | | | | | | | | |
| EPF8452A | 68 | 68 | | 120 | 120 | | | | | | | |
| EPF8636A | 68 | | | 118 | | 136 | 136 | | | | | |
| EPF8820A | | | 112 | 120 | | 152 | 152 | 152 | | | | |
| EPF81188A | | | | | | | 148 | | 184 | 184 | | |
| EPF81500A | | | | | | | | | | 181 | 208 | 208 |

*Note:*
(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

## General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 8000 architecture.

For more information on the MAX+PLUS II software, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

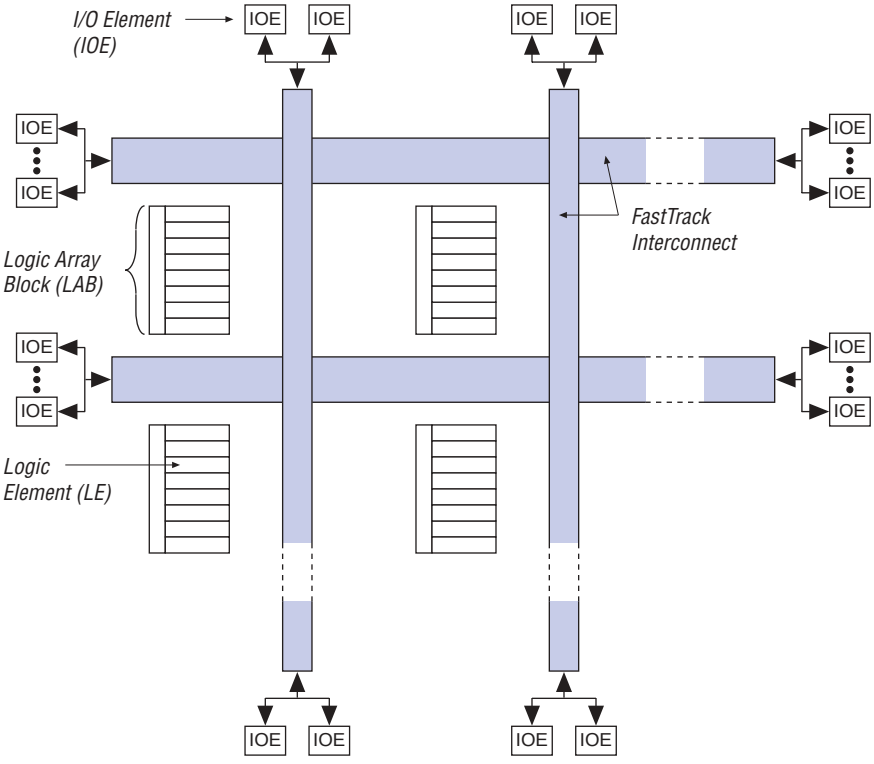
## Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

***Figure 1. FLEX 8000 Device Block Diagram***




Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in signal are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-Out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data output (Q) of the programmable register.

### Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 6, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three bits: a, b, and the carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports a cascade chain.

### Up/Down Counter Mode

The up/down counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control; the clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, and the output of this multiplexer is ANDed with a synchronous clear.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

### Asynchronous Clear

A register is cleared by one of the two LABCTRL signals. When the CLRn port receives a low signal, the register is set to zero.

### Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load or an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRL1 asynchronously loads a 1 into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

### Asynchronous Clear & Preset

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. The DATA3 input is tied to VCC; therefore, asserting LABCTRL1 asynchronously loads a 1 into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

### Asynchronous Load with Clear

When implementing an asynchronous load with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear.

### Asynchronous Load with Preset

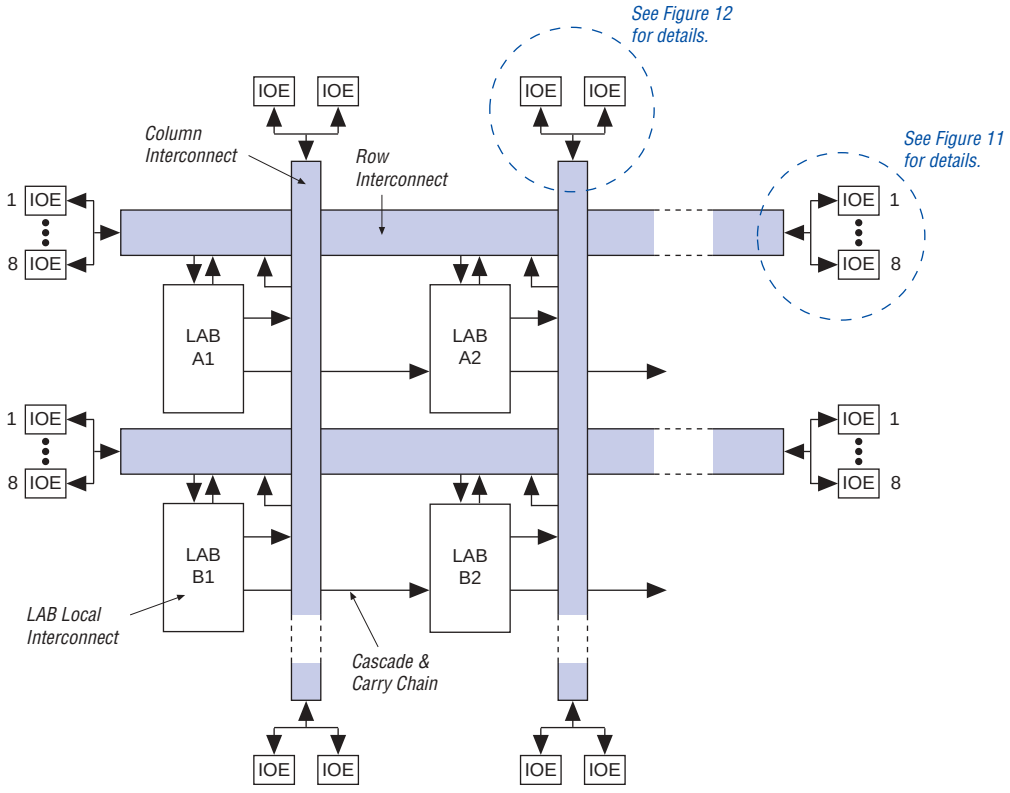
When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 clears the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives the DATA3 signal to account for the inversion of the register's output.

### Asynchronous Load without Clear or Preset

When implementing an asynchronous load without the clear or preset, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

***Figure 9. FLEX 8000 Device Interconnect Resources***

*Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.*




## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 10 shows the IOE block diagram.

### MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$. See Table 8 on page 26.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in Table 6.

*Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. |

*Table 8. JTAG Timing Parameters & Values*

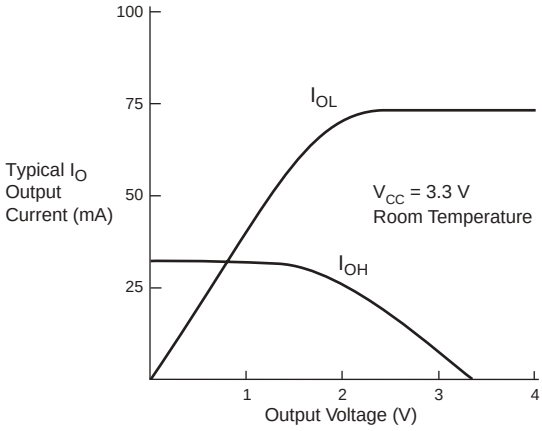
| Symbol | Parameter | EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high-impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high-impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high-impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high-impedance | | 35 | ns |

For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Designers can use multiple test patterns to configure devices during all stages of the production flow.

*Figure 18. Output Drive Characteristics of EPF8282AV Devices*




## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

| Table 17. FLEX 8000 Internal Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{IOD}$ | IOE register data delay |
| $t_{IOC}$ | IOE register control signal delay |
| $t_{IOE}$ | Output enable delay |
| $t_{IOCO}$ | IOE register clock-to-output delay |
| $t_{IOCOMB}$ | IOE combinatorial delay |
| $t_{IOSU}$ | IOE register setup time before clock; IOE register recovery time after asynchronous clear |
| $t_{IOH}$ | IOE register hold time after clock |
| $t_{IOCLR}$ | IOE register clear delay |
| $t_{IN}$ | Input pad and buffer delay |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 5.0 V C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V C1 = 35 pF *(2)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)* |
| $t_{XZ}$ | Output buffer disable delay, C1 = 5 pF |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 5.0 V, C1 = 35 pF *(2)* |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V, C1 = 35 pF *(2)* |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)* |

| Table 18. FLEX 8000 LE Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{CLUT}$ | LUT delay for carry-in |
| $t_{RLUT}$ | LUT delay for LE register feedback |
| $t_{GATE}$ | Cascade gate delay |
| $t_{CASC}$ | Cascade chain routing delay |
| $t_{CICO}$ | Carry-in to carry-out delay |
| $t_{CGEN}$ | Data-in to carry-out delay |
| $t_{CGENR}$ | LE register feedback to carry-out delay |
| $t_{C}$ | LE register control signal delay |
| $t_{CH}$ | LE register clock high time |
| $t_{CL}$ | LE register clock low time |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{COMB}$ | Combinatorial delay |
| $t_{SU}$ | LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load |
| $t_{H}$ | LE register hold time after clock |
| $t_{PRE}$ | LE register preset delay |
| $t_{CLR}$ | LE register clear delay |

| Table 19. FLEX 8000 Interconnect Timing Parameters Note (1) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs |
| $t_{LOCAL}$ | LAB local interconnect delay |
| $t_{ROW}$ | Row interconnect routing delay *(4)* |
| $t_{COL}$ | Column interconnect routing delay |
| $t_{DIN\_C}$ | Dedicated input to LE control delay |
| $t_{DIN\_D}$ | Dedicated input to LE data delay *(4)* |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay |

| Table 20. FLEX 8000 External Reference Timing Characteristics Note (5) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)* |
| $t_{ODH}$ | Output data hold time after clock *(7)* |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the $t_{OD3}$ and $t_{ZX3}$ parameters, $V_{CCIO}$ = 3.3 V or 5.0 V.
(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

*Table 23. EPF8282A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 4.2 | | 4.2 | | 4.2 | ns |
| $t_{COL}$ | | 2.5 | | 2.5 | | 2.5 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.2 | | 7.2 | | 7.2 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 24. EPF8282A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 25. EPF8282A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 15.8 | | 19.8 | | 24.8 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 34. EPF8636A I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | 1.6 | | 1.9 | | 2.2 | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | 1.9 | | 2.1 | | 2.3 | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 35. EPF8636A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.4 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.5 | | 0.7 | ns |
| $t_{ROW}$ | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 36. EPF8636A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.3 | | 3.0 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.2 | | 0.1 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.6 | | 1.6 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.9 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.4 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.0 | | 1.1 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.4 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 37. EPF8636A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.0 | | 20.0 | | 25.0 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 42. EPF81188A I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | 1.6 | | 1.9 | | 2.2 | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | 1.9 | | 2.1 | | 2.3 | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 43. EPF81188A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

## Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

*Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)*

| Pin Name | 84-Pin PLCC EPF8282A | 84-Pin PLCC EPF8452A EPF8636A | 100-Pin TQFP EPF8282A EPF8282AV | 100-Pin TQFP EPF8452A | 144-Pin TQFP EPF8820A | 160-Pin PGA EPF8452A | 160-Pin PQFP EPF8820A *(1)* |
|---|---|---|---|---|---|---|---|
| nSP *(2)* | 75 | 75 | 75 | 76 | 110 | R1 | 1 |
| MSEL0 *(2)* | 74 | 74 | 74 | 75 | 109 | P2 | 2 |
| MSEL1 *(2)* | 53 | 53 | 51 | 51 | 72 | A1 | 44 |
| nSTATUS *(2)* | 32 | 32 | 24 | 25 | 37 | C13 | 82 |
| nCONFIG *(2)* | 33 | 33 | 25 | 26 | 38 | A15 | 81 |
| DCLK *(2)* | 10 | 10 | 100 | 100 | 143 | P14 | 125 |
| CONF_DONE *(2)* | 11 | 11 | 1 | 1 | 144 | N13 | 124 |
| nWS | 30 | 30 | 22 | 23 | 33 | F13 | 87 |
| nRS | 48 | 48 | 42 | 45 | 31 | C6 | 89 |
| RDCLK | 49 | 49 | 45 | 46 | 12 | B5 | 110 |
| nCS | 29 | 29 | 21 | 22 | 4 | D15 | 118 |
| CS | 28 | 28 | 19 | 21 | 3 | E15 | 121 |
| RDYnBUSY | 77 | 77 | 77 | 78 | 20 | P3 | 100 |
| CLKUSR | 50 | 50 | 47 | 47 | 13 | C5 | 107 |
| ADD17 | 51 | 51 | 49 | 48 | 75 | B4 | 40 |
| ADD16 | 36 | 55 | 28 | 54 | 76 | E2 | 39 |
| ADD15 | 56 | 56 | 55 | 55 | 77 | D1 | 38 |
| ADD14 | 57 | 57 | 57 | 57 | 78 | E1 | 37 |
| ADD13 | 58 | 58 | 58 | 58 | 79 | F3 | 36 |
| ADD12 | 60 | 60 | 59 | 60 | 83 | F2 | 32 |
| ADD11 | 61 | 61 | 60 | 61 | 85 | F1 | 30 |
| ADD10 | 62 | 62 | 61 | 62 | 87 | G2 | 28 |
| ADD9 | 63 | 63 | 62 | 64 | 89 | G1 | 26 |
| ADD8 | 64 | 64 | 64 | 65 | 92 | H1 | 22 |
| ADD7 | 65 | 65 | 65 | 66 | 94 | H2 | 20 |
| ADD6 | 66 | 66 | 66 | 67 | 95 | J1 | 18 |
| ADD5 | 67 | 67 | 67 | 68 | 97 | J2 | 16 |
| ADD4 | 69 | 69 | 68 | 70 | 102 | K2 | 11 |
| ADD3 | 70 | 70 | 69 | 71 | 103 | K1 | 10 |
| ADD2 | 71 | 71 | 71 | 72 | 104 | K3 | 8 |
| ADD1 | 76 | 72 | 76 | 73 | 105 | M1 | 7 |

*Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)*

| Pin Name | 225-Pin BGA EPF8820A | 232-Pin PGA EPF81188A | 240-Pin PQFP EPF81188A | 240-Pin PQFP EPF81500A | 280-Pin PGA EPF81500A | 304-Pin RQFP EPF81500A |
|---|---|---|---|---|---|---|
| GND | B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1 | A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14 | 8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229 | 6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228 | D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17 | 9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291 |
| No Connect (N.C.) | – | – | 61, 62, 119, 120, 181, 182, 239, 240 | – | – | 10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303 |
| Total User I/O Pins *(9)* | 148 | 180 | 180 | 177 | 204 | 204 |

*Notes to tables:*

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a $V_{CC}$ pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) SDOUT does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

## Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.