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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	63
Number of Logic Elements/Cells	504
Total RAM Bits	-
Number of I/O	118
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf8636aqc160-3">https://www.e-xfl.com/product-detail/intel/epf8636aqc160-3</a>

### Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in signal are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-Out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data output (Q) of the programmable register.

### Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 6, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three bits: a, b, and the carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports a cascade chain.

### Up/Down Counter Mode

The up/down counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

### Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control; the clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, and the output of this multiplexer is ANDed with a synchronous clear.

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

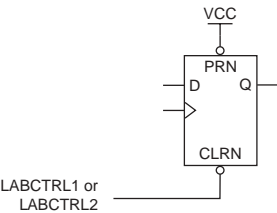
During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See [Figure 7](#).

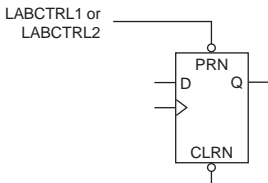
- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes

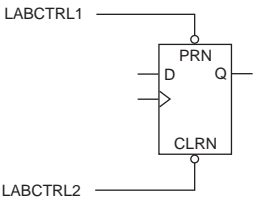
Asynchronous Clear



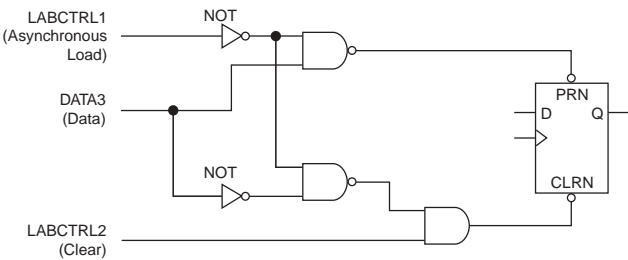
Asynchronous Preset



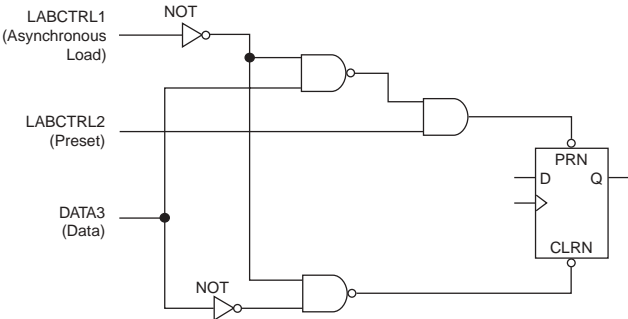
Asynchronous Clear & Preset



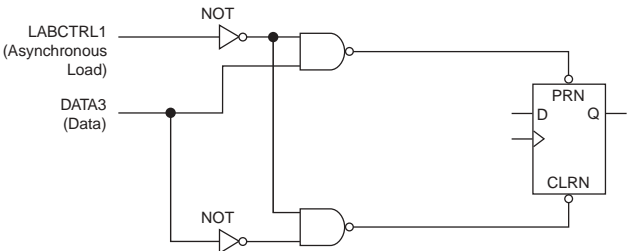
Asynchronous Load with Clear



Asynchronous Load with Preset



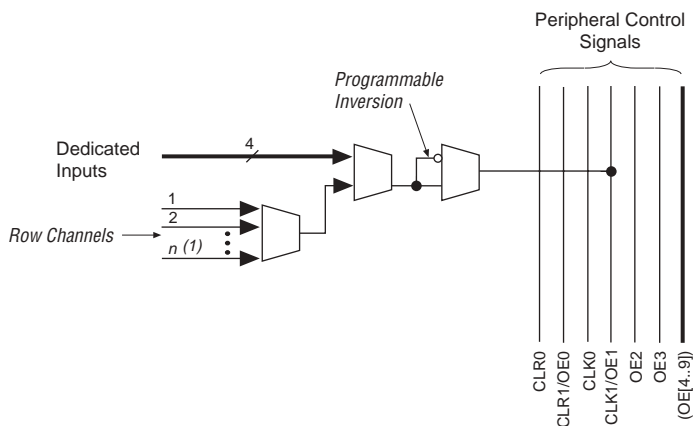
Asynchronous Load without Clear or Preset



The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

**Figure 13. FLEX 8000 Peripheral Bus**

*Numbers in parentheses are for EPF81500A devices.*



**Note:**

- (1)  $n = 13$  for EPF8282A and EPF8282AV devices.
- $n = 21$  for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
- $n = 27$  for EPF81500A devices.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

<b>Table 5. Row Sources of FLEX 8000 Peripheral Control Signals</b>						
<b>Peripheral Control Signal</b>	<b>EPF8282A EPF8282AV</b>	<b>EPF8452A</b>	<b>EPF8636A</b>	<b>EPF8820A</b>	<b>EPF81188A</b>	<b>EPF81500A</b>
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	—	—	—	—	—	Row B
OE5	—	—	—	—	—	Row C
OE6	—	—	—	—	—	Row D
OE7	—	—	—	—	—	Row D
OE8	—	—	—	—	—	Row E
OE9	—	—	—	—	—	Row F

## Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

### Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.



For more information on high-speed system design, go to [Application Note 75 \(High-Speed Board Designs\)](#).

## MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of  $V_{CC}$  pins for internal operation and input buffers ( $V_{CCINT}$ ), and another set for I/O output drivers ( $V_{CCIO}$ ).

The  $V_{CCINT}$  pins must always be connected to a 5.0-V power supply. With a 5.0-V  $V_{CCINT}$  level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The  $V_{CCIO}$  pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the  $V_{CCIO}$  pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the  $V_{CCIO}$  pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with  $V_{CCIO}$  levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ . See [Table 8 on page 26](#).

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in [Table 6](#).

**Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions**

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the $TDI$ and $TDO$ pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

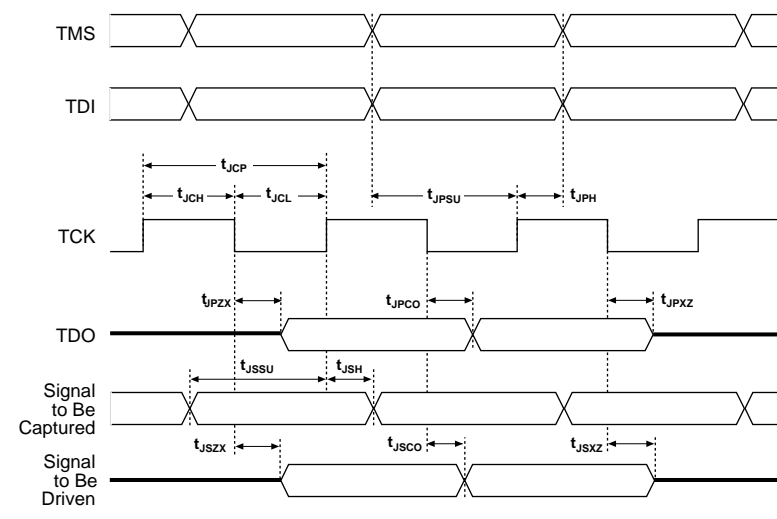
The instruction register length for FLEX 8000 devices is three bits. [Table 7](#) shows the boundary-scan register length for FLEX 8000 devices.

**Table 7. FLEX 8000 Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPF8282A, EPF8282AV	273
EPF8636A	417
EPF8820A	465
EPF81500A	645

FLEX 8000 devices that support JTAG include weak pull-ups on the JTAG pins. [Figure 14](#) shows the timing requirements for the JTAG signals.

**Figure 14. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Waveforms**



[Table 8](#) shows the timing parameters and values for EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices.



**Table 8. JTAG Timing Parameters & Values**

Symbol	Parameter	EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A		Unit
		Min	Max	
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high-impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high-impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		35	ns
$t_{JSZX}$	Update register high-impedance to valid output		35	ns
$t_{JSXZ}$	Update register valid output to high-impedance		35	ns



For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in *Figure 15*. Designers can use multiple test patterns to configure devices during all stages of the production flow.

**Table 12. FLEX 8000 5.0-V Device Capacitance** *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C <sub>IN</sub>	Input capacitance	V <sub>IN</sub> = 0 V, f = 1.0 MHz		10	pF
C <sub>OUT</sub>	Output capacitance	V <sub>OUT</sub> = 0 V, f = 1.0 MHz		10	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) The maximum V<sub>CC</sub> rise time is 100 ms.
- (4) Numbers in parentheses are for industrial-temperature-range devices.
- (5) Typical values are for T<sub>A</sub> = 25° C and V<sub>CC</sub> = 5.0 V.
- (6) These values are specified in Table 10 on page 28.
- (7) The I<sub>OH</sub> parameter refers to high-level TTL or CMOS output current; the I<sub>OL</sub> parameter refers to low-level TTL or CMOS output current.
- (8) Capacitance is sample-tested only.

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 3.3-V FLEX 8000 devices.

**Table 13. FLEX 8000 3.3-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply voltage	With respect to ground (2)	-2.0	5.3	V
V <sub>I</sub>	DC input voltage		-2.0	5.3	V
I <sub>OUT</sub>	DC output current, per pin		-25	25	mA
T <sub>STG</sub>	Storage temperature	No bias	-65	150	° C
T <sub>AMB</sub>	Ambient temperature	Under bias	-65	135	° C
T <sub>J</sub>	Junction temperature	Plastic packages, under bias		135	° C

**Table 14. FLEX 8000 3.3-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply voltage	(3)	3.0	3.6	V
V <sub>I</sub>	Input voltage		-0.3	V <sub>CC</sub> + 0.3	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating temperature	For commercial use	0	70	° C
t <sub>R</sub>	Input rise time			40	ns
t <sub>F</sub>	Input fall time			40	ns

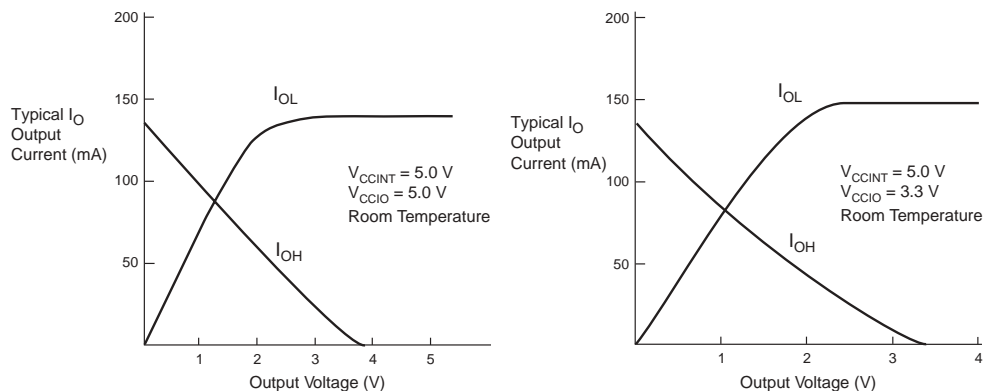
**Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)**

Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

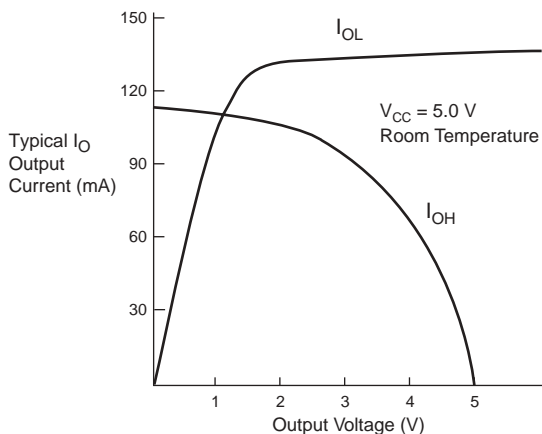
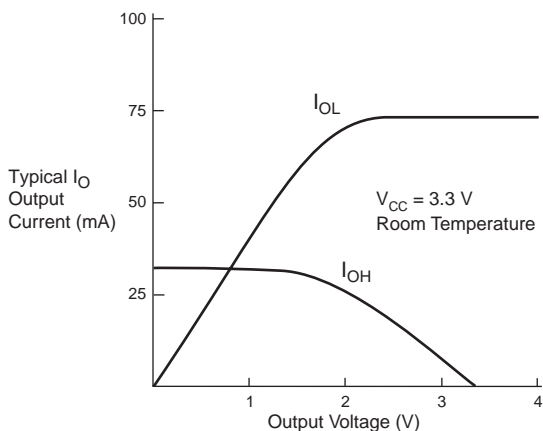
**Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V  $V_{CCIO}$** 

Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

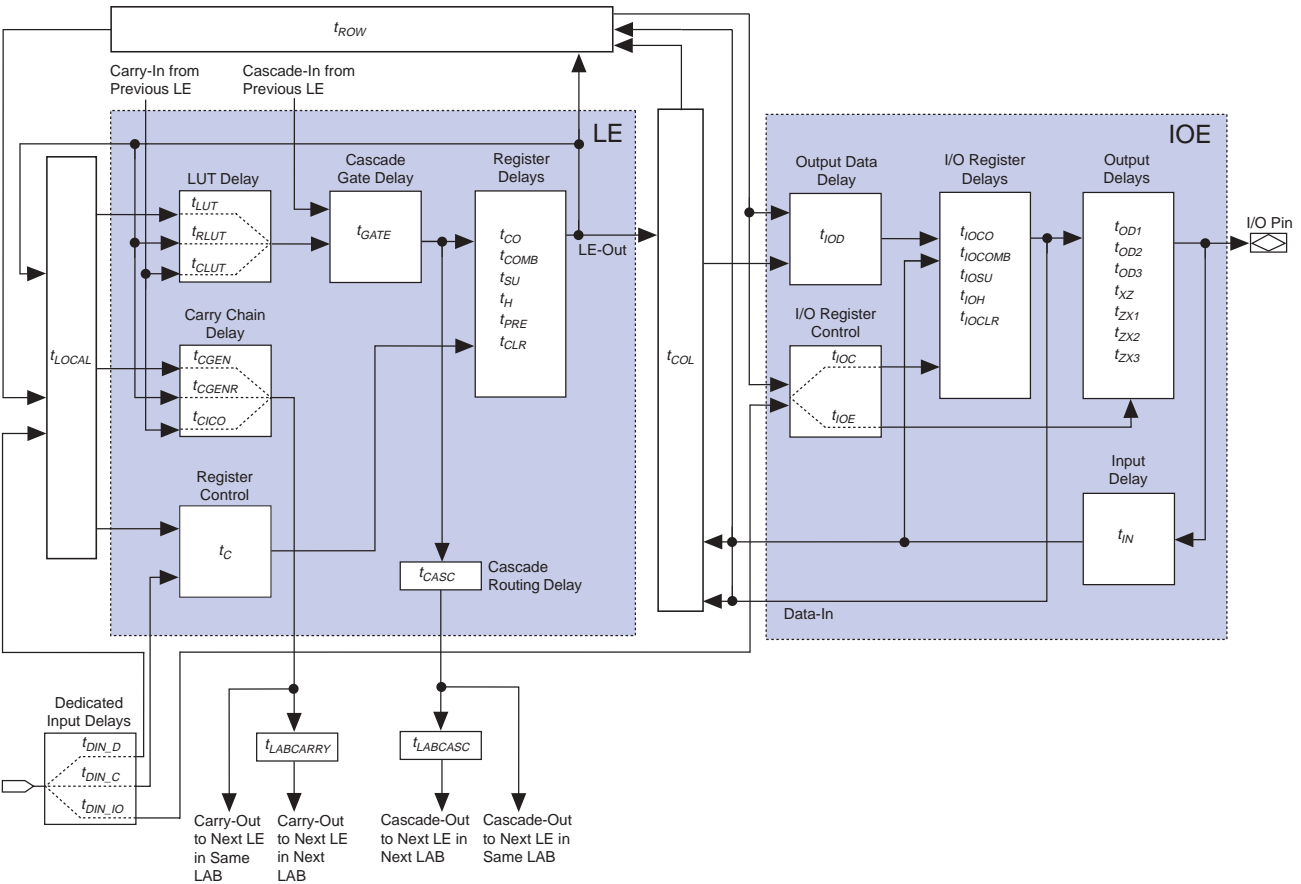
**Figure 18. Output Drive Characteristics of EPF8282AV Devices**

## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

Figure 19. FLEX 8000 Timing Model



**Table 23. EPF8282A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
$t_{LOCAL}$		0.5		0.6		0.8	ns
$t_{ROW}$		4.2		4.2		4.2	ns
$t_{COL}$		2.5		2.5		2.5	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		7.2		7.2		7.2	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns

**Table 30. EPF8452A I/O Element Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		0.7		0.8		0.9	ns
$t_{IOC}$		1.7		1.8		1.9	ns
$t_{IOE}$		1.7		1.8		1.9	ns
$t_{IOCO}$		1.0		1.0		1.0	ns
$t_{IOCOMB}$		0.3		0.2		0.1	ns
$t_{IOSU}$	1.4		1.6		1.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.2		1.2		1.2	ns
$t_{IN}$		1.5		1.6		1.7	ns
$t_{OD1}$		1.1		1.4		1.7	ns
$t_{OD2}$		—		—		—	ns
$t_{OD3}$		4.6		4.9		5.2	ns
$t_{XZ}$		1.4		1.6		1.8	ns
$t_{ZX1}$		1.4		1.6		1.8	ns
$t_{ZX2}$		—		—		—	ns
$t_{ZX3}$		4.9		5.1		5.3	ns

**Table 31. EPF8452A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
$t_{LOCAL}$		0.5		0.5		0.7	ns
$t_{ROW}$		5.0		5.0		5.0	ns
$t_{COL}$		3.0		3.0		3.0	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		7.0		7.0		7.5	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns

**Table 34. EPF8636A I/O Element Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		0.7		0.8		0.9	ns
$t_{IOC}$		1.7		1.8		1.9	ns
$t_{IOE}$		1.7		1.8		1.9	ns
$t_{IOCO}$		1.0		1.0		1.0	ns
$t_{IOCOMB}$		0.3		0.2		0.1	ns
$t_{IOSU}$	1.4		1.6		1.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.2		1.2		1.2	ns
$t_{IN}$		1.5		1.6		1.7	ns
$t_{OD1}$		1.1		1.4		1.7	ns
$t_{OD2}$		1.6		1.9		2.2	ns
$t_{OD3}$		4.6		4.9		5.2	ns
$t_{XZ}$		1.4		1.6		1.8	ns
$t_{ZX1}$		1.4		1.6		1.8	ns
$t_{ZX2}$		1.9		2.1		2.3	ns
$t_{ZX3}$		4.9		5.1		5.3	ns

**Table 35. EPF8636A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
$t_{LOCAL}$		0.5		0.5		0.7	ns
$t_{ROW}$		5.0		5.0		5.0	ns
$t_{COL}$		3.0		3.0		3.0	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		7.0		7.0		7.5	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns



**Table 48. EPF81500A LE Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LUT}$		2.0		2.5		3.2	ns
$t_{CLUT}$		0.0		0.0		0.0	ns
$t_{RLUT}$		0.9		1.1		1.5	ns
$t_{GATE}$		0.0		0.0		0.0	ns
$t_{CASC}$		0.6		0.7		0.9	ns
$t_{CICO}$		0.4		0.5		0.6	ns
$t_{CGEN}$		0.4		0.5		0.7	ns
$t_{CGENR}$		0.9		1.1		1.5	ns
$t_C$		1.6		2.0		2.5	ns
$t_{CH}$	4.0		4.0		4.0		ns
$t_{CL}$	4.0		4.0		4.0		ns
$t_{CO}$		0.4		0.5		0.6	ns
$t_{COMB}$		0.4		0.5		0.6	ns
$t_{SU}$	0.8		1.1		1.2		ns
$t_H$	0.9		1.1		1.5		ns
$t_{PRE}$		0.6		0.7		0.8	ns
$t_{CLR}$		0.6		0.7		0.8	ns

**Table 49. EPF81500A External Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t <sub>DRR</sub>		16.1		20.1		25.1	ns
t <sub>ODH</sub>	1.0		1.0		1.0		ns

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)**

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
ADD0	78	76	78	77	106	N3	6
DATA7	3	2	90	89	131	P8	140
DATA6	4	4	91	91	132	P10	139
DATA5	6	6	92	95	133	R12	138
DATA4	7	7	95	96	134	R13	136
DATA3	8	8	97	97	135	P13	135
DATA2	9	9	99	98	137	R14	133
DATA1	13	13	4	4	138	N15	132
DATA0	14	14	5	5	140	K13	129
SDOUT (3)	79	78	79	79	23	P4	97
TDI (4)	55	45 (5)	54	—	96	—	17
TDO (4)	27	27 (5)	18	—	18	—	102
TCK (4), (6)	72	44 (5)	72	—	88	—	27
TMS (4)	20	43 (5)	11	—	86	—	29
TRST (7)	52	52 (8)	50	—	71	—	45
Dedicated Inputs (10)	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
VCCIO	—	—	—	—	16, 40, 60, 69, 91, 112, 122, 141	—	23, 47, 57, 69, 79, 104, 127, 137, 149, 159

**Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)**

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A (1)	208-Pin PQFP EPF8820A (1)	208-Pin PQFP EPF8188A (1)
nSP (2)	120	1	R15	207	207	5
MSEL0 (2)	117	3	T15	4	4	21
MSEL1 (2)	84	38	T3	49	49	33
nSTATUS (2)	37	83	B3	108	108	124
nCONFIG (2)	40	81	C3	103	103	107
DCLK (2)	1	120	C15	158	158	154
CONF_DONE (2)	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

**Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)**

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP (2)	A15	C14	237	237	W1	304
MSEL0 (2)	B14	G15	21	19	N1	26
MSEL1 (2)	R15	L15	40	38	H3	51
nSTATUS (2)	P2	L3	141	142	G19	178
nCONFIG (2)	R1	R4	117	120	B18	152
DCLK (2)	B2	C4	184	183	U18	230
CONF_DONE (2)	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDynBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

### Notes to tables:

- (1) Perform a complete thermal analysis before committing a design to this device package. See [Application Note 74 \(Evaluating Power for Altera Devices\)](#) for more information.
- (2) This pin is a dedicated pin and is not available as a user I/O pin.
- (3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
- (4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
- (5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
- (6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
- (7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
- (8) Pin 52 is a  $V_{CC}$  pin on EPF8452A devices only.
- (9) The user I/O pin count includes dedicated input pins and all I/O pins.
- (10) Unused dedicated inputs should be tied to ground on the board.
- (11) SDOUT does not exist in the EPF8636GC192 device.
- (12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
- (13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
- (14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

## Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.