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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	63
Number of Logic Elements/Cells	504
Total RAM Bits	-
Number of I/O	118
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epf8636aqc160-4">https://www.e-xfl.com/product-detail/intel/epf8636aqc160-4</a>

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes
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## ...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see [Table 2](#))
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

**Table 2. FLEX 8000 Package Options & I/O Pin Count** *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

**Note:**

- (1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

## General Description

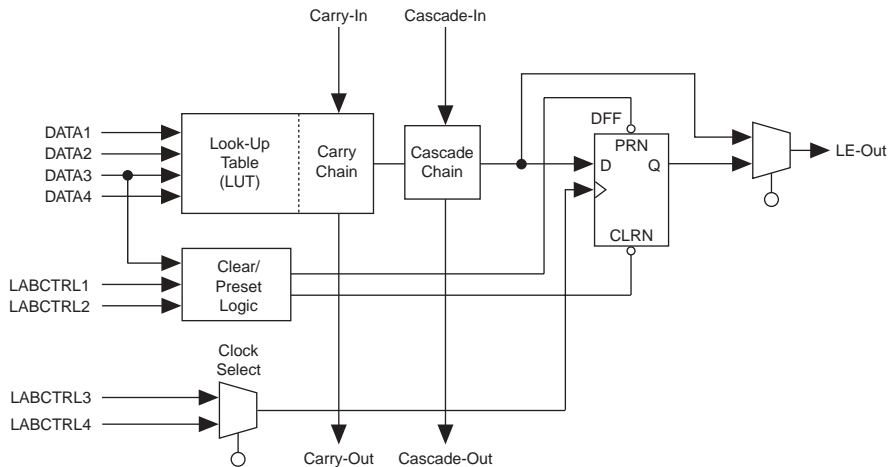
Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

## Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

**Figure 3. FLEX 8000 LE**



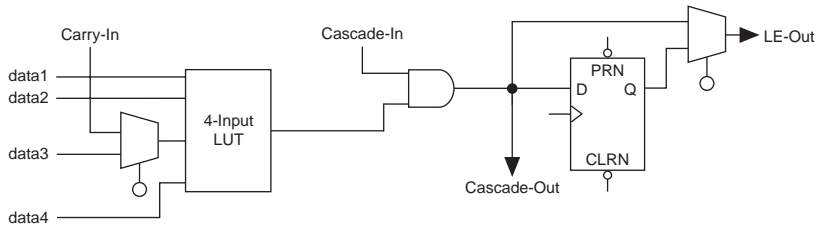
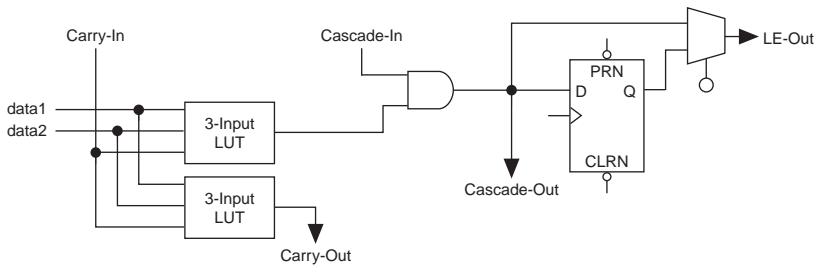
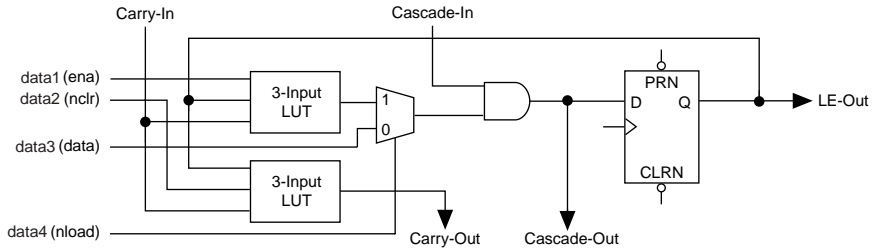
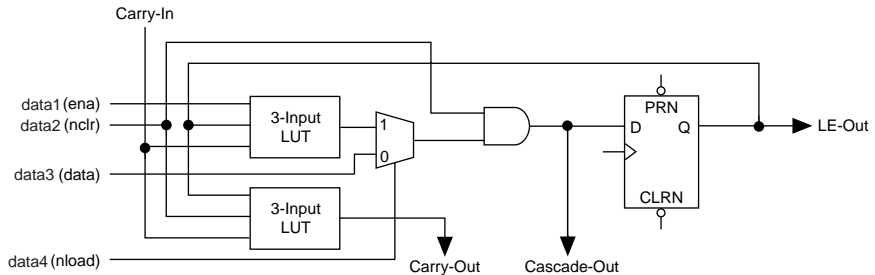
The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinational functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce routing flexibility. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

### *Carry Chain*

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 4 shows how an  $n$ -bit full adder can be implemented in  $n + 1$  LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to another LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

**Figure 6. FLEX 8000 LE Operating Modes****Normal Mode****Arithmetic Mode****Up/Down Counter Mode****Clearable Counter Mode**

### *Internal Tri-State Emulation*

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

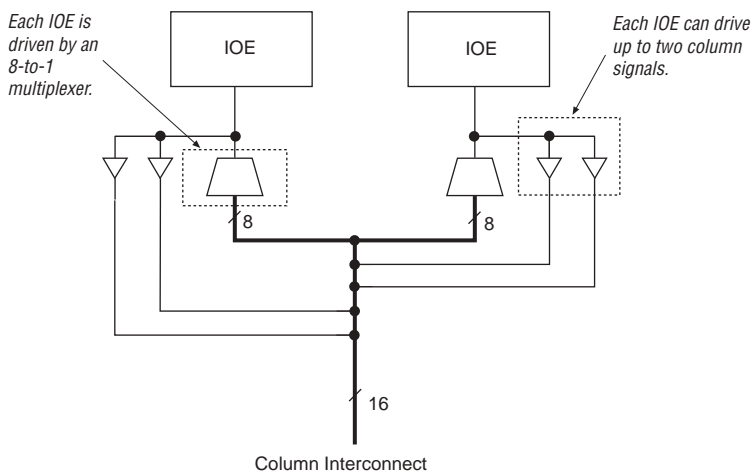
### *Clear & Preset Logic Control*

Logic for the programmable register's clear and preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that LABCTRL1 implements an asynchronous load. The data to be loaded is driven to DATA3; when LABCTRL1 is asserted, DATA3 is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See [Figure 7](#).

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

**Figure 12. FLEX 8000 Column-to-IOE Connections**

In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

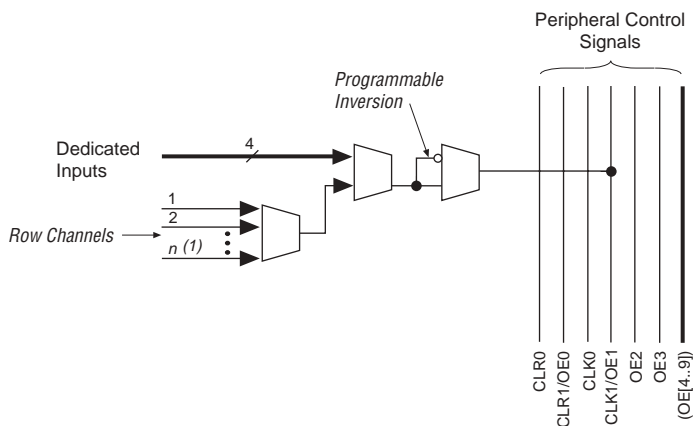
I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. [Figure 13 on page 22](#) shows how two output enable signals are shared with one clock and one clear signal.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

**Figure 13. FLEX 8000 Peripheral Bus**

*Numbers in parentheses are for EPF81500A devices.*



**Note:**

- (1)  $n = 13$  for EPF8282A and EPF8282AV devices.
- $n = 21$  for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
- $n = 27$  for EPF81500A devices.



Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

<b>Table 5. Row Sources of FLEX 8000 Peripheral Control Signals</b>						
<b>Peripheral Control Signal</b>	<b>EPF8282A EPF8282AV</b>	<b>EPF8452A</b>	<b>EPF8636A</b>	<b>EPF8820A</b>	<b>EPF81188A</b>	<b>EPF81500A</b>
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	—	—	—	—	—	Row B
OE5	—	—	—	—	—	Row C
OE6	—	—	—	—	—	Row D
OE7	—	—	—	—	—	Row D
OE8	—	—	—	—	—	Row E
OE9	—	—	—	—	—	Row F

## Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

### Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.



For more information on high-speed system design, go to [Application Note 75 \(High-Speed Board Designs\)](#).

**Table 15. FLEX 8000 3.3-V Device DC Operating Conditions** *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IH}$	High-level input voltage		2.0		$V_{CC} + 0.3$	V
$V_{IL}$	Low-level input voltage		-0.3		0.8	V
$V_{OH}$	High-level output voltage	$I_{OH} = -0.1$ mA DC (5)	$V_{CC} - 0.2$			V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA DC (5)			0.45	V
$I_I$	Input leakage current	$V_I = V_{CC}$ or ground	-10		10	$\mu$ A
$I_{OZ}$	Tri-state output off-state current	$V_O = V_{CC}$ or ground	-40		40	$\mu$ A
$I_{CC0}$	$V_{CC}$ supply current (standby)	$V_I =$ ground, no load (6)		0.3	10	mA

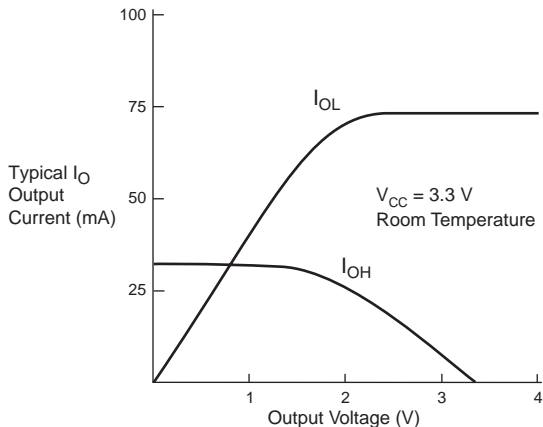
**Table 16. FLEX 8000 3.3-V Device Capacitance** *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{OUT}$	Output capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) The maximum  $V_{CC}$  rise time is 100 ms.  $V_{CC}$  must rise monotonically.
- (4) These values are specified in [Table 14 on page 29](#).
- (5) The  $I_{OH}$  parameter refers to high-level TTL output current; the  $I_{OL}$  parameter refers to low-level TTL output current.
- (6) Typical values are for  $T_A = 25^\circ$  C and  $V_{CC} = 3.3$  V.
- (7) Capacitance is sample-tested only.

**Figure 16** shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with *PCI Local Bus Specification, Revision 2.2*.

**Figure 18. Output Drive Characteristics of EPF8282AV Devices**

## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

**Table 17. FLEX 8000 Internal Timing Parameters** *Note (1)*

Symbol	Parameter
$t_{IOD}$	IOE register data delay
$t_{IOC}$	IOE register control signal delay
$t_{IOE}$	Output enable delay
$t_{IOCO}$	IOE register clock-to-output delay
$t_{IOCOMB}$	IOE combinatorial delay
$t_{IOSU}$	IOE register setup time before clock; IOE register recovery time after asynchronous clear
$t_{IOH}$	IOE register hold time after clock
$t_{IOCLR}$	IOE register clear delay
$t_{IN}$	Input pad and buffer delay
$t_{OD1}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 5.0\text{ V}$ , $C1 = 35\text{ pF}$ (2)
$t_{OD2}$	Output buffer and pad delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$ , $C1 = 35\text{ pF}$ (2)
$t_{OD3}$	Output buffer and pad delay, slow slew rate = on, $C1 = 35\text{ pF}$ (3)
$t_{XZ}$	Output buffer disable delay, $C1 = 5\text{ pF}$
$t_{ZX1}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = 5.0\text{ V}$ , $C1 = 35\text{ pF}$ (2)
$t_{ZX2}$	Output buffer enable delay, slow slew rate = off, $V_{CCIO} = 3.3\text{ V}$ , $C1 = 35\text{ pF}$ (2)
$t_{ZX3}$	Output buffer enable delay, slow slew rate = on, $C1 = 35\text{ pF}$ (3)

**Table 18. FLEX 8000 LE Timing Parameters** *Note (1)*

Symbol	Parameter
$t_{LUT}$	LUT delay for data-in
$t_{CLUT}$	LUT delay for carry-in
$t_{RLUT}$	LUT delay for LE register feedback
$t_{GATE}$	Cascade gate delay
$t_{CASC}$	Cascade chain routing delay
$t_{CICO}$	Carry-in to carry-out delay
$t_{CGEN}$	Data-in to carry-out delay
$t_{CGENR}$	LE register feedback to carry-out delay
$t_C$	LE register control signal delay
$t_{CH}$	LE register clock high time
$t_{CL}$	LE register clock low time
$t_{CO}$	LE register clock-to-output delay
$t_{COMB}$	Combinatorial delay
$t_{SU}$	LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load
$t_H$	LE register hold time after clock
$t_{PRE}$	LE register preset delay
$t_{CLR}$	LE register clear delay

**Table 19. FLEX 8000 Interconnect Timing Parameters** *Note (1)*

Symbol	Parameter
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
$t_{LOCAL}$	LAB local interconnect delay
$t_{ROW}$	Row interconnect routing delay (4)
$t_{COL}$	Column interconnect routing delay
$t_{DIN\_C}$	Dedicated input to LE control delay
$t_{DIN\_D}$	Dedicated input to LE data delay (4)
$t_{DIN\_IO}$	Dedicated input to IOE control delay

**Table 20. FLEX 8000 External Reference Timing Characteristics** *Note (5)*

Symbol	Parameter
$t_{DRR}$	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects (6)
$t_{ODH}$	Output data hold time after clock (7)

**Notes to tables:**

- (1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
- (2) These values are specified in [Table 10 on page 28](#) or [Table 14 on page 29](#).
- (3) For the  $t_{OD3}$  and  $t_{ZX3}$  parameters,  $V_{CCIO} = 3.3\text{ V}$  or  $5.0\text{ V}$ .
- (4) The  $t_{ROW}$  and  $t_{DIN\_D}$  delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
- (5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
- (6) For more information on test conditions, see [Application Note 76 \(Understanding FLEX 8000 Timing\)](#).
- (7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See [Figure 19](#). This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in [Figure 19](#) is expressed as a worst-case value in [Tables 22 through 49](#). Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. [Table 21](#) summarizes the interconnect paths shown in [Figure 19](#).



For more information on timing parameters, go to [Application Note 76 \(Understanding FLEX 8000 Timing\)](#).

**Table 21. FLEX 8000 Timing Model Interconnect Paths**

Source	Destination	Total Delay
LE-Out	LE in same LAB	$t_{LOCAL}$
LE-Out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-Out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-Out	IOE on column	$t_{COL}$
LE-Out	IOE on row	$t_{ROW}$
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Tables 22 through 49 show the FLEX 8000 internal and external timing parameters.

**Table 22. EPF8282A Internal I/O Element Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		0.7		0.8		0.9	ns
$t_{IOC}$		1.7		1.8		1.9	ns
$t_{IOE}$		1.7		1.8		1.9	ns
$t_{IOCO}$		1.0		1.0		1.0	ns
$t_{IOCOMB}$		0.3		0.2		0.1	ns
$t_{IOSU}$	1.4		1.6		1.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.2		1.2		1.2	ns
$t_{IN}$		1.5		1.6		1.7	ns
$t_{OD1}$		1.1		1.4		1.7	ns
$t_{OD2}$		—		—		—	ns
$t_{OD3}$		4.6		4.9		5.2	ns
$t_{XZ}$		1.4		1.6		1.8	ns
$t_{ZX1}$		1.4		1.6		1.8	ns
$t_{ZX2}$		—		—		—	ns
$t_{ZX3}$		4.9		5.1		5.3	ns

**Table 23. EPF8282A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
$t_{LOCAL}$		0.5		0.6		0.8	ns
$t_{ROW}$		4.2		4.2		4.2	ns
$t_{COL}$		2.5		2.5		2.5	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		7.2		7.2		7.2	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns

**Table 42. EPF81188A I/O Element Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{IOD}$		0.7		0.8		0.9	ns
$t_{IOC}$		1.7		1.8		1.9	ns
$t_{IOE}$		1.7		1.8		1.9	ns
$t_{IOCO}$		1.0		1.0		1.0	ns
$t_{IOCOMB}$		0.3		0.2		0.1	ns
$t_{IOSU}$	1.4		1.6		1.8		ns
$t_{IOH}$	0.0		0.0		0.0		ns
$t_{IOCLR}$		1.2		1.2		1.2	ns
$t_{IN}$		1.5		1.6		1.7	ns
$t_{OD1}$		1.1		1.4		1.7	ns
$t_{OD2}$		1.6		1.9		2.2	ns
$t_{OD3}$		4.6		4.9		5.2	ns
$t_{XZ}$		1.4		1.6		1.8	ns
$t_{ZX1}$		1.4		1.6		1.8	ns
$t_{ZX2}$		1.9		2.1		2.3	ns
$t_{ZX3}$		4.9		5.1		5.3	ns

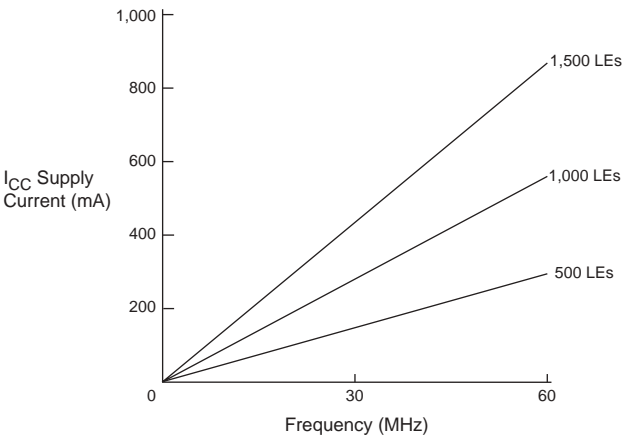
**Table 43. EPF81188A Interconnect Timing Parameters**

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
$t_{LOCAL}$		0.5		0.6		0.8	ns
$t_{ROW}$		5.0		5.0		5.0	ns
$t_{COL}$		3.0		3.0		3.0	ns
$t_{DIN\_C}$		5.0		5.0		5.5	ns
$t_{DIN\_D}$		7.0		7.0		7.5	ns
$t_{DIN\_IO}$		5.0		5.0		5.5	ns

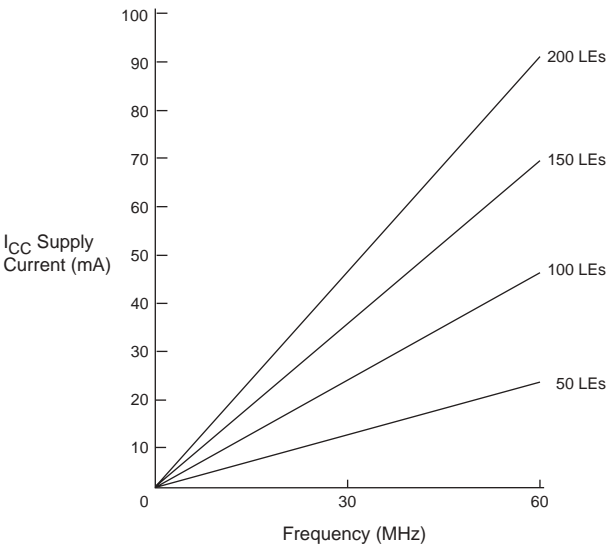


Figure 20. FLEX 8000  $I_{CCACTIVE}$  vs. Operating Frequency

5.0-V FLEX 8000 Devices



3.3-V FLEX 8000 Devices



# Configuration & Operation



The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to [Application Note 33 \(Configuring FLEX 8000 Devices\)](#) and [Application Note 38 \(Configuring Multiple FLEX 8000 Devices\)](#).

## Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)**

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
nSP (2)	75	75	75	76	110	R1	1
MSEL0 (2)	74	74	74	75	109	P2	2
MSEL1 (2)	53	53	51	51	72	A1	44
nSTATUS (2)	32	32	24	25	37	C13	82
nCONFIG (2)	33	33	25	26	38	A15	81
DCLK (2)	10	10	100	100	143	P14	125
CONF_DONE (2)	11	11	1	1	144	N13	124
nWS	30	30	22	23	33	F13	87
nRS	48	48	42	45	31	C6	89
RDCLK	49	49	45	46	12	B5	110
nCS	29	29	21	22	4	D15	118
CS	28	28	19	21	3	E15	121
RDYnBUSY	77	77	77	78	20	P3	100
CLKUSR	50	50	47	47	13	C5	107
ADD17	51	51	49	48	75	B4	40
ADD16	36	55	28	54	76	E2	39
ADD15	56	56	55	55	77	D1	38
ADD14	57	57	57	57	78	E1	37
ADD13	58	58	58	58	79	F3	36
ADD12	60	60	59	60	83	F2	32
ADD11	61	61	60	61	85	F1	30
ADD10	62	62	61	62	87	G2	28
ADD9	63	63	62	64	89	G1	26
ADD8	64	64	64	65	92	H1	22
ADD7	65	65	65	66	94	H2	20
ADD6	66	66	66	67	95	J1	18
ADD5	67	67	67	68	97	J2	16
ADD4	69	69	68	70	102	K2	11
ADD3	70	70	69	71	103	K1	10
ADD2	71	71	71	72	104	K3	8
ADD1	76	72	76	73	105	M1	7

**Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 3 of 3)**

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A (1)
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	19, 44, 69, 94	7, 17, 27, 39, 54, 80, 81, 100, 101, 128, 142	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155
No Connect (N.C.)	—	—	—	2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99	—	—	—
Total User I/O Pins (9)	64	64	74	64	108	116	116

**Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)**

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP (2)	A15	C14	237	237	W1	304
MSEL0 (2)	B14	G15	21	19	N1	26
MSEL1 (2)	R15	L15	40	38	H3	51
nSTATUS (2)	P2	L3	141	142	G19	178
nCONFIG (2)	R1	R4	117	120	B18	152
DCLK (2)	B2	C4	184	183	U18	230
CONF_DONE (2)	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDynBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

### Notes to tables:

- (1) Perform a complete thermal analysis before committing a design to this device package. See [Application Note 74 \(Evaluating Power for Altera Devices\)](#) for more information.
- (2) This pin is a dedicated pin and is not available as a user I/O pin.
- (3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
- (4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
- (5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
- (6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
- (7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
- (8) Pin 52 is a  $V_{CC}$  pin on EPF8452A devices only.
- (9) The user I/O pin count includes dedicated input pins and all I/O pins.
- (10) Unused dedicated inputs should be tied to ground on the board.
- (11) SDOUT does not exist in the EPF8636GC192 device.
- (12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
- (13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
- (14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

## Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.