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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 63 |
| Number of Logic Elements/Cells | 504 |
| Total RAM Bits | - |
| Number of I/O | 136 |
| Number of Gates | - |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf8636aqc208-3 |

| | | | | | | |
|---|---|---|---|---|---|---|
| JTAG BST circuitry | Yes | No | Yes | Yes | No | Yes |

## ...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

*Table 2. FLEX 8000 Package Options & I/O Pin Count* *Note (1)*

| Device | 84-Pin PLCC | 100-Pin TQFP | 144-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 225-Pin BGA | 232-Pin PGA | 240-Pin PQFP | 280-Pin PGA | 304-Pin RQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPF8282A | 68 | 78 | | | | | | | | | | |
| EPF8282AV | | 78 | | | | | | | | | | |
| EPF8452A | 68 | 68 | | 120 | 120 | | | | | | | |
| EPF8636A | 68 | | | 118 | | 136 | 136 | | | | | |
| EPF8820A | | | 112 | 120 | | 152 | 152 | 152 | | | | |
| EPF81188A | | | | | | | 148 | | 184 | 184 | | |
| EPF81500A | | | | | | | | | | 181 | 208 | 208 |

*Note:*
(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

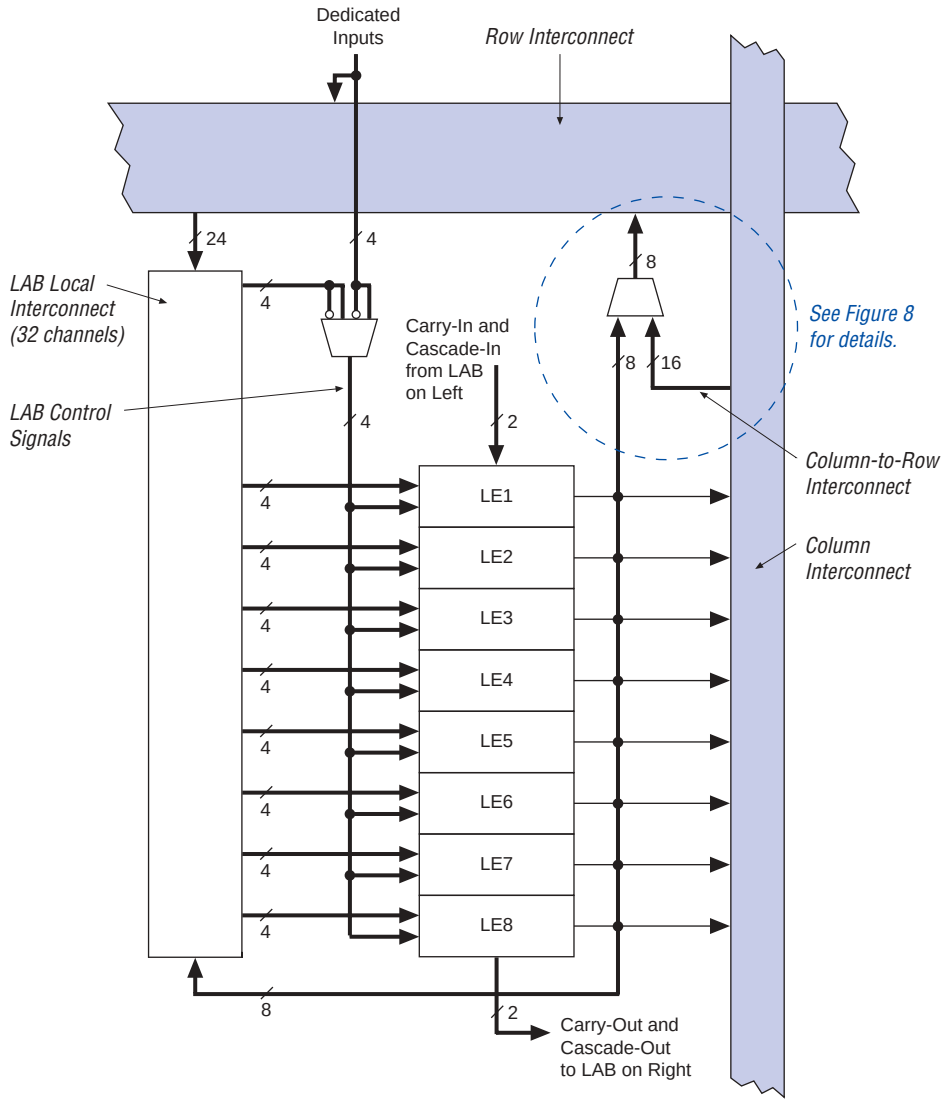
## General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

## Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

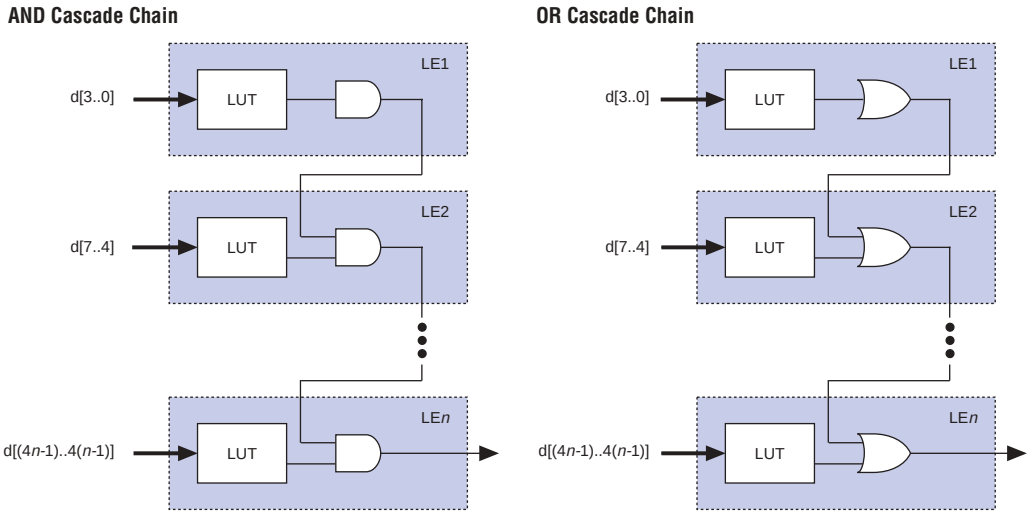
*Figure 2. FLEX 8000 Logic Array Block*



The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

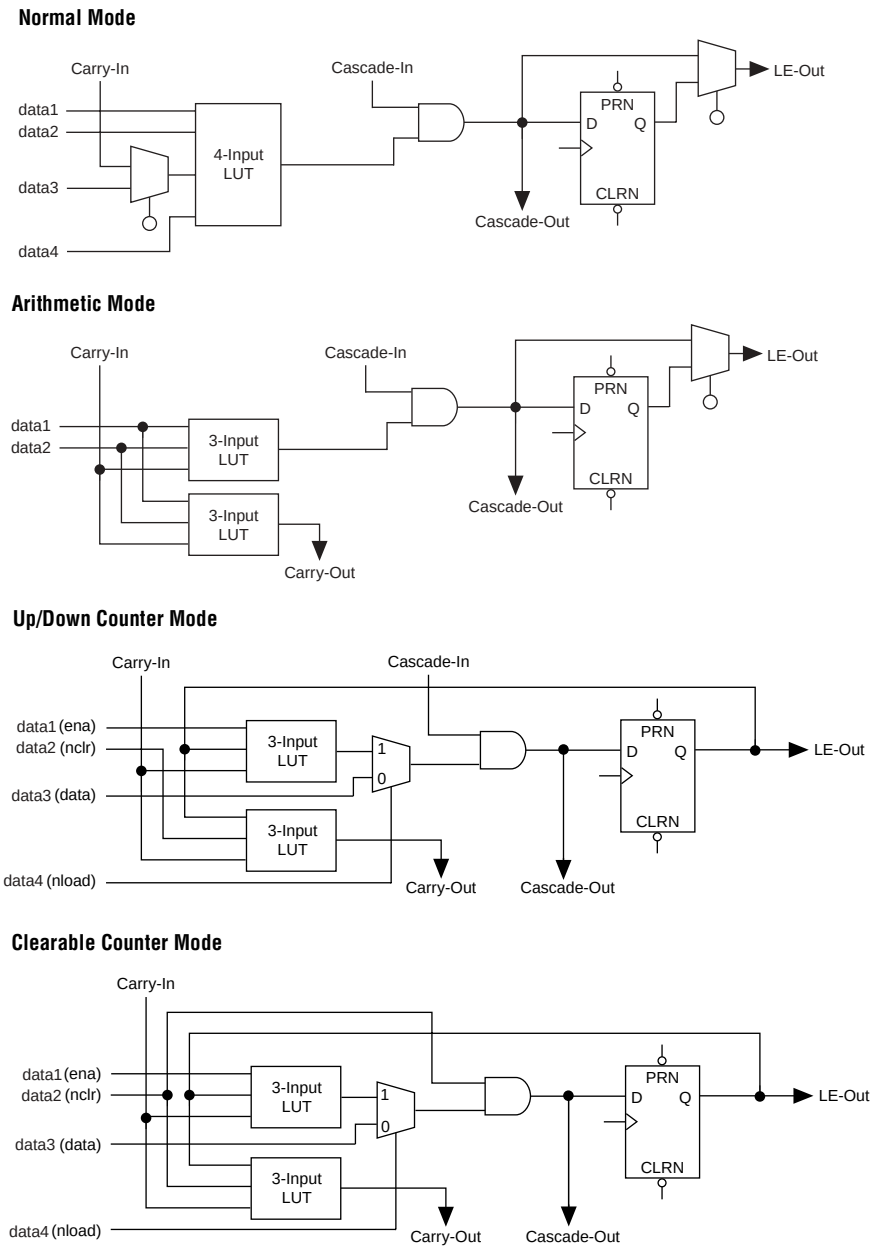
***Figure 5. FLEX 8000 Cascade Chain Operation***




## *LE Operating Modes*

The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

*Figure 6. FLEX 8000 LE Operating Modes*



The instruction register length for FLEX 8000 devices is three bits. Table 7 shows the boundary-scan register length for FLEX 8000 devices.

*Table 7. FLEX 8000 Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EPF8282A, EPF8282AV | 273 |
| EPF8636A | 417 |
| EPF8820A | 465 |
| EPF81500A | 645 |

FLEX 8000 devices that support JTAG include weak pull-ups on the JTAG pins. Figure 14 shows the timing requirements for the JTAG signals.

*Figure 14. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Waveforms*

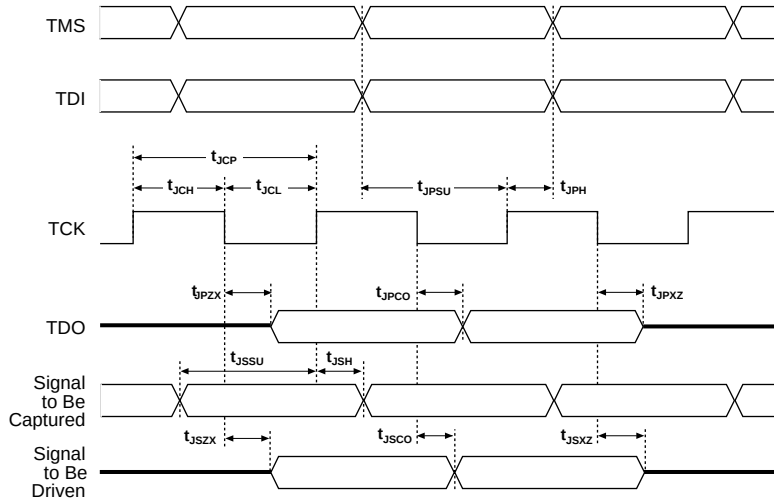
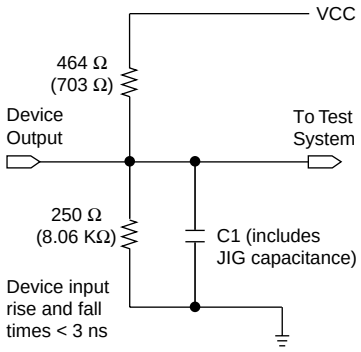



Table 8 shows the timing parameters and values for EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices.

*Figure 15. FLEX 8000 AC Test Conditions*

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices or outputs. Numbers without parentheses are for 5.0-V devices or outputs.*



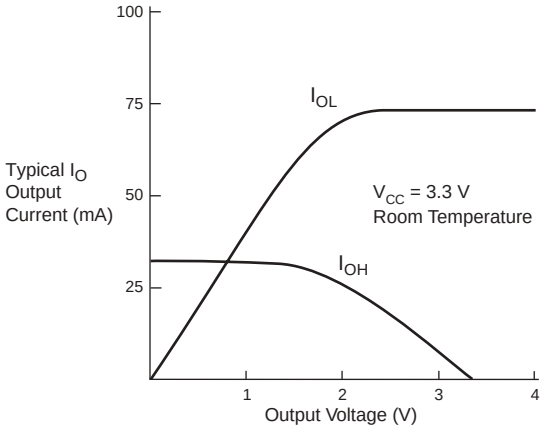

## Operating Conditions

Tables 9 through 12 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V FLEX 8000 devices.

*Table 9. FLEX 8000 5.0-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP and RQFP, under bias | | 135 | ° C |

*Figure 18. Output Drive Characteristics of EPF8282AV Devices*




## Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

| Table 17. FLEX 8000 Internal Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{IOD}$ | IOE register data delay |
| $t_{IOC}$ | IOE register control signal delay |
| $t_{IOE}$ | Output enable delay |
| $t_{IOCO}$ | IOE register clock-to-output delay |
| $t_{IOCOMB}$ | IOE combinatorial delay |
| $t_{IOSU}$ | IOE register setup time before clock; IOE register recovery time after asynchronous clear |
| $t_{IOH}$ | IOE register hold time after clock |
| $t_{IOCLR}$ | IOE register clear delay |
| $t_{IN}$ | Input pad and buffer delay |
| $t_{OD1}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 5.0 V C1 = 35 pF *(2)* |
| $t_{OD2}$ | Output buffer and pad delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V C1 = 35 pF *(2)* |
| $t_{OD3}$ | Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)* |
| $t_{XZ}$ | Output buffer disable delay, C1 = 5 pF |
| $t_{ZX1}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 5.0 V, C1 = 35 pF *(2)* |
| $t_{ZX2}$ | Output buffer enable delay, slow slew rate = off, $V_{CCIO}$ = 3.3 V, C1 = 35 pF *(2)* |
| $t_{ZX3}$ | Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)* |

| Table 18. FLEX 8000 LE Timing Parameters *Note (1)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{CLUT}$ | LUT delay for carry-in |
| $t_{RLUT}$ | LUT delay for LE register feedback |
| $t_{GATE}$ | Cascade gate delay |
| $t_{CASC}$ | Cascade chain routing delay |
| $t_{CICO}$ | Carry-in to carry-out delay |
| $t_{CGEN}$ | Data-in to carry-out delay |
| $t_{CGENR}$ | LE register feedback to carry-out delay |
| $t_{C}$ | LE register control signal delay |
| $t_{CH}$ | LE register clock high time |
| $t_{CL}$ | LE register clock low time |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{COMB}$ | Combinatorial delay |
| $t_{SU}$ | LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load |
| $t_{H}$ | LE register hold time after clock |
| $t_{PRE}$ | LE register preset delay |
| $t_{CLR}$ | LE register clear delay |

| Table 19. FLEX 8000 Interconnect Timing Parameters Note (1) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs |
| $t_{LOCAL}$ | LAB local interconnect delay |
| $t_{ROW}$ | Row interconnect routing delay *(4)* |
| $t_{COL}$ | Column interconnect routing delay |
| $t_{DIN\_C}$ | Dedicated input to LE control delay |
| $t_{DIN\_D}$ | Dedicated input to LE data delay *(4)* |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay |

| Table 20. FLEX 8000 External Reference Timing Characteristics Note (5) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)* |
| $t_{ODH}$ | Output data hold time after clock *(7)* |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the $t_{OD3}$ and $t_{ZX3}$ parameters, $V_{CCIO}$ = 3.3 V or 5.0 V.
(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

*Figure 19. FLEX 8000 Timing Model*

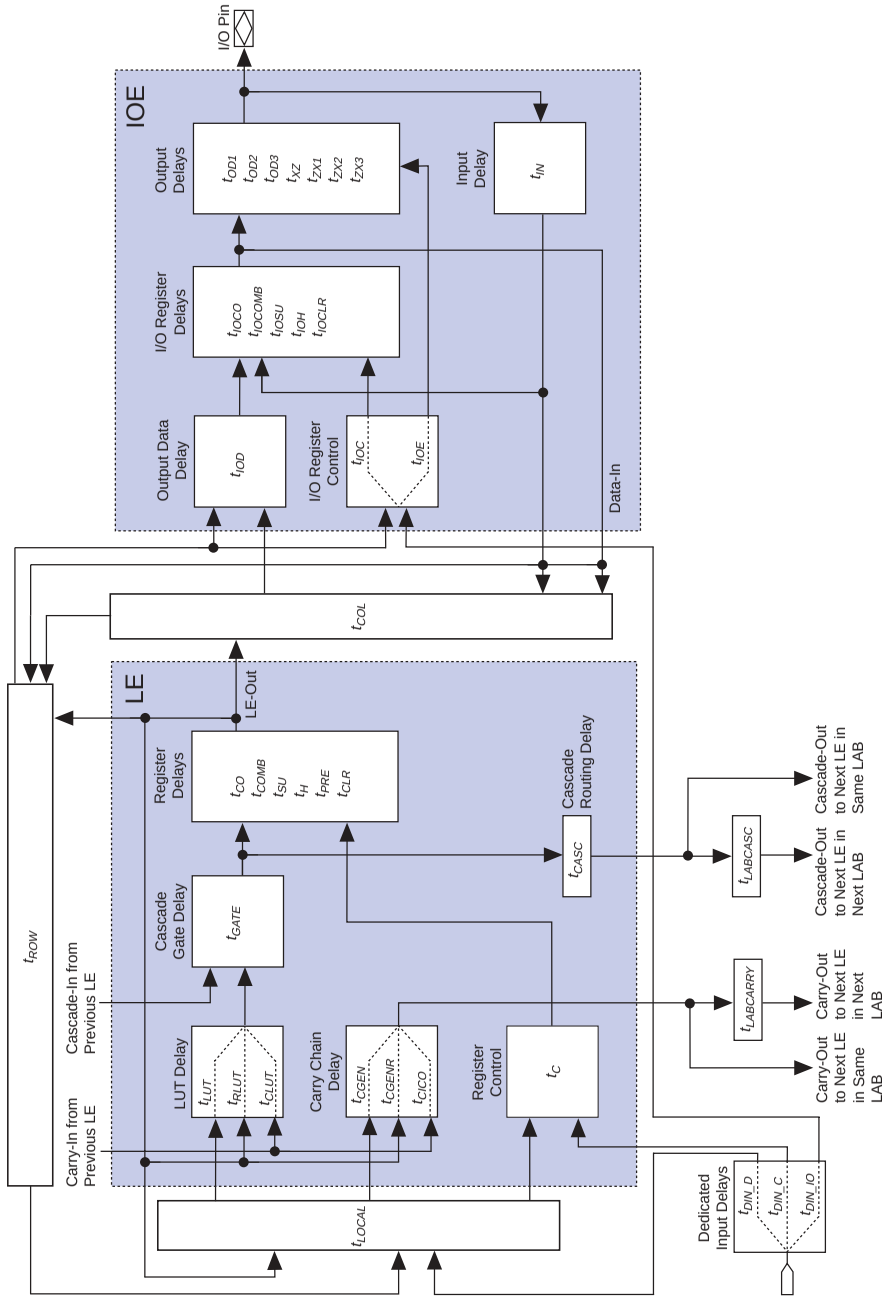


*Table 24. EPF8282A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 25. EPF8282A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 15.8 | | 19.8 | | 24.8 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 26. EPF8282AV I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.9 | | 2.2 | ns |
| $t_{IOC}$ | | 1.9 | | 2.0 | ns |
| $t_{IOE}$ | | 1.9 | | 2.0 | ns |
| $t_{IOCO}$ | | 1.0 | | 2.0 | ns |
| $t_{IOCOMB}$ | | 0.1 | | 0.0 | ns |
| $t_{IOSU}$ | 1.8 | | 2.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.2 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 2.3 | ns |
| $t_{IN}$ | | 1.7 | | 3.4 | ns |
| $t_{OD1}$ | | 1.7 | | 4.1 | ns |
| $t_{OD2}$ | | – | | – | ns |
| $t_{OD3}$ | | 5.2 | | 7.1 | ns |
| $t_{XZ}$ | | 1.8 | | 4.3 | ns |
| $t_{ZX1}$ | | 1.8 | | 4.3 | ns |
| $t_{ZX2}$ | | – | | – | ns |
| $t_{ZX3}$ | | 5.3 | | 8.3 | ns |

*Table 27. EPF8282AV Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.4 | | 1.3 | ns |
| $t_{LABCARRY}$ | | 0.4 | | 0.8 | ns |
| $t_{LOCAL}$ | | 0.8 | | 1.5 | ns |
| $t_{ROW}$ | | 4.2 | | 6.3 | ns |
| $t_{COL}$ | | 2.5 | | 3.8 | ns |
| $t_{DIN\_C}$ | | 5.5 | | 8.0 | ns |
| $t_{DIN\_D}$ | | 7.2 | | 10.8 | ns |
| $t_{DIN\_IO}$ | | 5.5 | | 9.0 | ns |

*Table 28. EPF8282AV Logic Element Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{LUT}$ | | 3.2 | | 7.3 | ns |
| $t_{CLUT}$ | | 0.0 | | 1.4 | ns |
| $t_{RLUT}$ | | 1.5 | | 5.1 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.9 | | 2.8 | ns |
| $t_{CICO}$ | | 0.6 | | 1.5 | ns |
| $t_{CGEN}$ | | 0.7 | | 2.2 | ns |
| $t_{CGENR}$ | | 1.5 | | 3.7 | ns |
| $t_{C}$ | | 2.5 | | 4.7 | ns |
| $t_{CH}$ | 4.0 | | 6.0 | | ns |
| $t_{CL}$ | 4.0 | | 6.0 | | ns |
| $t_{CO}$ | | 0.6 | | 0.9 | ns |
| $t_{COMB}$ | | 0.6 | | 0.9 | ns |
| $t_{SU}$ | 1.2 | | 2.4 | | ns |
| $t_{H}$ | 1.5 | | 4.6 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.3 | ns |
| $t_{CLR}$ | | 0.8 | | 1.3 | ns |

*Table 29. EPF8282AV External Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{DRR}$ | | 24.8 | | 50.1 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | ns |

*Table 36. EPF8636A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.3 | | 3.0 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.2 | | 0.1 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.6 | | 1.6 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.9 | | 0.8 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.4 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 1.8 | | 2.4 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.0 | | 1.1 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.4 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 37. EPF8636A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.0 | | 20.0 | | 25.0 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 40. EPF8820A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 41. EPF8820A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.0 | | 20.0 | | 25.0 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 46. EPF81500A I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | 1.6 | | 1.9 | | 2.2 | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | 1.9 | | 2.1 | | 2.3 | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 47. EPF81500A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 6.2 | | 6.2 | | 6.2 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 8.2 | | 8.2 | | 8.7 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

## Power Consumption

The supply power (P) for FLEX 8000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = [(I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC}] + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as $I_{CC0}$ in Table 11 on page 28 and Table 15 on page 30. The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock
K = Constant, shown in Table 50

*Table 50. Values for Constant K*

| Device | K |
|---|---|
| 5.0-V FLEX 8000 devices | 75 |
| 3.3-V FLEX 8000 devices | 60 |

This calculation provides an $I_{CC}$ estimate based on typical conditions with no output load. The actual $I_{CC}$ value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 20 shows the relationship between $I_{CC}$ and operating frequency for several LE utilization values.

*Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 84-Pin PLCC EPF8282A | 84-Pin PLCC EPF8452A EPF8636A | 100-Pin TQFP EPF8282A EPF8282AV | 100-Pin TQFP EPF8452A | 144-Pin TQFP EPF8820A | 160-Pin PGA EPF8452A | 160-Pin PQFP EPF8820A *(1)* |
|---|---|---|---|---|---|---|---|
| ADD0 | 78 | 76 | 78 | 77 | 106 | N3 | 6 |
| DATA7 | 3 | 2 | 90 | 89 | 131 | P8 | 140 |
| DATA6 | 4 | 4 | 91 | 91 | 132 | P10 | 139 |
| DATA5 | 6 | 6 | 92 | 95 | 133 | R12 | 138 |
| DATA4 | 7 | 7 | 95 | 96 | 134 | R13 | 136 |
| DATA3 | 8 | 8 | 97 | 97 | 135 | P13 | 135 |
| DATA2 | 9 | 9 | 99 | 98 | 137 | R14 | 133 |
| DATA1 | 13 | 13 | 4 | 4 | 138 | N15 | 132 |
| DATA0 | 14 | 14 | 5 | 5 | 140 | K13 | 129 |
| SDOUT *(3)* | 79 | 78 | 79 | 79 | 23 | P4 | 97 |
| TDI *(4)* | 55 | 45 *(5)* | 54 | – | 96 | – | 17 |
| TDO *(4)* | 27 | 27 *(5)* | 18 | – | 18 | – | 102 |
| TCK *(4)*, *(6)* | 72 | 44 *(5)* | 72 | – | 88 | – | 27 |
| TMS *(4)* | 20 | 43 *(5)* | 11 | – | 86 | – | 29 |
| TRST *(7)* | 52 | 52 *(8)* | 50 | – | 71 | – | 45 |
| Dedicated Inputs *(10)* | 12, 31, 54, 73 | 12, 31, 54, 73 | 3, 23, 53, 73 | 3, 24, 53, 74 | 9, 26, 82, 99 | C3, D14, N2, R15 | 14, 33, 94, 113 |
| VCCINT | 17, 38, 59, 80 | 17, 38, 59, 80 | 6, 20, 37, 56, 70, 87 | 9, 32, 49, 59, 82 | 8, 28, 70, 90, 111 | B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12 | 3, 24, 46, 92, 114, 160 |
| VCCIO | – | – | – | – | 16, 40, 60, 69, 91, 112, 122, 141 | – | 23, 47, 57, 69, 79, 104, 127, 137, 149, 159 |

*Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 3 of 3)*

| Pin Name | 84-Pin PLCC EPF8282A | 84-Pin PLCC EPF8452A EPF8636A | 100-Pin TQFP EPF8282A EPF8282AV | 100-Pin TQFP EPF8452A | 144-Pin TQFP EPF8820A | 160-Pin PGA EPF8452A | 160-Pin PQFP EPF8820A *(1)* |
|---|---|---|---|---|---|---|---|
| GND | 5, 26, 47, 68 | 5, 26, 47, 68 | 2, 13, 30, 44, 52, 63, 80, 94 | 19, 44, 69, 94 | 7, 17, 27, 39, 54, 80, 81, 100,101, 128, 142 | C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4 | 12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155 |
| No Connect (N.C.) | – | – | – | 2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99 | – | – | – |
| Total User I/O Pins *(9)* | 64 | 64 | 74 | 64 | 108 | 116 | 116 |

*Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 225-Pin BGA EPF8820A | 232-Pin PGA EPF81188A | 240-Pin PQFP EPF81188A | 240-Pin PQFP EPF81500A | 280-Pin PGA EPF81500A | 304-Pin RQFP EPF81500A |
|---|---|---|---|---|---|---|
| DATA4 | A5 | C7 | 198 | 194 | W16 | 248 |
| DATA3 | B5 | D7 | 196 | 193 | W17 | 246 |
| DATA2 | E6 | B5 | 194 | 190 | V16 | 243 |
| DATA1 | D5 | A3 | 191 | 189 | U16 | 241 |
| DATA0 | C4 | A2 | 189 | 187 | V17 | 239 |
| SDOUT *(3)* | K1 | N2 | 135 | 136 | F19 | 169 |
| TDI | F15 *(4)* | – | – | 63 *(14)* | B1 *(14)* | 80 *(14)* |
| TDO | J2 *(4)* | – | – | 117 | C17 | 149 |
| TCK *(6)* | J14 *(4)* | – | – | 116 *(14)* | A19 *(14)* | 148 *(14)* |
| TMS | J12 *(4)* | – | – | 64 *(14)* | C2 *(14)* | 81 *(14)* |
| TRST *(7)* | P14 | – | – | 115 *(14)* | A18 *(14)* | 145 *(14)* |
| Dedicated Inputs *(10)* | F4, L1, K12, E15 | C1, C17, R1, R17 | 10, 51, 130, 171 | 8, 49, 131, 172 | F1, F16, P3, P19 | 12, 64, 164, 217 |
| VCCINT (5.0 V) | F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13 | E4, H4, L4, P12, L14, H14, E14, R14, U1 | 20, 42, 64, 66, 114, 128, 150, 172, 236 | 18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236 | B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14 | 24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301 |
| VCCIO (5.0 V or 3.3 V) | H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2 | N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13 | 19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235 | 17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235 | D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15 | 22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300 |