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Understanding Embedded - FPGAs (Field Programmable Gate Array)

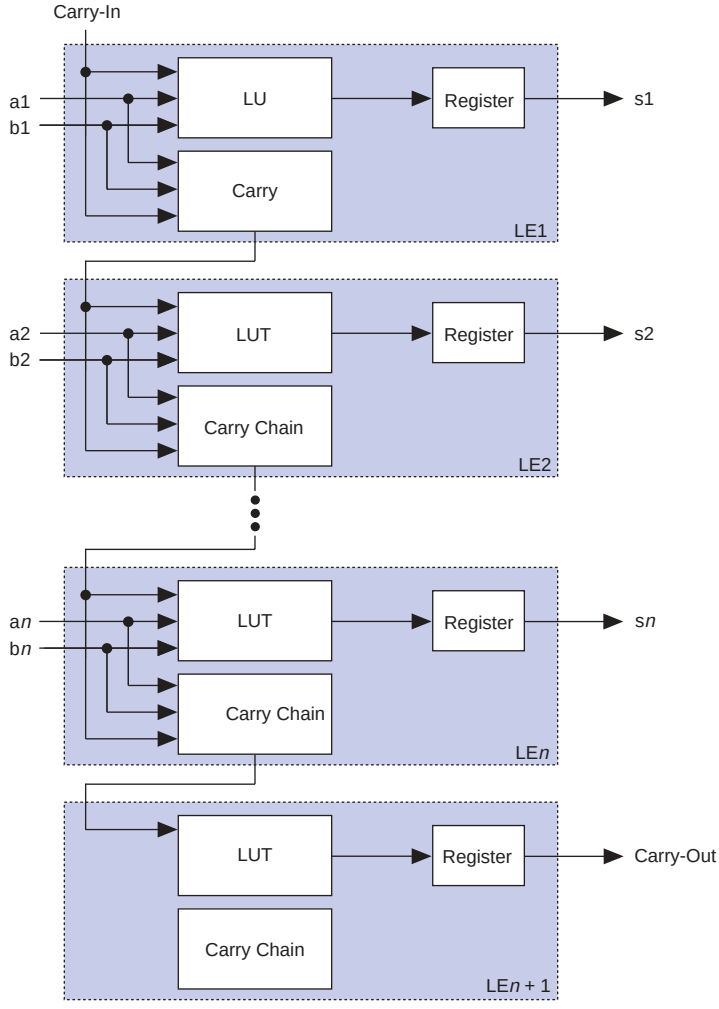
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	63
Number of Logic Elements/Cells	504
Total RAM Bits	-
Number of I/O	136
Number of Gates	-
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf8636aqc208-4

Figure 4. FLEX 8000 Carry Chain Operation



Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.6 ns per LE.

Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes

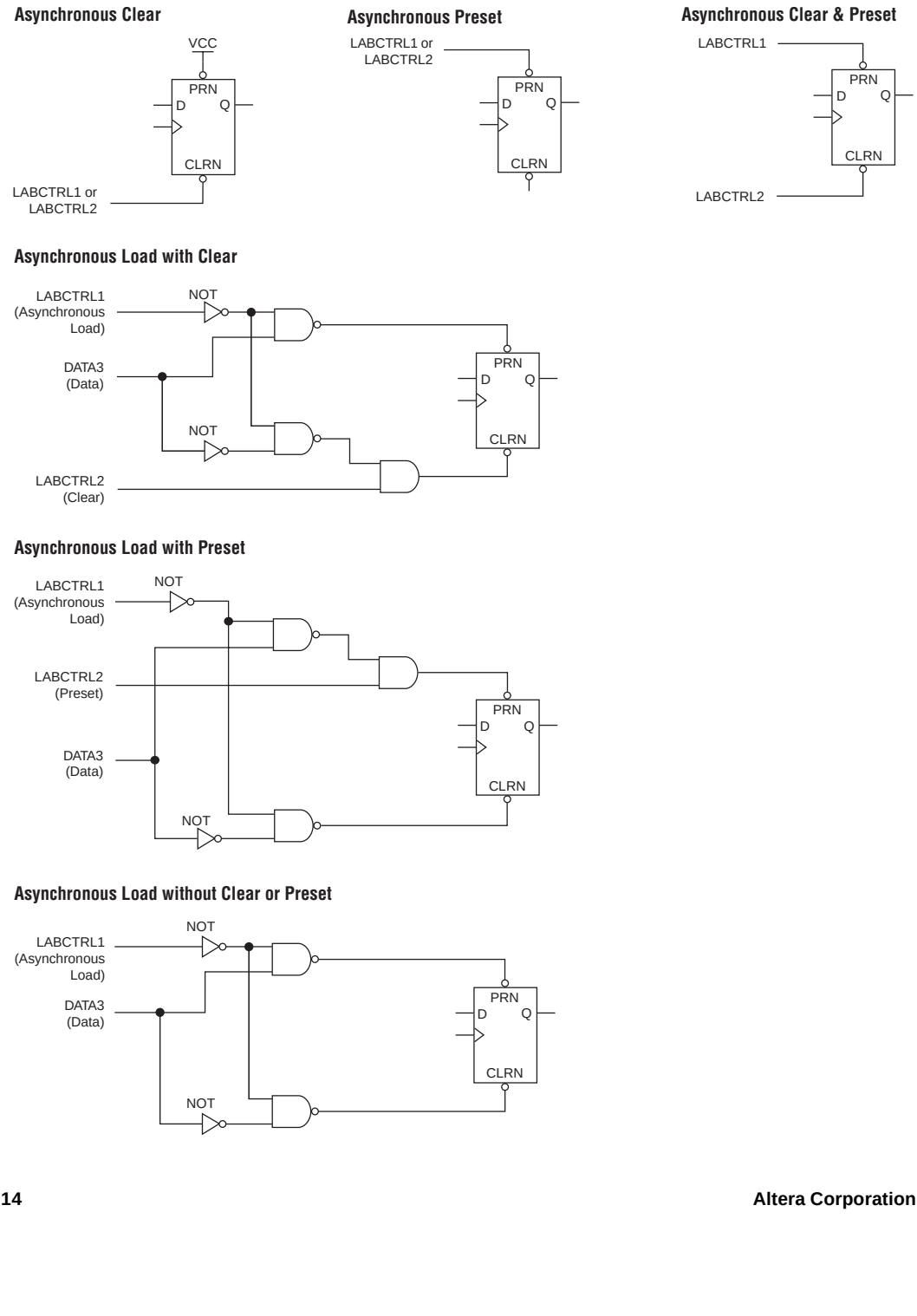
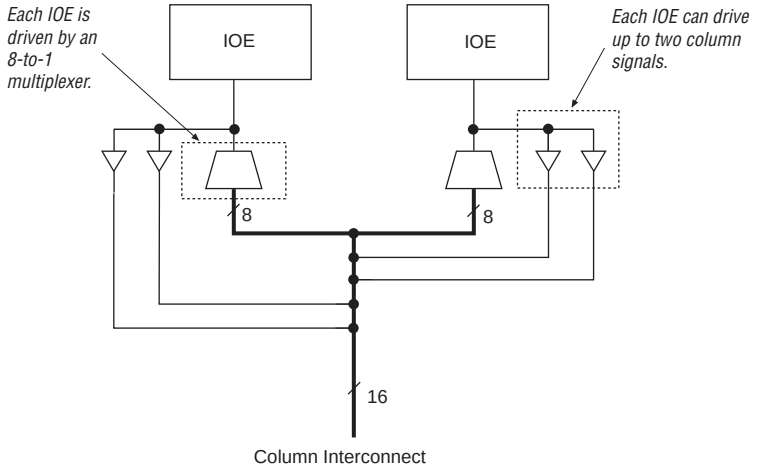


Figure 12. FLEX 8000 Column-to-IOE Connections



In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

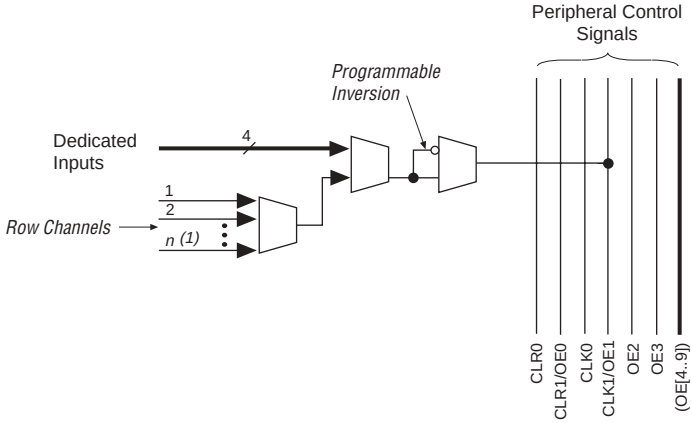
I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. Figure 13 on page 22 shows how two output enable signals are shared with one clock and one clear signal.

The signals for the peripheral bus can be generated by any of the four dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels in a row that can drive the peripheral bus correlates to the number of columns in the FLEX 8000 device. EPF8282A and EPF8282AV devices use 13 channels; EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices use 21 channels; and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The six peripheral control signals (12 in EPF81500A devices) can be accessed by each IOE.

Figure 13. FLEX 8000 Peripheral Bus

Numbers in parentheses are for EPF81500A devices.



Note:

(1) n = 13 for EPF8282A and EPF8282AV devices.
n = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
n = 27 for EPF81500A devices.

The instruction register length for FLEX 8000 devices is three bits. Table 7 shows the boundary-scan register length for FLEX 8000 devices.

Table 7. FLEX 8000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF8282A, EPF8282AV	273
EPF8636A	417
EPF8820A	465
EPF81500A	645

FLEX 8000 devices that support JTAG include weak pull-ups on the JTAG pins. Figure 14 shows the timing requirements for the JTAG signals.

Figure 14. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Waveforms

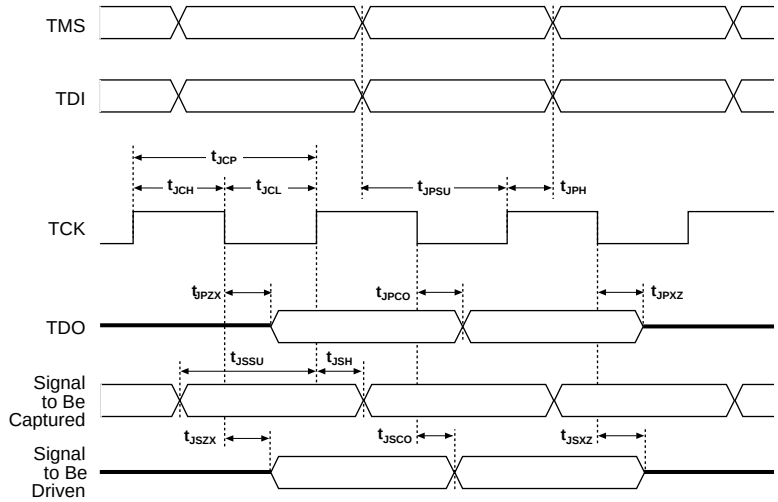


Table 8 shows the timing parameters and values for EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices.

Table 8. JTAG Timing Parameters & Values

Symbol	Parameter	EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A		Unit
		Min	Max	
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high-impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high-impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high-impedance		35	ns

For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Designers can use multiple test patterns to configure devices during all stages of the production flow.

Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)

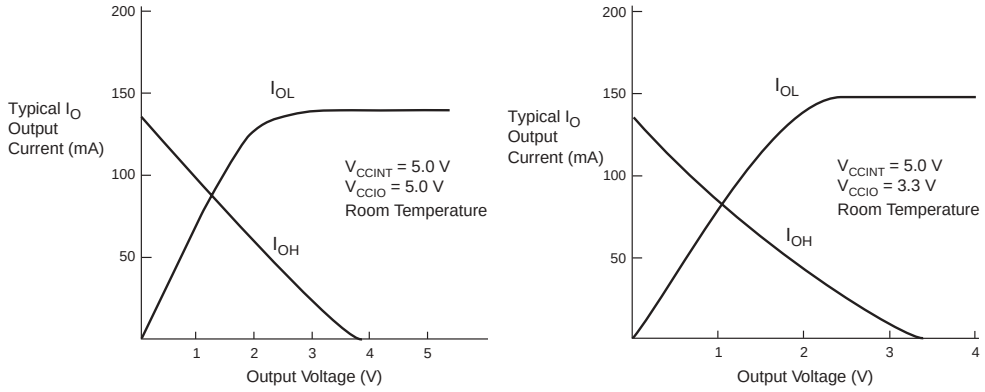


Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V V_{CCIO}

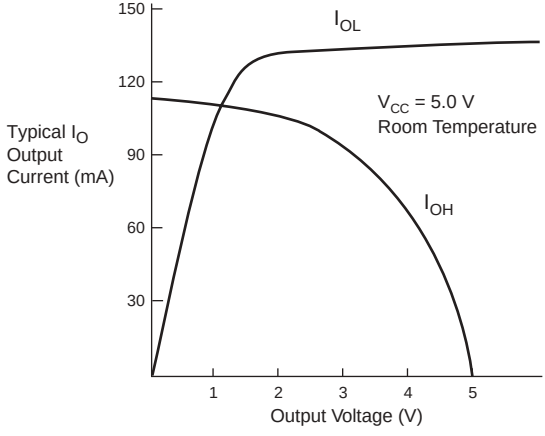


Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

Table 17. FLEX 8000 Internal Timing Parameters *Note (1)*	
Symbol	**Parameter**
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock; IOE register recovery time after asynchronous clear
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V C1 = 35 pF *(2)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF *(2)*
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF *(2)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)*

Table 18. FLEX 8000 LE Timing Parameters *Note (1)*	
Symbol	**Parameter**
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	LE register clock high time
t_{CL}	LE register clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 19. FLEX 8000 Interconnect Timing Parameters Note (1)	
Symbol	**Parameter**
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay *(4)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay *(4)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 20. FLEX 8000 External Reference Timing Characteristics Note (5)	
Symbol	**Parameter**
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)*
t_{ODH}	Output data hold time after clock *(7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.
(4) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

Table 21. FLEX 8000 Timing Model Interconnect Paths

Source	Destination	Total Delay
LE-Out	LE in same LAB	t_{LOCAL}
LE-Out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-Out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-Out	IOE on column	t_{COL}
LE-Out	IOE on row	t_{ROW}
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Tables 22 through 49 show the FLEX 8000 internal and external timing parameters.

Table 22. EPF8282A Internal I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		–		–		–	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 23. EPF8282A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.2		7.2		7.2	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 26. EPF8282AV I/O Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{IOD}		0.9		2.2	ns
t_{IOC}		1.9		2.0	ns
t_{IOE}		1.9		2.0	ns
t_{IOCO}		1.0		2.0	ns
t_{IOCOMB}		0.1		0.0	ns
t_{IOSU}	1.8		2.8		ns
t_{IOH}	0.0		0.2		ns
t_{IOCLR}		1.2		2.3	ns
t_{IN}		1.7		3.4	ns
t_{OD1}		1.7		4.1	ns
t_{OD2}		–		–	ns
t_{OD3}		5.2		7.1	ns
t_{XZ}		1.8		4.3	ns
t_{ZX1}		1.8		4.3	ns
t_{ZX2}		–		–	ns
t_{ZX3}		5.3		8.3	ns

Table 27. EPF8282AV Interconnect Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
$t_{LABCASC}$		0.4		1.3	ns
$t_{LABCARRY}$		0.4		0.8	ns
t_{LOCAL}		0.8		1.5	ns
t_{ROW}		4.2		6.3	ns
t_{COL}		2.5		3.8	ns
t_{DIN_C}		5.5		8.0	ns
t_{DIN_D}		7.2		10.8	ns
t_{DIN_IO}		5.5		9.0	ns

Table 32. EPF8452A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_{C}		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_{H}	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 33. EPF8452A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 44. EPF81188A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 45. EPF81188A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 46. EPF81500A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 47. EPF81500A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. Table 51 shows the data source for each of the six configuration schemes.

Table 51. Data Source for Configuration

Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera configuration device
Active parallel up	APU	Parallel configuration device
Active parallel down	APD	Parallel configuration device
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
ADD0	78	76	78	77	106	N3	6
DATA7	3	2	90	89	131	P8	140
DATA6	4	4	91	91	132	P10	139
DATA5	6	6	92	95	133	R12	138
DATA4	7	7	95	96	134	R13	136
DATA3	8	8	97	97	135	P13	135
DATA2	9	9	99	98	137	R14	133
DATA1	13	13	4	4	138	N15	132
DATA0	14	14	5	5	140	K13	129
SDOUT *(3)*	79	78	79	79	23	P4	97
TDI *(4)*	55	45 *(5)*	54	–	96	–	17
TDO *(4)*	27	27 *(5)*	18	–	18	–	102
TCK *(4)*, *(6)*	72	44 *(5)*	72	–	88	–	27
TMS *(4)*	20	43 *(5)*	11	–	86	–	29
TRST *(7)*	52	52 *(8)*	50	–	71	–	45
Dedicated Inputs *(10)*	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
VCCIO	–	–	–	–	16, 40, 60, 69, 91, 112, 122, 141	–	23, 47, 57, 69, 79, 104, 127, 137, 149, 159

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
nSP *(2)*	120	1	R15	207	207	5
MSEL0 *(2)*	117	3	T15	4	4	21
MSEL1 *(2)*	84	38	T3	49	49	33
nSTATUS *(2)*	37	83	B3	108	108	124
nCONFIG *(2)*	40	81	C3	103	103	107
DCLK *(2)*	1	120	C15	158	158	154
CONF_DONE *(2)*	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP *(2)*	A15	C14	237	237	W1	304
MSEL0 *(2)*	B14	G15	21	19	N1	26
MSEL1 *(2)*	R15	L15	40	38	H3	51
nSTATUS *(2)*	P2	L3	141	142	G19	178
nCONFIG *(2)*	R1	R4	117	120	B18	152
DCLK *(2)*	B2	C4	184	183	U18	230
CONF_DONE *(2)*	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDYnBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

Notes to tables:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a V_{CC} pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) SDOUT does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.