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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	84
Number of Logic Elements/Cells	672
Total RAM Bits	-
Number of I/O	152
Number of Gates	8000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	225-BGA
Supplier Device Package	225-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf8820abc225-2

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes

...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

Table 2. FLEX 8000 Package Options & I/O Pin Count *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

Note:
(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide-data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 3 shows FLEX 8000 performance and LE requirements for typical applications.

Table 3. FLEX 8000 Performance

Application	LEs Used	Speed Grade			Units
		A-2	A-3	A-4	
16-bit loadable counter	16	125	95	83	MHz
16-bit up/down counter	16	125	95	83	MHz
24-bit accumulator	24	87	67	58	MHz
16-bit address decode	4	4.2	4.9	6.3	ns
16-to-1 multiplexer	10	6.6	7.9	9.5	ns

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

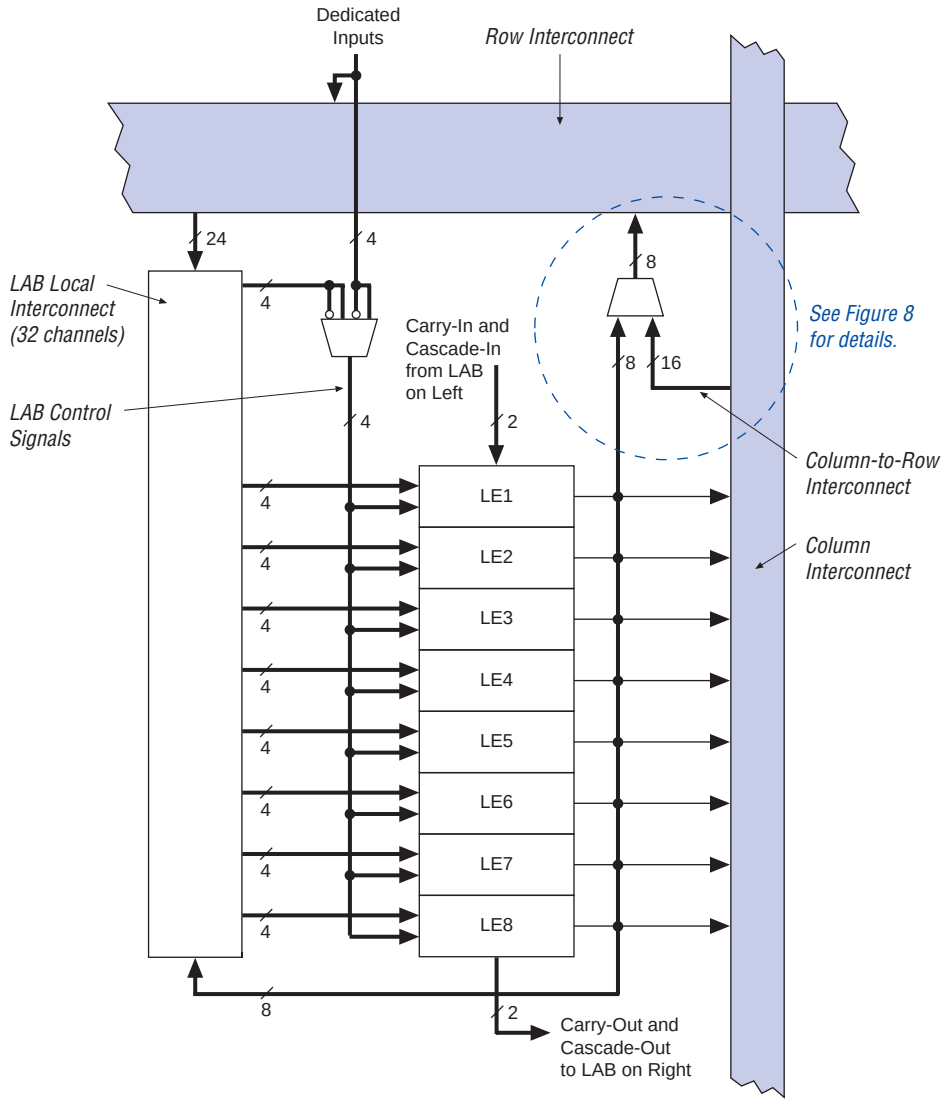
The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial configuration devices, or with data provided by a system controller. Altera offers the EPC1, EPC1213, EPC1064, and EPC1441 configuration devices, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32 K × 8 bit or larger configuration device, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation. For information on how to configure FLEX 8000 devices, go to the following documents:

- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block

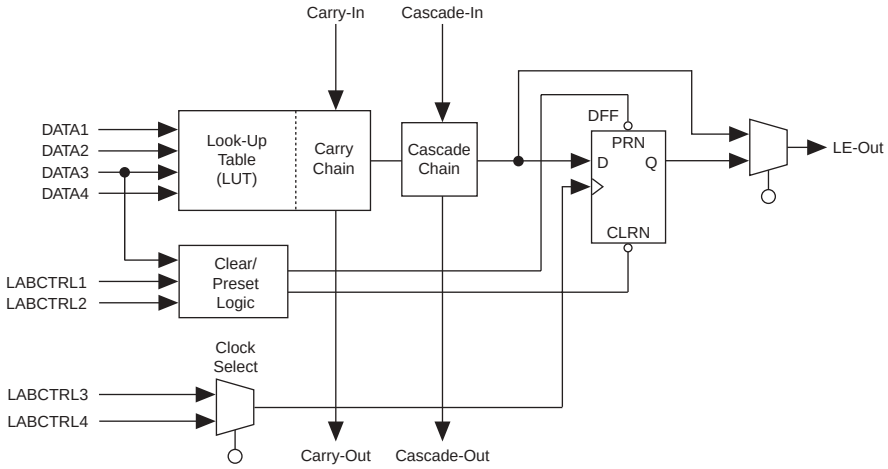


Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

Logic Element

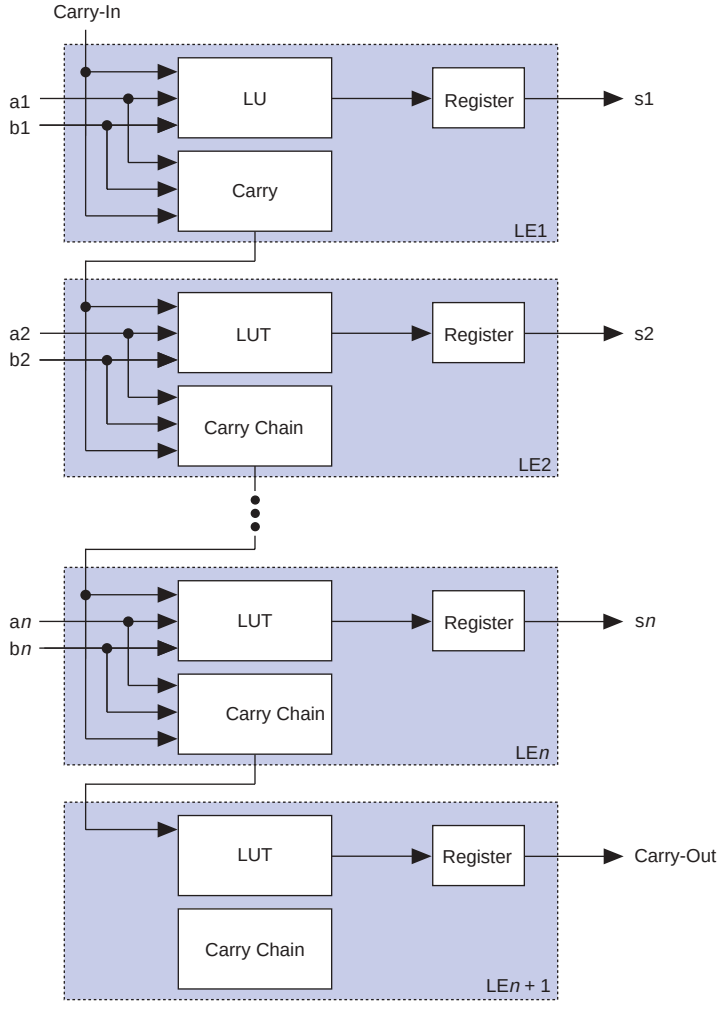
The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

Figure 3. FLEX 8000 LE



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

Figure 4. FLEX 8000 Carry Chain Operation



Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay as low as 0.6 ns per LE.

Normal Mode

The normal mode is suitable for general logic applications and wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in signal are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-Out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data output (Q) of the programmable register.

Arithmetic Mode

The arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 6, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output is the sum of three bits: a, b, and the carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports a cascade chain.

Up/Down Counter Mode

The up/down counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the clear and preset register control signals, without using the LUT resources.

Clearable Counter Mode

The clearable counter mode is similar to the up/down counter mode, but supports a synchronous clear instead of the up/down control; the clear function is substituted for the cascade-in signal in the up/down counter mode. Two 3-input LUTs are used: one generates the counter data, and the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, and the output of this multiplexer is ANDed with a synchronous clear.

MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. See Table 8 on page 26.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in Table 6.

Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

Figure 16. Output Drive Characteristics of 5.0-V FLEX 8000 Devices (Except EPF8282A)

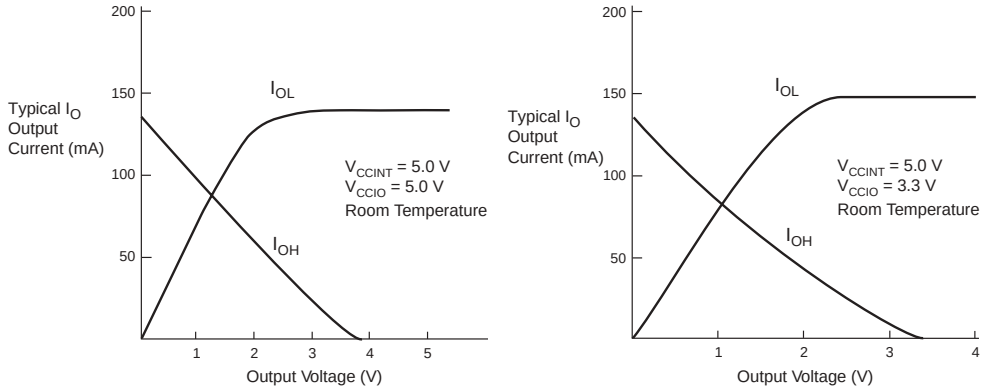


Figure 17 shows the typical output drive characteristics of 5.0-V EPF8282A devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

Figure 17. Output Drive Characteristics of EPF8282A Devices with 5.0-V V_{CCIO}

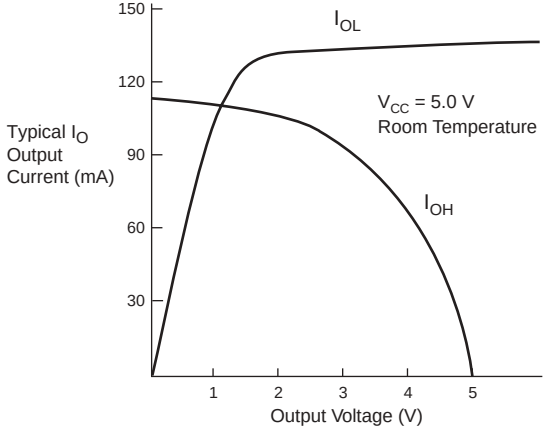
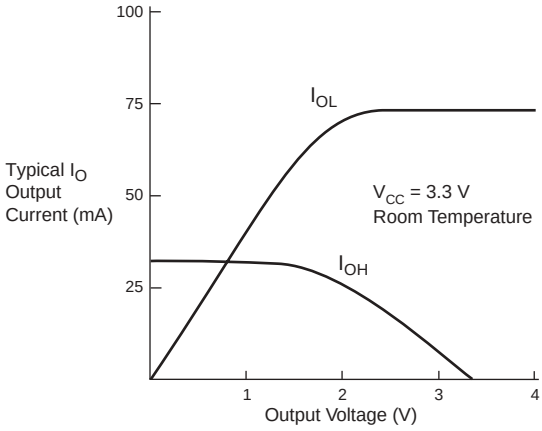


Figure 18 shows the typical output drive characteristics of EPF8282AV devices.

Figure 18. Output Drive Characteristics of EPF8282AV Devices



Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

Table 17. FLEX 8000 Internal Timing Parameters *Note (1)*	
Symbol	**Parameter**
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock; IOE register recovery time after asynchronous clear
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V C1 = 35 pF *(2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V C1 = 35 pF *(2)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF *(3)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF *(2)*
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF *(2)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF *(3)*

Table 18. FLEX 8000 LE Timing Parameters *Note (1)*	
Symbol	**Parameter**
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	LE register clock high time
t_{CL}	LE register clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock; LE register recovery time after asynchronous preset, clear, or load
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 19. FLEX 8000 Interconnect Timing Parameters Note (1)	
Symbol	**Parameter**
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay *(4)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay *(4)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 20. FLEX 8000 External Reference Timing Characteristics Note (5)	
Symbol	**Parameter**
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)*
t_{ODH}	Output data hold time after clock *(7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.
(4) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

Table 32. EPF8452A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_{C}		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_{H}	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 33. EPF8452A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 42. EPF81188A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 43. EPF81188A Interconnect Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Power Consumption

The supply power (P) for FLEX 8000 devices can be calculated with the following equation:

$$P = P_{INT} + P_{IO} = [(I_{CCSTANDBY} + I_{CCACTIVE}) \times V_{CC}] + P_{IO}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in Table 11 on page 28 and Table 15 on page 30. The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes.

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}} \times \frac{\mu A}{MHz \times LE}$$

The parameters in this equation are shown below:

$\mathbf{f_{MAX}}$ = Maximum operating frequency in MHz
N = Total number of logic cells used in the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock
K = Constant, shown in Table 50

Table 50. Values for Constant K

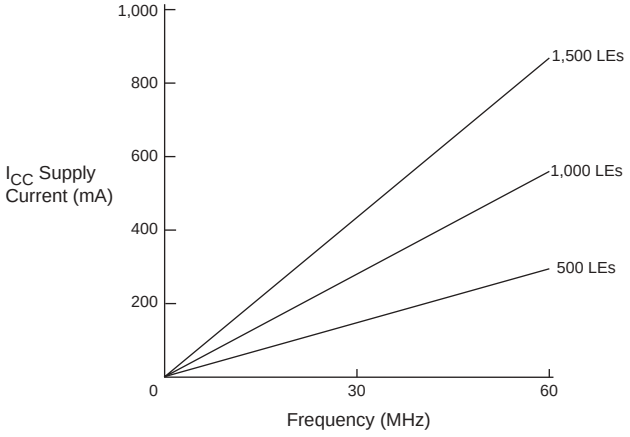
Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60

This calculation provides an I_{CC} estimate based on typical conditions with no output load. The actual I_{CC} value should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

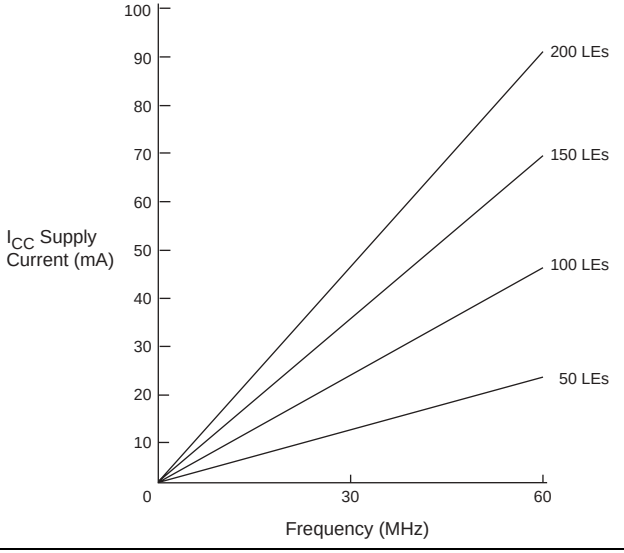
Figure 20 shows the relationship between I_{CC} and operating frequency for several LE utilization values.

Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices



3.3-V FLEX 8000 Devices



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. Table 51 shows the data source for each of the six configuration schemes.

Table 51. Data Source for Configuration

Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera configuration device
Active parallel up	APU	Parallel configuration device
Active parallel down	APD	Parallel configuration device
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Table 53. FLEX 8000 160-, 192- & 208-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	160-Pin PQFP EPF8452A	160-Pin PQFP EPF8636A	192-Pin PGA EPF8636A EPF8820A	208-Pin PQFP EPF8636A *(1)*	208-Pin PQFP EPF8820A *(1)*	208-Pin PQFP EPF81188A *(1)*
nSP *(2)*	120	1	R15	207	207	5
MSEL0 *(2)*	117	3	T15	4	4	21
MSEL1 *(2)*	84	38	T3	49	49	33
nSTATUS *(2)*	37	83	B3	108	108	124
nCONFIG *(2)*	40	81	C3	103	103	107
DCLK *(2)*	1	120	C15	158	158	154
CONF_DONE *(2)*	4	118	B15	153	153	138
nWS	30	89	C5	114	114	118
nRS	71	50	B5	66	116	121
RDCLK	73	48	C11	64	137	137
nCS	29	91	B13	116	145	142
CS	27	93	A16	118	148	144
RDYnBUSY	125	155	A8	201	127	128
CLKUSR	76	44	A10	59	134	134
ADD17	78	43	R5	57	43	46
ADD16	91	33	U3	43	42	45
ADD15	92	31	T5	41	41	44
ADD14	94	29	U4	39	40	39
ADD13	95	27	R6	37	39	37
ADD12	96	24	T6	31	35	36
ADD11	97	23	R7	30	33	31
ADD10	98	22	T7	29	31	30
ADD9	99	21	T8	28	29	29
ADD8	101	20	U9	24	25	26
ADD7	102	19	U10	23	23	25
ADD6	103	18	U11	22	21	24
ADD5	104	17	U12	21	19	18
ADD4	105	13	R12	14	14	17
ADD3	106	11	U14	12	13	16
ADD2	109	9	U15	10	11	10
ADD1	110	7	R13	8	10	9
ADD0	123	157	U16	203	9	8
DATA7	144	137	H17	178	178	177
DATA6	150	132	G17	172	176	175
DATA5	152	129	F17	169	174	172

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP *(2)*	A15	C14	237	237	W1	304
MSEL0 *(2)*	B14	G15	21	19	N1	26
MSEL1 *(2)*	R15	L15	40	38	H3	51
nSTATUS *(2)*	P2	L3	141	142	G19	178
nCONFIG *(2)*	R1	R4	117	120	B18	152
DCLK *(2)*	B2	C4	184	183	U18	230
CONF_DONE *(2)*	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDYnBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
DATA4	A5	C7	198	194	W16	248
DATA3	B5	D7	196	193	W17	246
DATA2	E6	B5	194	190	V16	243
DATA1	D5	A3	191	189	U16	241
DATA0	C4	A2	189	187	V17	239
SDOUT *(3)*	K1	N2	135	136	F19	169
TDI	F15 *(4)*	–	–	63 *(14)*	B1 *(14)*	80 *(14)*
TDO	J2 *(4)*	–	–	117	C17	149
TCK *(6)*	J14 *(4)*	–	–	116 *(14)*	A19 *(14)*	148 *(14)*
TMS	J12 *(4)*	–	–	64 *(14)*	C2 *(14)*	81 *(14)*
TRST *(7)*	P14	–	–	115 *(14)*	A18 *(14)*	145 *(14)*
Dedicated Inputs *(10)*	F4, L1, K12, E15	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
VCCINT (5.0 V)	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209, 236	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO (5.0 V or 3.3 V)	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300

Notes to tables:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* for more information.
(2) This pin is a dedicated pin and is not available as a user I/O pin.
(3) SDOUT will drive out during configuration. After configuration, it may be used as a user I/O pin. By default, the MAX+PLUS II software will not use SDOUT as a user I/O pin; the user can override the MAX+PLUS II software and use SDOUT as a user I/O pin.
(4) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(5) JTAG pins are available for EPF8636A devices only. These pins are dedicated user I/O pins.
(6) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(7) TRST is a dedicated input pin for JTAG use. This pin must be grounded if JTAG BST is not used.
(8) Pin 52 is a V_{CC} pin on EPF8452A devices only.
(9) The user I/O pin count includes dedicated input pins and all I/O pins.
(10) Unused dedicated inputs should be tied to ground on the board.
(11) SDOUT does not exist in the EPF8636GC192 device.
(12) These pins are no connect (N.C.) pins for EPF8636A devices only. They are user I/O pins in EPF8820A devices.
(13) EPF8636A devices have 132 user I/O pins; EPF8820A devices have 148 user I/O pins.
(14) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TDI, TCK, TMS, and TRST should be tied to GND.

Revision History

The information contained in the *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 supersedes information published in previous versions. The *FLEX 8000 Programmable Logic Device Family Data Sheet* version 11.1 contains the following change: minor textual updates.