Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

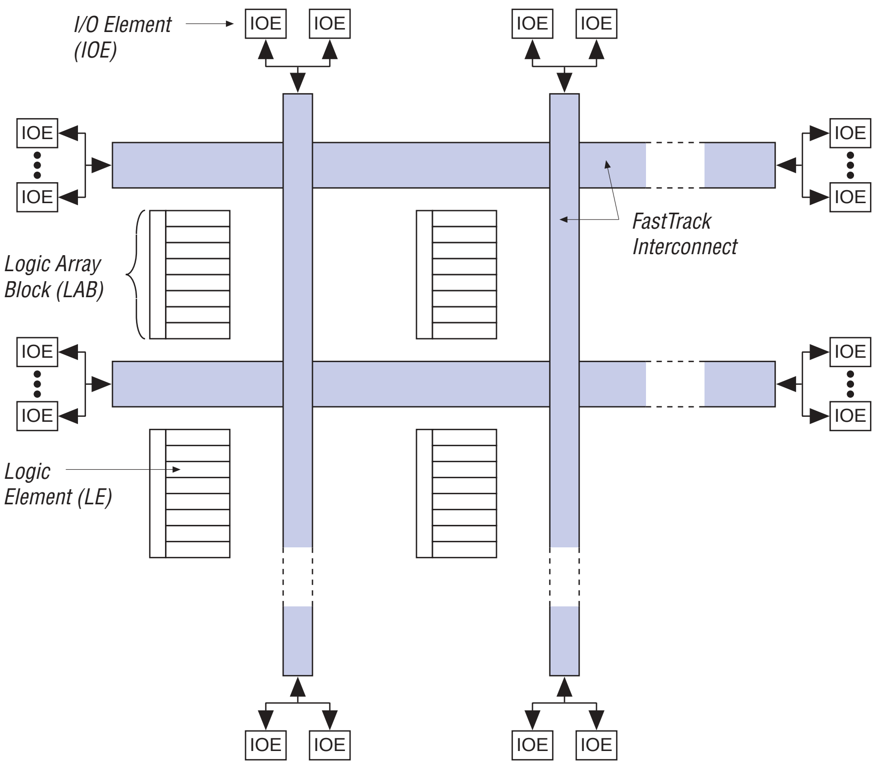
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	84
Number of Logic Elements/Cells	672
Total RAM Bits	-
Number of I/O	152
Number of Gates	8000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf8820aqc208-4

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram

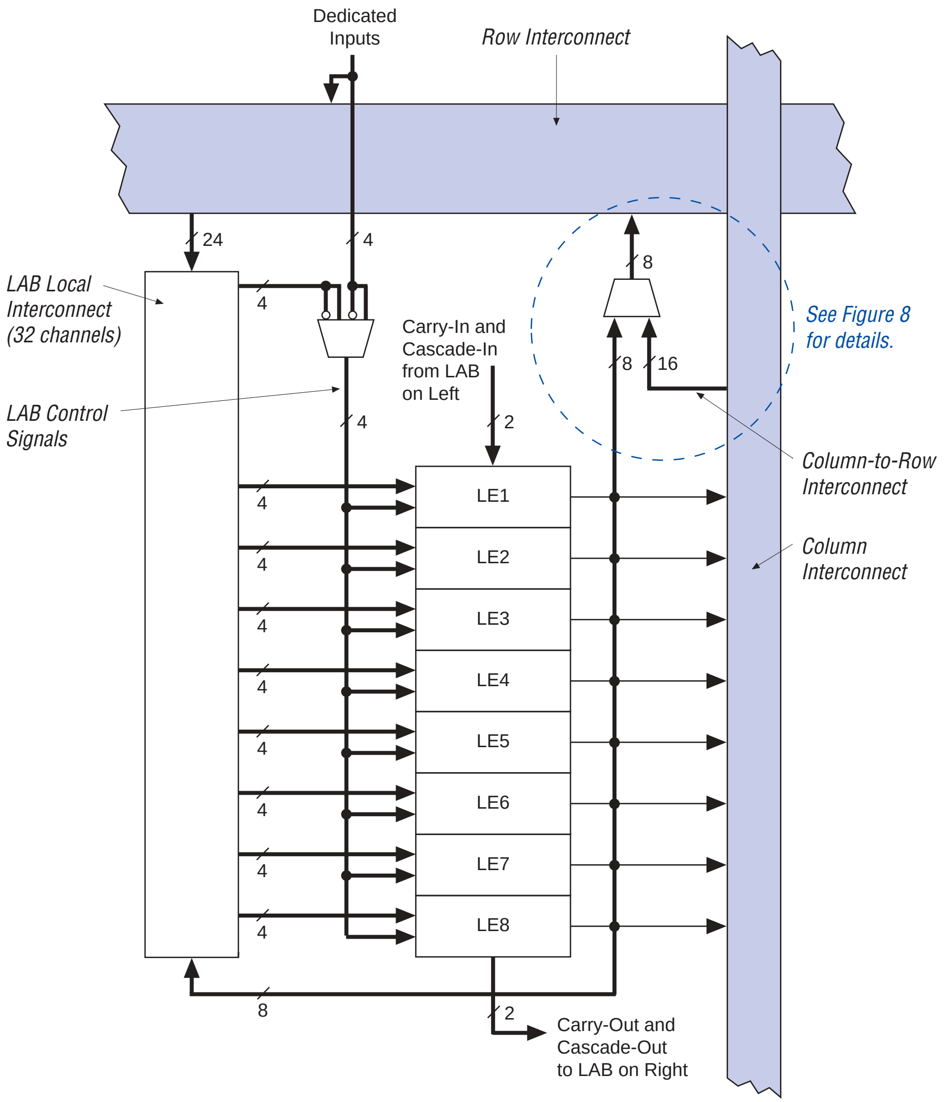


Signal interconnections within FLEX 8000 devices and between device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Array Block

A logic array block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 2 shows a block diagram of the FLEX 8000 LAB.

Figure 2. FLEX 8000 Logic Array Block

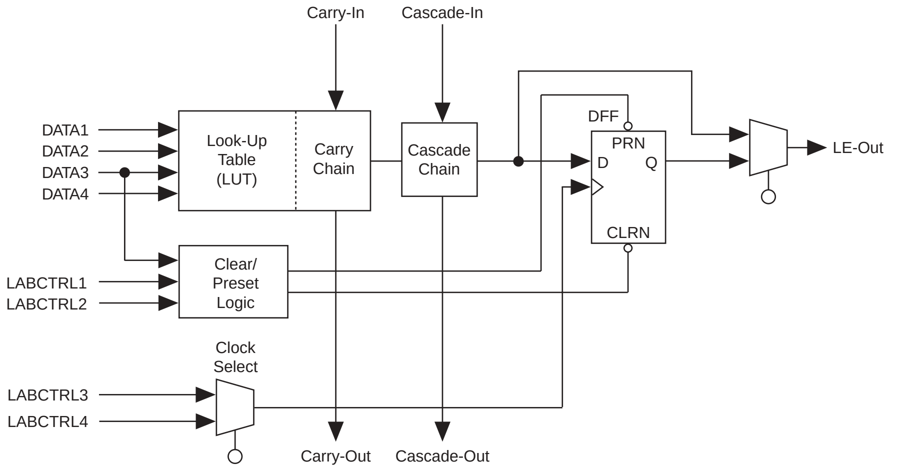


Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

Figure 3. FLEX 8000 LE



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce routing flexibility. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

Carry Chain

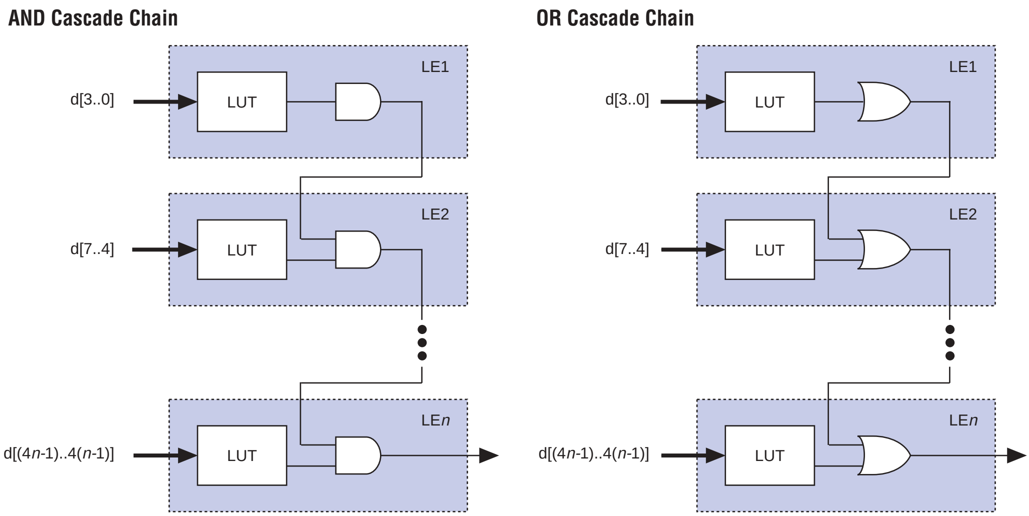
The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 4 shows how an n-bit full adder can be implemented in $n + 1$ LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to another LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 5. FLEX 8000 Cascade Chain Operation



LE Operating Modes

The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

Logic for the programmable register's clear and preset functions is controlled by the `DATA3`, `LABCTRL1`, and `LABCTRL2` inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that `LABCTRL1` implements an asynchronous load. The data to be loaded is driven to `DATA3`; when `LABCTRL1` is asserted, `DATA3` is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Asynchronous Clear

A register is cleared by one of the two LABCTRL signals. When the CLRn port receives a low signal, the register is set to zero.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load or an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRLl asynchronously loads a 1 into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Clear & Preset

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. The DATA3 input is tied to VCC; therefore, asserting LABCTRL1 asynchronously loads a 1 into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear.

Asynchronous Load with Preset

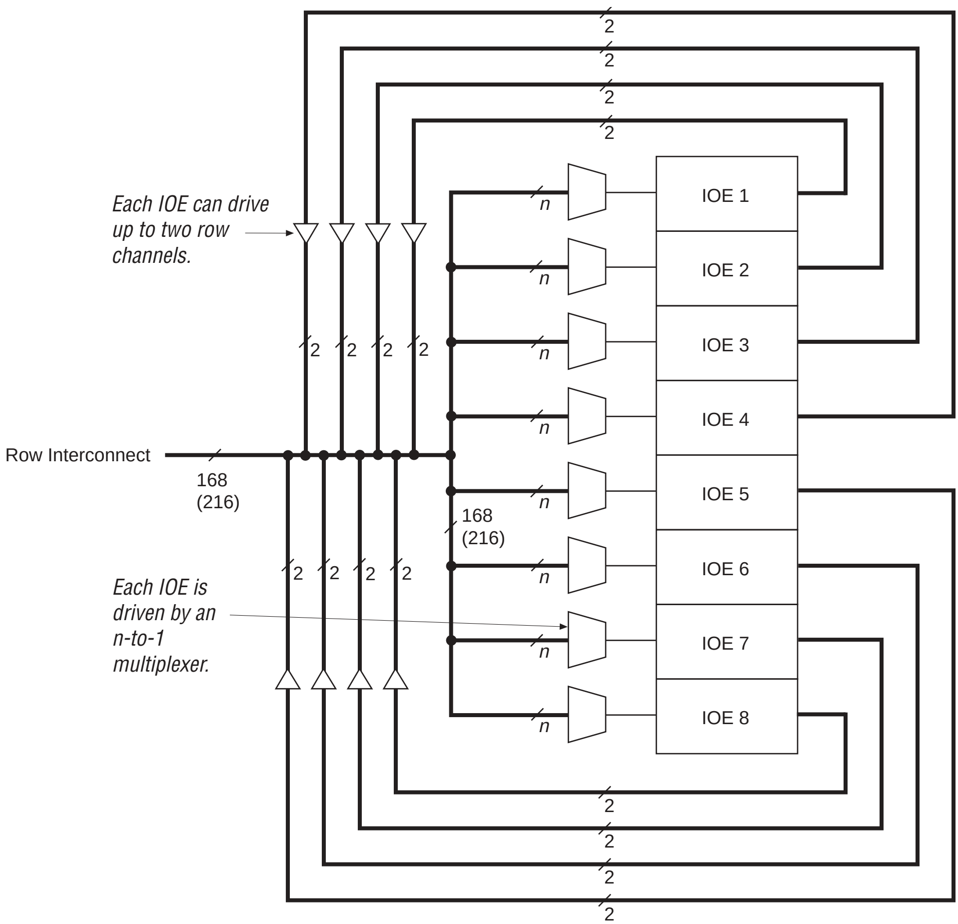
When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 clears the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives the DATA3 signal to account for the inversion of the register's output.

Asynchronous Load without Clear or Preset

When implementing an asynchronous load without the clear or preset, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

Figure 11. FLEX 8000 Row-to-IOE Connections

Numbers in parentheses are for EPF81500A devices. See Note (1).



Note:

(1) n = 13 for EPF8282A and EPF8282AV devices.
n = 21 for EPF8452A, EPF8636A, EPF8820A, and EPF81188A devices.
n = 27 for EPF81500A devices.

Column-to-IOE Connections

Two IOEs are located at the top and bottom of the column channels (see Figure 12). When an IOE is used as an input, it can drive up to two separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

The instruction register length for FLEX 8000 devices is three bits. Table 7 shows the boundary-scan register length for FLEX 8000 devices.

Table 7. FLEX 8000 Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPF8282A, EPF8282AV	273
EPF8636A	417
EPF8820A	465
EPF81500A	645

FLEX 8000 devices that support JTAG include weak pull-ups on the JTAG pins. Figure 14 shows the timing requirements for the JTAG signals.

Figure 14. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Waveforms

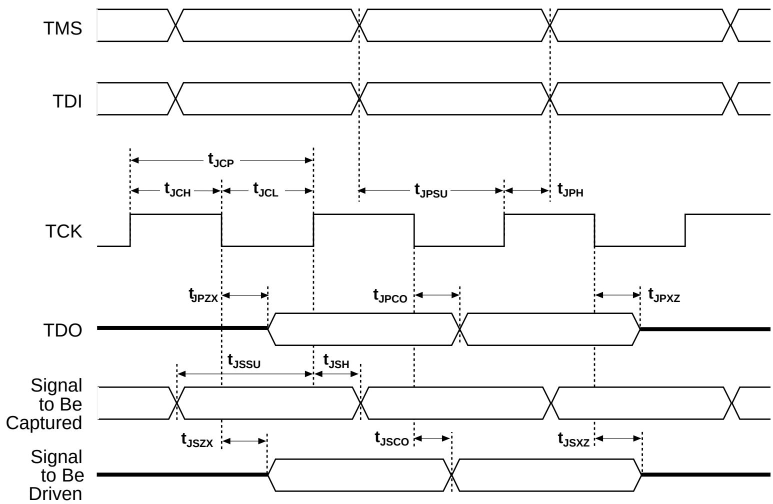


Table 8 shows the timing parameters and values for EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices.

Table 15. FLEX 8000 3.3-V Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA DC *(5)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(5)*			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load *(6)*		0.3	10	mA

Table 16. FLEX 8000 3.3-V Device Capacitance *Note (7)*

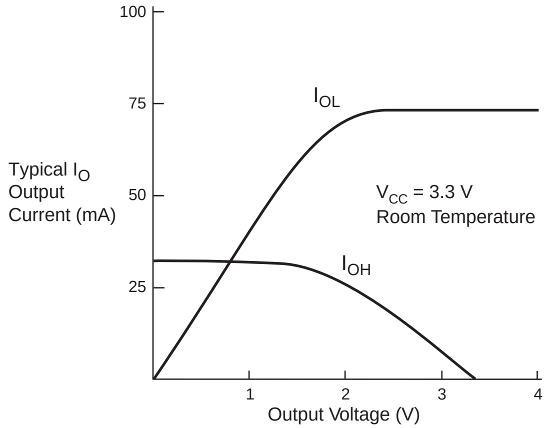
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(4) These values are specified in Table 14 on page 29.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

Figure 18. Output Drive Characteristics of EPF8282AV Devices



Timing Model

The continuous, high-performance FastTrack Interconnect routing structure ensures predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

Tables 17 through 20 describe the FLEX 8000 timing parameters and their symbols.

Table 21. FLEX 8000 Timing Model Interconnect Paths

Source	Destination	Total Delay
LE-Out	LE in same LAB	t_{LOCAL}
LE-Out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-Out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-Out	IOE on column	t_{COL}
LE-Out	IOE on row	t_{ROW}
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Tables 22 through 49 show the FLEX 8000 internal and external timing parameters.

Table 22. EPF8282A Internal I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		–		–		–	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 26. EPF8282AV I/O Element Timing Parameters					
Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{IOD}		0.9		2.2	ns
t_{IOC}		1.9		2.0	ns
t_{IOE}		1.9		2.0	ns
t_{IOCO}		1.0		2.0	ns
t_{IOCOMB}		0.1		0.0	ns
t_{IOSU}	1.8		2.8		ns
t_{IOH}	0.0		0.2		ns
t_{IOCLR}		1.2		2.3	ns
t_{IN}		1.7		3.4	ns
t_{OD1}		1.7		4.1	ns
t_{OD2}		–		–	ns
t_{OD3}		5.2		7.1	ns
t_{XZ}		1.8		4.3	ns
t_{ZX1}		1.8		4.3	ns
t_{ZX2}		–		–	ns
t_{ZX3}		5.3		8.3	ns

Table 27. EPF8282AV Interconnect Timing Parameters					
Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
$t_{LABCASC}$		0.4		1.3	ns
$t_{LABCARRY}$		0.4		0.8	ns
t_{LOCAL}		0.8		1.5	ns
t_{ROW}		4.2		6.3	ns
t_{COL}		2.5		3.8	ns
t_{DIN_C}		5.5		8.0	ns
t_{DIN_D}		7.2		10.8	ns
t_{DIN_IO}		5.5		9.0	ns

Table 36. EPF8636A LE Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_C		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_H	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 37. EPF8636A External Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$\mathbf{t_{DRR}}$		16.0		20.0		25.0	ns
$\mathbf{t_{ODH}}$	1.0		1.0		1.0		ns

Table 40. EPF8820A LE Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 41. EPF8820A External Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$\mathbf{t_{DRR}}$		16.0		20.0		25.0	ns
$\mathbf{t_{ODH}}$	1.0		1.0		1.0		ns

Table 44. EPF81188A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 45. EPF81188A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$\mathbf{t_{DRR}}$		16.0		20.0		25.0	ns
$\mathbf{t_{ODH}}$	1.0		1.0		1.0		ns

Table 46. EPF81500A I/O Element Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 47. EPF81500A Interconnect Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		8.2		8.2		8.7	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 48. EPF81500A LE Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 49. EPF81500A External Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$\mathbf{t_{DRR}}$		16.1		20.1		25.1	ns
$\mathbf{t_{ODH}}$	1.0		1.0		1.0		ns

Device Pin-Outs

Tables 52 through 54 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
nSP *(2)*	75	75	75	76	110	R1	1
MSEL0 *(2)*	74	74	74	75	109	P2	2
MSEL1 *(2)*	53	53	51	51	72	A1	44
nSTATUS *(2)*	32	32	24	25	37	C13	82
nCONFIG *(2)*	33	33	25	26	38	A15	81
DCLK *(2)*	10	10	100	100	143	P14	125
CONF_DONE *(2)*	11	11	1	1	144	N13	124
nWS	30	30	22	23	33	F13	87
nRS	48	48	42	45	31	C6	89
RDCLK	49	49	45	46	12	B5	110
nCS	29	29	21	22	4	D15	118
CS	28	28	19	21	3	E15	121
RDYnBUSY	77	77	77	78	20	P3	100
CLKUSR	50	50	47	47	13	C5	107
ADD17	51	51	49	48	75	B4	40
ADD16	36	55	28	54	76	E2	39
ADD15	56	56	55	55	77	D1	38
ADD14	57	57	57	57	78	E1	37
ADD13	58	58	58	58	79	F3	36
ADD12	60	60	59	60	83	F2	32
ADD11	61	61	60	61	85	F1	30
ADD10	62	62	61	62	87	G2	28
ADD9	63	63	62	64	89	G1	26
ADD8	64	64	64	65	92	H1	22
ADD7	65	65	65	66	94	H2	20
ADD6	66	66	66	67	95	J1	18
ADD5	67	67	67	68	97	J2	16
ADD4	69	69	68	70	102	K2	11
ADD3	70	70	69	71	103	K1	10
ADD2	71	71	71	72	104	K3	8
ADD1	76	72	76	73	105	M1	7

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	225-Pin BGA EPF8820A	232-Pin PGA EPF81188A	240-Pin PQFP EPF81188A	240-Pin PQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500A
nSP *(2)*	A15	C14	237	237	W1	304
MSEL0 *(2)*	B14	G15	21	19	N1	26
MSEL1 *(2)*	R15	L15	40	38	H3	51
nSTATUS *(2)*	P2	L3	141	142	G19	178
nCONFIG *(2)*	R1	R4	117	120	B18	152
DCLK *(2)*	B2	C4	184	183	U18	230
CONF_DONE *(2)*	A1	G3	160	161	M16	204
nWS	L4	P1	133	134	F18	167
nRS	K5	N1	137	138	G18	171
RDCLK	F1	G2	158	159	M17	202
nCS	D1	E2	166	167	N16	212
CS	C1	E3	169	170	N18	215
RDYnBUSY	J3	K2	146	147	J17	183
CLKUSR	G2	H2	155	156	K19	199
ADD17	M14	R15	58	56	E3	73
ADD16	L12	T17	56	54	E2	71
ADD15	M15	P15	54	52	F4	69
ADD14	L13	M14	47	45	G1	60
ADD13	L14	M15	45	43	H2	58
ADD12	K13	M16	43	41	H1	56
ADD11	K15	K15	36	34	J3	47
ADD10	J13	K17	34	32	K3	45
ADD9	J15	J14	32	30	K4	43
ADD8	G14	J15	29	27	L1	34
ADD7	G13	H17	27	25	L2	32
ADD6	G11	H15	25	23	M1	30
ADD5	F14	F16	18	16	N2	20
ADD4	E13	F15	16	14	N3	18
ADD3	D15	F14	14	12	N4	16
ADD2	D14	D15	7	5	U1	8
ADD1	E12	B17	5	3	U2	6
ADD0	C15	C15	3	1	V1	4
DATA7	A7	A7	205	199	W13	254
DATA6	D7	D8	203	197	W14	252
DATA5	A6	B7	200	196	W15	250