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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 84 |
| Number of Logic Elements/Cells | 672 |
| Total RAM Bits | - |
| Number of I/O | 152 |
| Number of Gates | 8000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epf8820atc144-3 |

| | | | | | | |
|---|---|---|---|---|---|---|
| JTAG BST circuitry | Yes | No | Yes | Yes | No | Yes |

## ...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

*Table 2. FLEX 8000 Package Options & I/O Pin Count* *Note (1)*

| Device | 84-Pin PLCC | 100-Pin TQFP | 144-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 225-Pin BGA | 232-Pin PGA | 240-Pin PQFP | 280-Pin PGA | 304-Pin RQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPF8282A | 68 | 78 | | | | | | | | | | |
| EPF8282AV | | 78 | | | | | | | | | | |
| EPF8452A | 68 | 68 | | 120 | 120 | | | | | | | |
| EPF8636A | 68 | | | 118 | | 136 | 136 | | | | | |
| EPF8820A | | | 112 | 120 | | 152 | 152 | 152 | | | | |
| EPF81188A | | | | | | | 148 | | 184 | 184 | | |
| EPF81500A | | | | | | | | | | 181 | 208 | 208 |

*Note:*
(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

## General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing (DSP), wide-data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 3 shows FLEX 8000 performance and LE requirements for typical applications.

*Table 3. FLEX 8000 Performance*

| Application | LEs Used | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | A-2 | A-3 | A-4 | |
| 16-bit loadable counter | 16 | 125 | 95 | 83 | MHz |
| 16-bit up/down counter | 16 | 125 | 95 | 83 | MHz |
| 24-bit accumulator | 24 | 87 | 67 | 58 | MHz |
| 16-bit address decode | 4 | 4.2 | 4.9 | 6.3 | ns |
| 16-to-1 multiplexer | 10 | 6.6 | 7.9 | 9.5 | ns |

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an industry-standard parallel EPROM or an Altera serial configuration devices, or with data provided by a system controller. Altera offers the EPC1, EPC1213, EPC1064, and EPC1441 configuration devices, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32 K × 8 bit or larger configuration device, or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation. For information on how to configure FLEX 8000 devices, go to the following documents:

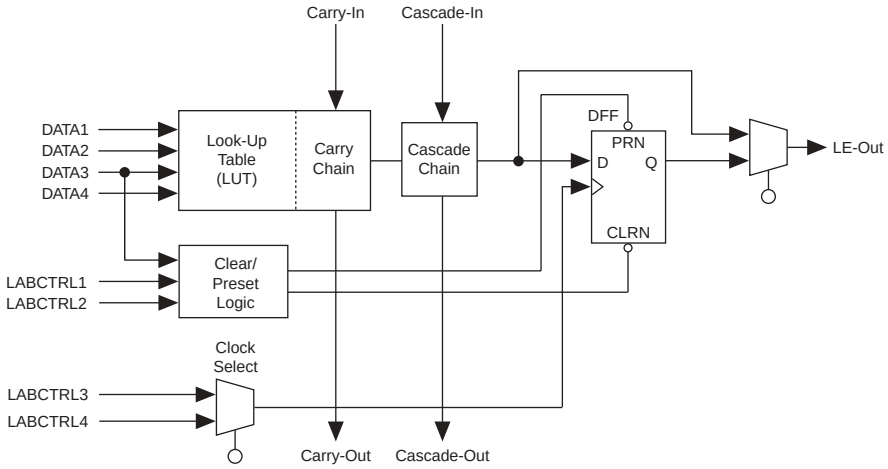
- *Configuration Devices for APEX & FLEX Devices Data Sheet*
- *BitBlaster Serial Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*
- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as clocks, and the other two for clear/preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global clock, clear, or preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global clock, clear, or preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB.

## Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a 4-input LUT, a programmable flipflop, a carry chain, and cascade chain. Figure 3 shows a block diagram of an LE.

*Figure 3. FLEX 8000 LE*




The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The clock, clear, and preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 4 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

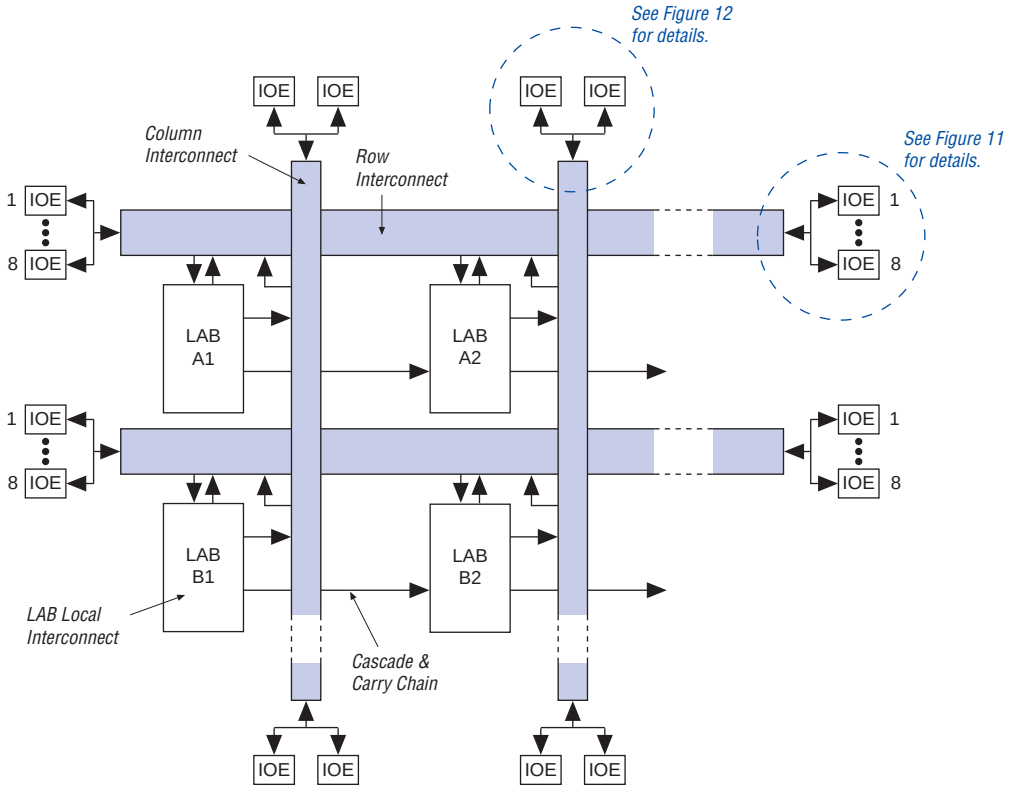
*Table 4. FLEX 8000 FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF8282A<br>EPF8282AV | 2 | 168 | 13 | 16 |
| EPF8452A | 2 | 168 | 21 | 16 |
| EPF8636A | 3 | 168 | 21 | 16 |
| EPF8820A | 4 | 168 | 21 | 16 |
| EPF81188A | 6 | 168 | 21 | 16 |
| EPF81500A | 6 | 216 | 27 | 16 |

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

***Figure 9. FLEX 8000 Device Interconnect Resources***

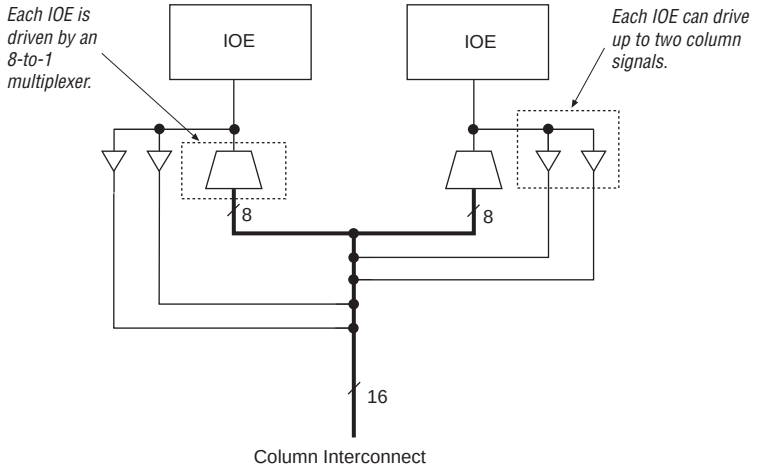
*Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.*




## I/O Element

An IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data that requires a fast setup time, or as an output register for data that requires fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect where appropriate. Figure 10 shows the IOE block diagram.

*Figure 12. FLEX 8000 Column-to-IOE Connections*




In addition to general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global clock, clear, and preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to invert signals automatically from the row and column interconnect when appropriate.

The clock, clear, and output enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or by internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four output enable signals (10 in EPF81500A devices), and up to two clock or clear signals. Figure 13 on page 22 shows how two output enable signals are shared with one clock and one clear signal.

### MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$. See Table 8 on page 26.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in Table 6.

*Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. |

*Table 8. JTAG Timing Parameters & Values*

| Symbol | Parameter | EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high-impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high-impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high-impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high-impedance | | 35 | ns |

For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

## Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Designers can use multiple test patterns to configure devices during all stages of the production flow.

*Table 10. FLEX 8000 5.0-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output buffers, 3.3-V operation | *(3)*, *(4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_I$ | Input voltage | | –0.5 | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 11. FLEX 8000 5.0-V Device DC Operating Conditions* *Notes (5), (6)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CCINT}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC *(7)*<br>$V_{CCIO}$ = 4.75 V | 2.4 | | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | $V_{CCIO}$ – 0.2 | | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC *(7)*<br>$V_{CCIO}$ = 4.75 V | | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC *(7)*<br>$V_{CCIO}$ = 3.00 V | | | 0.2 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or ground | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or ground | –40 | | 40 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = ground, no load | | 0.5 | 10 | mA |

*Table 12. FLEX 8000 5.0-V Device Capacitance* *Note (8)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

*Notes to tables:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum $V_{CC}$ rise time is 100 ms.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5.0 V.
(6) These values are specified in Table 10 on page 28.
(7) The $I_{OH}$ parameter refers to high-level TTL or CMOS output current; the $I_{OL}$ parameter refers to low-level TTL or CMOS output current.
(8) Capacitance is sample-tested only.

Tables 13 through 16 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 3.3-V FLEX 8000 devices.

*Table 13. FLEX 8000 3.3-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 5.3 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.3 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Plastic packages, under bias | | 135 | ° C |

*Table 14. FLEX 8000 3.3-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | *(3)* | 3.0 | 3.6 | V |
| $V_I$ | Input voltage | | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

| Table 19. FLEX 8000 Interconnect Timing Parameters Note (1) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs |
| $t_{LOCAL}$ | LAB local interconnect delay |
| $t_{ROW}$ | Row interconnect routing delay *(4)* |
| $t_{COL}$ | Column interconnect routing delay |
| $t_{DIN\_C}$ | Dedicated input to LE control delay |
| $t_{DIN\_D}$ | Dedicated input to LE data delay *(4)* |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay |

| Table 20. FLEX 8000 External Reference Timing Characteristics Note (5) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects *(6)* |
| $t_{ODH}$ | Output data hold time after clock *(7)* |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and external parameters specified by Altera. Internal timing parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(2) These values are specified in Table 10 on page 28 or Table 14 on page 29.
(3) For the $t_{OD3}$ and $t_{ZX3}$ parameters, $V_{CCIO}$ = 3.3 V or 5.0 V.
(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(5) External reference timing characteristics are factory-tested, worst-case values specified by Altera. A representative subset of signal paths is tested to approximate typical device applications.
(6) For more information on test conditions, see *Application Note 76 (Understanding FLEX 8000 Timing)*.
(7) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to global and non-global clocking, and for LE and I/O element registers.

The FLEX 8000 timing model shows the delays for various paths and functions in the circuit. See Figure 19. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 19 is expressed as a worst-case value in Tables 22 through 49. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance. Table 21 summarizes the interconnect paths shown in Figure 19.

For more information on timing parameters, go to *Application Note 76 (Understanding FLEX 8000 Timing)*.

*Table 24. EPF8282A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 25. EPF8282A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 15.8 | | 19.8 | | 24.8 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 28. EPF8282AV Logic Element Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{LUT}$ | | 3.2 | | 7.3 | ns |
| $t_{CLUT}$ | | 0.0 | | 1.4 | ns |
| $t_{RLUT}$ | | 1.5 | | 5.1 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.9 | | 2.8 | ns |
| $t_{CICO}$ | | 0.6 | | 1.5 | ns |
| $t_{CGEN}$ | | 0.7 | | 2.2 | ns |
| $t_{CGENR}$ | | 1.5 | | 3.7 | ns |
| $t_{C}$ | | 2.5 | | 4.7 | ns |
| $t_{CH}$ | 4.0 | | 6.0 | | ns |
| $t_{CL}$ | 4.0 | | 6.0 | | ns |
| $t_{CO}$ | | 0.6 | | 0.9 | ns |
| $t_{COMB}$ | | 0.6 | | 0.9 | ns |
| $t_{SU}$ | 1.2 | | 2.4 | | ns |
| $t_{H}$ | 1.5 | | 4.6 | | ns |
| $t_{PRE}$ | | 0.8 | | 1.3 | ns |
| $t_{CLR}$ | | 0.8 | | 1.3 | ns |

*Table 29. EPF8282AV External Timing Parameters*

| Symbol | Speed Grade | | | | Unit |
|---|---|---|---|---|---|
| | A-3 | | A-4 | | |
| | Min | Max | Min | Max | |
| $t_{DRR}$ | | 24.8 | | 50.1 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | ns |

*Table 42. EPF81188A I/O Element Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{IOD}$ | | 0.7 | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOE}$ | | 1.7 | | 1.8 | | 1.9 | ns |
| $t_{IOCO}$ | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | | 0.3 | | 0.2 | | 0.1 | ns |
| $t_{IOSU}$ | 1.4 | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | | 1.2 | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | | 1.5 | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | | 1.1 | | 1.4 | | 1.7 | ns |
| $t_{OD2}$ | | 1.6 | | 1.9 | | 2.2 | ns |
| $t_{OD3}$ | | 4.6 | | 4.9 | | 5.2 | ns |
| $t_{XZ}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX1}$ | | 1.4 | | 1.6 | | 1.8 | ns |
| $t_{ZX2}$ | | 1.9 | | 2.1 | | 2.3 | ns |
| $t_{ZX3}$ | | 4.9 | | 5.1 | | 5.3 | ns |

*Table 43. EPF81188A Interconnect Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LABCASC}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LABCARRY}$ | | 0.3 | | 0.3 | | 0.4 | ns |
| $t_{LOCAL}$ | | 0.5 | | 0.6 | | 0.8 | ns |
| $t_{ROW}$ | | 5.0 | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | | 3.0 | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | | 5.0 | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | | 7.0 | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | | 5.0 | | 5.0 | | 5.5 | ns |

*Table 44. EPF81188A LE Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 45. EPF81188A External Timing Parameters*

| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.0 | | 20.0 | | 25.0 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Table 48. EPF81500A LE Timing Parameters*

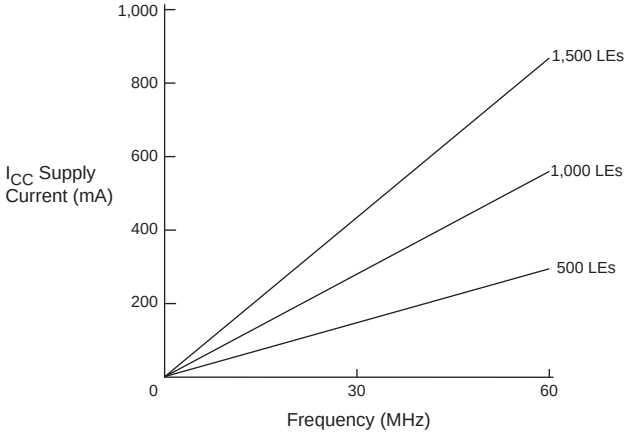
| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{LUT}$ | | 2.0 | | 2.5 | | 3.2 | ns |
| $t_{CLUT}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{RLUT}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{GATE}$ | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | | 0.4 | | 0.5 | | 0.7 | ns |
| $t_{CGENR}$ | | 0.9 | | 1.1 | | 1.5 | ns |
| $t_{C}$ | | 1.6 | | 2.0 | | 2.5 | ns |
| $t_{CH}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{CO}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | 0.8 | | 1.1 | | 1.2 | | ns |
| $t_{H}$ | 0.9 | | 1.1 | | 1.5 | | ns |
| $t_{PRE}$ | | 0.6 | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | | 0.6 | | 0.7 | | 0.8 | ns |

*Table 49. EPF81500A External Timing Parameters*

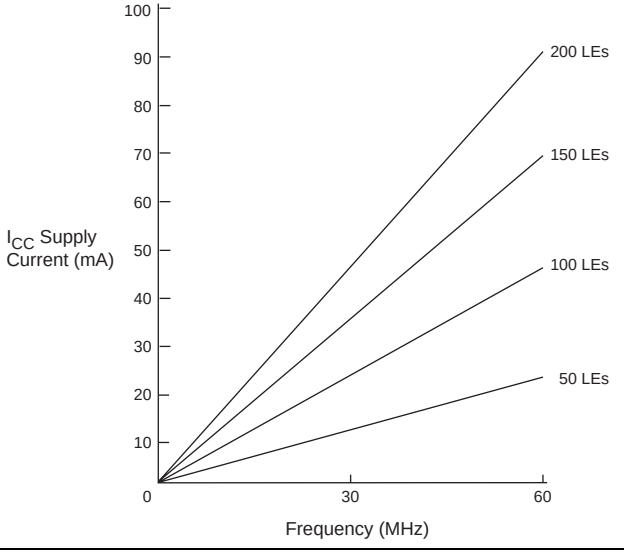
| Symbol | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | A-2 | | A-3 | | A-4 | | |
| | Min | Max | Min | Max | Min | Max | |
| $t_{DRR}$ | | 16.1 | | 20.1 | | 25.1 | ns |
| $t_{ODH}$ | 1.0 | | 1.0 | | 1.0 | | ns |

*Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency*

**5.0-V FLEX 8000 Devices**




**3.3-V FLEX 8000 Devices**




# Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

## Operating Modes

The FLEX 8000 architecture uses SRAM elements that require configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

## Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external configuration devices, and completing the loading process. The clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device. Table 51 shows the data source for each of the six configuration schemes.

*Table 51. Data Source for Configuration*

| Configuration Scheme | Acronym | Data Source |
|---|---|---|
| Active serial | AS | Altera configuration device |
| Active parallel up | APU | Parallel configuration device |
| Active parallel down | APD | Parallel configuration device |
| Passive serial | PS | Serial data path |
| Passive parallel synchronous | PPS | Intelligent host |
| Passive parallel asynchronous | PPA | Intelligent host |

*Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 84-Pin PLCC EPF8282A | 84-Pin PLCC EPF8452A EPF8636A | 100-Pin TQFP EPF8282A EPF8282AV | 100-Pin TQFP EPF8452A | 144-Pin TQFP EPF8820A | 160-Pin PGA EPF8452A | 160-Pin PQFP EPF8820A *(1)* |
|---|---|---|---|---|---|---|---|
| ADD0 | 78 | 76 | 78 | 77 | 106 | N3 | 6 |
| DATA7 | 3 | 2 | 90 | 89 | 131 | P8 | 140 |
| DATA6 | 4 | 4 | 91 | 91 | 132 | P10 | 139 |
| DATA5 | 6 | 6 | 92 | 95 | 133 | R12 | 138 |
| DATA4 | 7 | 7 | 95 | 96 | 134 | R13 | 136 |
| DATA3 | 8 | 8 | 97 | 97 | 135 | P13 | 135 |
| DATA2 | 9 | 9 | 99 | 98 | 137 | R14 | 133 |
| DATA1 | 13 | 13 | 4 | 4 | 138 | N15 | 132 |
| DATA0 | 14 | 14 | 5 | 5 | 140 | K13 | 129 |
| SDOUT *(3)* | 79 | 78 | 79 | 79 | 23 | P4 | 97 |
| TDI *(4)* | 55 | 45 *(5)* | 54 | – | 96 | – | 17 |
| TDO *(4)* | 27 | 27 *(5)* | 18 | – | 18 | – | 102 |
| TCK *(4)*, *(6)* | 72 | 44 *(5)* | 72 | – | 88 | – | 27 |
| TMS *(4)* | 20 | 43 *(5)* | 11 | – | 86 | – | 29 |
| TRST *(7)* | 52 | 52 *(8)* | 50 | – | 71 | – | 45 |
| Dedicated Inputs *(10)* | 12, 31, 54, 73 | 12, 31, 54, 73 | 3, 23, 53, 73 | 3, 24, 53, 74 | 9, 26, 82, 99 | C3, D14, N2, R15 | 14, 33, 94, 113 |
| VCCINT | 17, 38, 59, 80 | 17, 38, 59, 80 | 6, 20, 37, 56, 70, 87 | 9, 32, 49, 59, 82 | 8, 28, 70, 90, 111 | B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12 | 3, 24, 46, 92, 114, 160 |
| VCCIO | – | – | – | – | 16, 40, 60, 69, 91, 112, 122, 141 | – | 23, 47, 57, 69, 79, 104, 127, 137, 149, 159 |

*Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 1 of 3)*

| Pin Name | 225-Pin BGA EPF8820A | 232-Pin PGA EPF81188A | 240-Pin PQFP EPF81188A | 240-Pin PQFP EPF81500A | 280-Pin PGA EPF81500A | 304-Pin RQFP EPF81500A |
|---|---|---|---|---|---|---|
| nSP *(2)* | A15 | C14 | 237 | 237 | W1 | 304 |
| MSEL0 *(2)* | B14 | G15 | 21 | 19 | N1 | 26 |
| MSEL1 *(2)* | R15 | L15 | 40 | 38 | H3 | 51 |
| nSTATUS *(2)* | P2 | L3 | 141 | 142 | G19 | 178 |
| nCONFIG *(2)* | R1 | R4 | 117 | 120 | B18 | 152 |
| DCLK *(2)* | B2 | C4 | 184 | 183 | U18 | 230 |
| CONF_DONE *(2)* | A1 | G3 | 160 | 161 | M16 | 204 |
| nWS | L4 | P1 | 133 | 134 | F18 | 167 |
| nRS | K5 | N1 | 137 | 138 | G18 | 171 |
| RDCLK | F1 | G2 | 158 | 159 | M17 | 202 |
| nCS | D1 | E2 | 166 | 167 | N16 | 212 |
| CS | C1 | E3 | 169 | 170 | N18 | 215 |
| RDYnBUSY | J3 | K2 | 146 | 147 | J17 | 183 |
| CLKUSR | G2 | H2 | 155 | 156 | K19 | 199 |
| ADD17 | M14 | R15 | 58 | 56 | E3 | 73 |
| ADD16 | L12 | T17 | 56 | 54 | E2 | 71 |
| ADD15 | M15 | P15 | 54 | 52 | F4 | 69 |
| ADD14 | L13 | M14 | 47 | 45 | G1 | 60 |
| ADD13 | L14 | M15 | 45 | 43 | H2 | 58 |
| ADD12 | K13 | M16 | 43 | 41 | H1 | 56 |
| ADD11 | K15 | K15 | 36 | 34 | J3 | 47 |
| ADD10 | J13 | K17 | 34 | 32 | K3 | 45 |
| ADD9 | J15 | J14 | 32 | 30 | K4 | 43 |
| ADD8 | G14 | J15 | 29 | 27 | L1 | 34 |
| ADD7 | G13 | H17 | 27 | 25 | L2 | 32 |
| ADD6 | G11 | H15 | 25 | 23 | M1 | 30 |
| ADD5 | F14 | F16 | 18 | 16 | N2 | 20 |
| ADD4 | E13 | F15 | 16 | 14 | N3 | 18 |
| ADD3 | D15 | F14 | 14 | 12 | N4 | 16 |
| ADD2 | D14 | D15 | 7 | 5 | U1 | 8 |
| ADD1 | E12 | B17 | 5 | 3 | U2 | 6 |
| ADD0 | C15 | C15 | 3 | 1 | V1 | 4 |
| DATA7 | A7 | A7 | 205 | 199 | W13 | 254 |
| DATA6 | D7 | D8 | 203 | 197 | W14 | 252 |
| DATA5 | A6 | B7 | 200 | 196 | W15 | 250 |