Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	84
Number of Logic Elements/Cells	672
Total RAM Bits	-
Number of I/O	112
Number of Gates	8000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epf8820atc144-4

JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes

...and More Features

- Peripheral register for fast setup and clock-to-output delay
- Fabricated on an advanced SRAM process
- Available in a variety of packages with 84 to 304 pins (see Table 2)
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system for Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and Veribest

Table 2. FLEX 8000 Package Options & I/O Pin Count *Note (1)*

Device	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	225-Pin BGA	232-Pin PGA	240-Pin PQFP	280-Pin PGA	304-Pin RQFP
EPF8282A	68	78										
EPF8282AV		78										
EPF8452A	68	68		120	120							
EPF8636A	68			118		136	136					
EPF8820A			112	120		152	152	152				
EPF81188A							148		184	184		
EPF81500A										181	208	208

Note:

(1) FLEX 8000 device package types include plastic J-lead chip carrier (PLCC), thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), ball-grid array (BGA), and pin-grid array (PGA) packages.

General Description

Altera's Flexible Logic Element MatriX (FLEX®) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The FLEX 8000 device family is ideal for a variety of applications because it combines the fine-grained architecture and high register count characteristics of FPGAs with the high speed and predictable interconnect delays of EPLDs. Logic is implemented in LEs that include compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices contain an optimized microprocessor interface that permits the microprocessor to configure FLEX 8000 devices serially, in parallel, synchronously, or asynchronously. The interface also enables the microprocessor to treat a FLEX 8000 device as memory and configure the device by writing to a virtual memory location, making it very easy for the designer to create configuration software.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

The MAX+PLUS II software interfaces easily with common gate array EDA tools for synthesis and simulation. For example, the MAX+PLUS II software can generate Verilog HDL files for simulation with tools such as Cadence Verilog-XL. Additionally, the MAX+PLUS II software contains EDA libraries that use device-specific features such as carry chains, which are used for fast counter and arithmetic functions. For instance, the Synopsys Design Compiler library supplied with the MAX+PLUS II development system includes DesignWare functions that are optimized for the FLEX 8000 architecture.

For more information on the MAX+PLUS II software, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

Functional Description

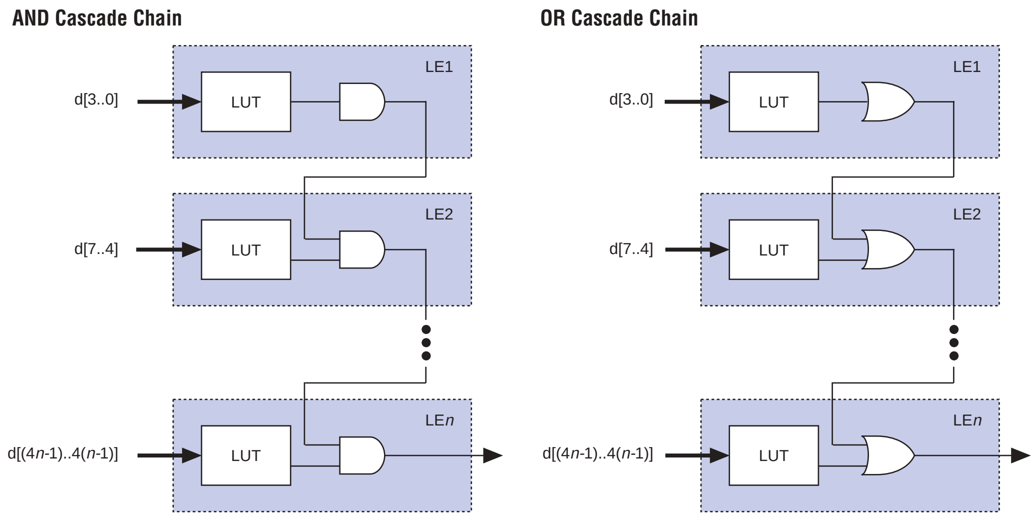
The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

Eight LEs are grouped together to form a logic array block (LAB). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry. Cascade chains longer than eight LEs are automatically implemented by linking LABs together. The last LE of an LAB cascades to the first LE of the next LAB.

Figure 5 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A-2 speed grade, the LE delay is 2.4 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 5. FLEX 8000 Cascade Chain Operation



LE Operating Modes

The FLEX 8000 LE can operate in one of four modes, each of which uses LE resources differently. See Figure 6. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide clock, clear, and preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Internal Tri-State Emulation

Internal tri-state emulation provides internal tri-stating without the limitations of a physical tri-state bus. In a physical tri-state bus, the tri-state buffers' output enable signals select the signal that drives the bus. However, if multiple output enable signals are active, contending signals can be driven onto the bus. Conversely, if no output enable signals are active, the bus will float. Internal tri-state emulation resolves contending tri-state buffers to a low value and floating buses to a high value, thereby eliminating these problems. The MAX+PLUS II software automatically implements tri-state bus functionality with a multiplexer.

Clear & Preset Logic Control

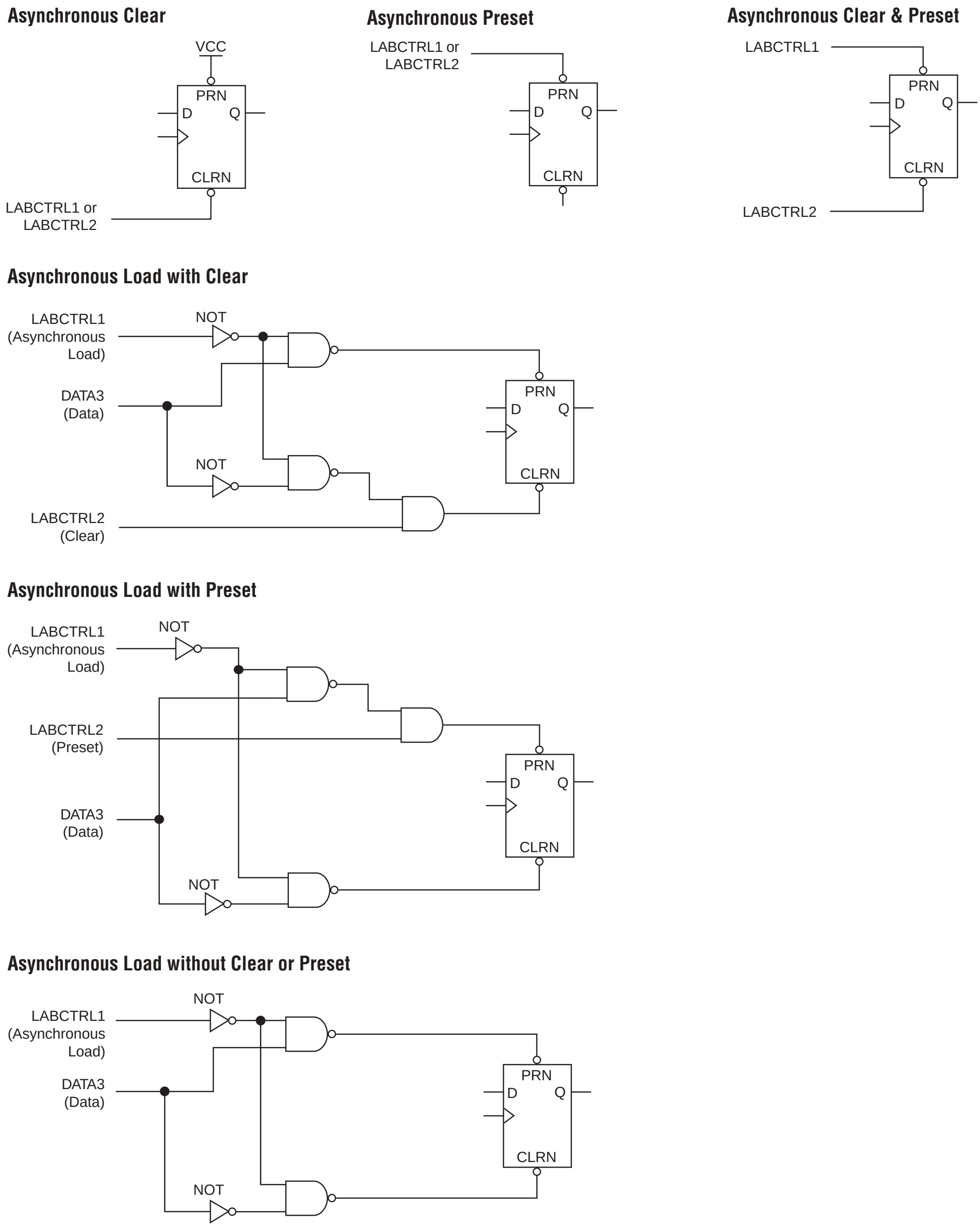
Logic for the programmable register's clear and preset functions is controlled by the `DATA3`, `LABCTRL1`, and `LABCTRL2` inputs to the LE. The clear and preset control structure of the LE is used to asynchronously load signals into a register. The register can be set up so that `LABCTRL1` implements an asynchronous load. The data to be loaded is driven to `DATA3`; when `LABCTRL1` is asserted, `DATA3` is loaded into the register.

During compilation, the MAX+PLUS II Compiler automatically selects the best control signal implementation. Because the clear and preset functions are active-low, the Compiler automatically assigns a logic high to an unused clear or preset.

The clear and preset logic is implemented in one of the following six asynchronous modes, which are chosen during design entry. LPM functions that use registers will automatically use the correct asynchronous mode. See Figure 7.

- Clear only
- Preset only
- Clear and preset
- Load with clear
- Load with preset
- Load without clear or preset

Figure 7. FLEX 8000 LE Asynchronous Clear & Preset Modes



Asynchronous Clear

A register is cleared by one of the two LABCTRL signals. When the CLRn port receives a low signal, the register is set to zero.

Asynchronous Preset

An asynchronous preset is implemented as either an asynchronous load or an asynchronous clear. If DATA3 is tied to VCC, asserting LABCTRLl asynchronously loads a 1 into the register. Alternatively, the MAX+PLUS II software can provide preset control by using the clear and inverting the input and output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is preset by only one of the two LABCTRL signals, the DATA3 input is not needed and can be used for one of the LE operating modes.

Asynchronous Clear & Preset

When implementing asynchronous clear and preset, LABCTRL1 controls the preset and LABCTRL2 controls the clear. The DATA3 input is tied to VCC; therefore, asserting LABCTRL1 asynchronously loads a 1 into the register, effectively presetting the register. Asserting LABCTRL2 clears the register.

Asynchronous Load with Clear

When implementing an asynchronous load with the clear, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear. LABCTRL2 implements the clear by controlling the register clear.

Asynchronous Load with Preset

When implementing an asynchronous load in conjunction with a preset, the MAX+PLUS II software provides preset control by using the clear and inverting the input and output of the register. Asserting LABCTRL2 clears the register, while asserting LABCTRL1 loads the register. The MAX+PLUS II software inverts the signal that drives the DATA3 signal to account for the inversion of the register's output.

Asynchronous Load without Clear or Preset

When implementing an asynchronous load without the clear or preset, LABCTRL1 implements the asynchronous load of DATA3 by controlling the register preset and clear.

Table 5 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 5. Row Sources of FLEX 8000 Peripheral Control Signals

Peripheral Control Signal	EPF8282A EPF8282AV	EPF8452A	EPF8636A	EPF8820A	EPF81188A	EPF81500A
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	–	–	–	–	–	Row B
OE5	–	–	–	–	–	Row C
OE6	–	–	–	–	–	Row D
OE7	–	–	–	–	–	Row D
OE8	–	–	–	–	–	Row E
OE9	–	–	–	–	–	Row F

Output Configuration

This section discusses slew-rate control and MultiVolt I/O interface operation for FLEX 8000 devices.

Slew-Rate Control

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise by slowing signal transitions, adding a maximum delay of 3.5 ns. The slow slew-rate setting affects only the falling edge of a signal. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

For more information on high-speed system design, go to *Application Note 75 (High-Speed Board Designs)*.

MultiVolt I/O Interface

The FLEX 8000 device architecture supports the MultiVolt I/O interface feature, which allows EPF81500A, EPF81188A, EPF8820A, and EPF8636A devices to interface with systems with differing supply voltages. These devices in all packages—except for EPF8636A devices in 84-pin PLCC packages—can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCINT` pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs.

The `VCCIO` pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the `VCCIO` pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. See Table 8 on page 26.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

The EPF8282A, EPF8282AV, EPF8636A, EPF8820A, and EPF81500A devices provide JTAG BST circuitry. FLEX 8000 devices with JTAG circuitry support the JTAG instructions shown in Table 6.

Table 6. EPF8282A, EPF8282AV, EPF8636A, EPF8820A & EPF81500A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.

Table 8. JTAG Timing Parameters & Values

Symbol	Parameter	EPF8282A EPF8282AV EPF8636A EPF8820A EPF81500A		Unit
		Min	Max	
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high-impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high-impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high-impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high-impedance		35	ns

For detailed information on JTAG operation in FLEX 8000 devices, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Generic Testing

Each FLEX 8000 device is functionally tested and specified by Altera. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Designers can use multiple test patterns to configure devices during all stages of the production flow.

Table 15. FLEX 8000 3.3-V Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA DC *(5)*	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(5)*			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or ground	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or ground	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = ground, no load *(6)*		0.3	10	mA

Table 16. FLEX 8000 3.3-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) The maximum V_{CC} rise time is 100 ms. V_{CC} must rise monotonically.
(4) These values are specified in Table 14 on page 29.
(5) The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to low-level TTL output current.
(6) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.
(7) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices. The output driver is compliant with ***PCI Local Bus Specification, Revision 2.2***.

Table 24. EPF8282A LE Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 25. EPF8282A External Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		15.8		19.8		24.8	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 28. EPF8282AV Logic Element Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{LUT}		3.2		7.3	ns
t_{CLUT}		0.0		1.4	ns
t_{RLUT}		1.5		5.1	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		0.9		2.8	ns
t_{CICO}		0.6		1.5	ns
t_{CGEN}		0.7		2.2	ns
t_{CGENR}		1.5		3.7	ns
t_{C}		2.5		4.7	ns
t_{CH}	4.0		6.0		ns
t_{CL}	4.0		6.0		ns
t_{CO}		0.6		0.9	ns
t_{COMB}		0.6		0.9	ns
t_{SU}	1.2		2.4		ns
t_{H}	1.5		4.6		ns
t_{PRE}		0.8		1.3	ns
t_{CLR}		0.8		1.3	ns

Table 29. EPF8282AV External Timing Parameters

Symbol	Speed Grade				Unit
	A-3		A-4		
	Min	Max	Min	Max	
t_{DRR}		24.8		50.1	ns
t_{ODH}	1.0		1.0		ns

Table 30. EPF8452A I/O Element Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		–		–		–	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		–		–		–	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 31. EPF8452A Interconnect Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
$t_{LABCASC}$		0.3		0.4		0.4	ns
$t_{LABCARRY}$		0.3		0.4		0.4	ns
t_{LOCAL}		0.5		0.5		0.7	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 32. EPF8452A LE Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{LUT}		2.0		2.3		3.0	ns
t_{CLUT}		0.0		0.2		0.1	ns
t_{RLUT}		0.9		1.6		1.6	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.9		0.8	ns
t_{CGENR}		0.9		1.4		1.5	ns
t_{C}		1.6		1.8		2.4	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.0		1.1		ns
t_{H}	0.9		1.1		1.4		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

Table 33. EPF8452A External Timing Parameters							
Symbol	**Speed Grade**						**Unit**
	A-2		**A-3**		**A-4**		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Table 38. EPF8820A I/O Element Timing Parameters

Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{IOD}		0.7		0.8		0.9	ns
t_{IOC}		1.7		1.8		1.9	ns
t_{IOE}		1.7		1.8		1.9	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1	ns
t_{IOSU}	1.4		1.6		1.8		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7	ns
t_{OD1}		1.1		1.4		1.7	ns
t_{OD2}		1.6		1.9		2.2	ns
t_{OD3}		4.6		4.9		5.2	ns
t_{XZ}		1.4		1.6		1.8	ns
t_{ZX1}		1.4		1.6		1.8	ns
t_{ZX2}		1.9		2.1		2.3	ns
t_{ZX3}		4.9		5.1		5.3	ns

Table 39. EPF8820A Interconnect Timing Parameters

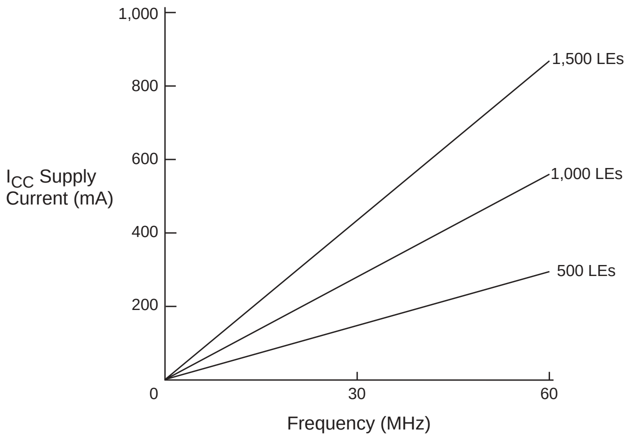
Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
$t_{LABCASC}$		0.3		0.3		0.4	ns
$t_{LABCARRY}$		0.3		0.3		0.4	ns
t_{LOCAL}		0.5		0.6		0.8	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5	ns
t_{DIN_D}		7.0		7.0		7.5	ns
t_{DIN_IO}		5.0		5.0		5.5	ns

Table 40. EPF8820A LE Timing Parameters							
Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{LUT}		2.0		2.5		3.2	ns
t_{CLUT}		0.0		0.0		0.0	ns
t_{RLUT}		0.9		1.1		1.5	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9	ns
t_{CICO}		0.4		0.5		0.6	ns
t_{CGEN}		0.4		0.5		0.7	ns
t_{CGENR}		0.9		1.1		1.5	ns
t_{C}		1.6		2.0		2.5	ns
t_{CH}	4.0		4.0		4.0		ns
t_{CL}	4.0		4.0		4.0		ns
t_{CO}		0.4		0.5		0.6	ns
t_{COMB}		0.4		0.5		0.6	ns
t_{SU}	0.8		1.1		1.2		ns
t_{H}	0.9		1.1		1.5		ns
t_{PRE}		0.6		0.7		0.8	ns
t_{CLR}		0.6		0.7		0.8	ns

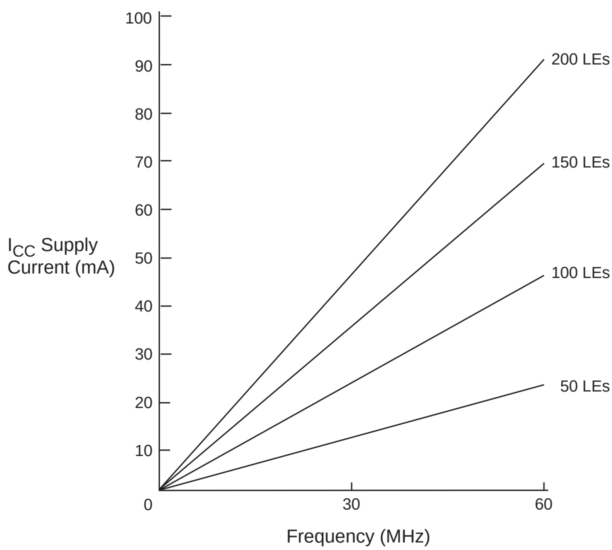
Table 41. EPF8820A External Timing Parameters							
Symbol	Speed Grade						Unit
	A-2		A-3		A-4		
	Min	Max	Min	Max	Min	Max	
t_{DRR}		16.0		20.0		25.0	ns
t_{ODH}	1.0		1.0		1.0		ns

Figure 20. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices



3.3-V FLEX 8000 Devices



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This section summarizes the device operating modes and available device configuration schemes.

For more information, go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
ADD0	78	76	78	77	106	N3	6
DATA7	3	2	90	89	131	P8	140
DATA6	4	4	91	91	132	P10	139
DATA5	6	6	92	95	133	R12	138
DATA4	7	7	95	96	134	R13	136
DATA3	8	8	97	97	135	P13	135
DATA2	9	9	99	98	137	R14	133
DATA1	13	13	4	4	138	N15	132
DATA0	14	14	5	5	140	K13	129
SDOUT *(3)*	79	78	79	79	23	P4	97
TDI *(4)*	55	45 *(5)*	54	–	96	–	17
TDO *(4)*	27	27 *(5)*	18	–	18	–	102
TCK *(4)*, *(6)*	72	44 *(5)*	72	–	88	–	27
TMS *(4)*	20	43 *(5)*	11	–	86	–	29
TRST *(7)*	52	52 *(8)*	50	–	71	–	45
Dedicated Inputs *(10)*	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	3, 24, 53, 74	9, 26, 82, 99	C3, D14, N2, R15	14, 33, 94, 113
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	9, 32, 49, 59, 82	8, 28, 70, 90, 111	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160
VCCIO	–	–	–	–	16, 40, 60, 69, 91, 112, 122, 141	–	23, 47, 57, 69, 79, 104, 127, 137, 149, 159

Table 52. FLEX 8000 84-, 100-, 144- & 160-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	84-Pin PLCC EPF8282A	84-Pin PLCC EPF8452A EPF8636A	100-Pin TQFP EPF8282A EPF8282AV	100-Pin TQFP EPF8452A	144-Pin TQFP EPF8820A	160-Pin PGA EPF8452A	160-Pin PQFP EPF8820A *(1)*
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	19, 44, 69, 94	7, 17, 27, 39, 54, 80, 81, 100,101, 128, 142	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155
No Connect (N.C.)	–	–	–	2, 6, 13, 30, 37, 42, 43, 50, 52, 56, 63, 80, 87, 92, 93, 99	–	–	–
Total User I/O Pins *(9)*	64	64	74	64	108	116	116

Table 54. FLEX 8000 225-, 232-, 240-, 280- & 304-Pin Package Pin-Outs (Part 3 of 3)						
Pin Name	**225-Pin BGA EPF8820A**	**232-Pin PGA EPF81188A**	**240-Pin PQFP EPF81188A**	**240-Pin PQFP EPF81500A**	**280-Pin PGA EPF81500A**	**304-Pin RQFP EPF81500A**
GND	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 85, 92, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 214, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291
No Connect (N.C.)	–	–	61, 62, 119, 120, 181, 182, 239, 240	–	–	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins *(9)*	148	180	180	177	204	204