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Core Size	-
Speed	-
Connectivity	-
Peripherals	-
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Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
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Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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1. Pin Group Information

1.1 Device package information

The V850ES/Fx3-L device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
µPD70F3610 µPD70F3611 µPD70F3612 µPD70F3613 µPD70F3614	64	FE3-L
µPD70F3615 µPD70F3616 µPD70F3617 µPD70F3618 µPD70F3619	80	FF3-L
µPD70F3620 µPD70F3621 µPD70F3622	100	FG3-L

This document describes the specification for the V850ES/FF3-L.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3-L)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3-L)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3-L)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3-L)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3-L)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3-L)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3-L)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3-L)

2D: (SHMT3)
- PDL0-7 (FE3-L)
- PDL0-11 (FF3-L)

1.4 Pin Groups 3x: Pins supplied by BVDD

3A: (CMOS)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FG3-L)

3D: (SHMT3)
- PDL0-13 (FG3-L)

1.5 Pin Groups 4: Pins supplied by AVREF0

4: (CMOS)
- P70-79 (FE3-L)
- P70-711 (FF3-L)
- P70-715 (FG3-L)

1.6 Pin Groups 6: Pins supplied by EVDD

- RESET (SHMT2)
- IC, FLMD0

1.7 Pin Groups 7: Pins supplied by VRO

- X1, X2, XT1, XT2

2. Electrical Specifications

This product has to be used only under the conditions of VDD=EVDD. Operation is not ensured at the time of using this product except this condition.

The operating ambient temperature of each quality grade is as follows:
(A)-Grade: Ta = -40 to +85°C
(A1)-Grade: Ta = -40 to +110°C
(A2)-Grade: Ta = -40 to +125°C

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions			Rating	Unit
Supply voltage	VDD	VDD=EVDD,			-0.5 to +6.5	V
	EVDD	VDD=EVDD			-0.5 to +6.5	
	AVREF0				-0.5 to +6.5	
	VSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	EVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	AVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
Input voltage	VI1	Pin Group 1x, 2x, 6			-0.5 to EVDD+0.5 Note1	V
	VI3	Pin Group 7			-0.5 to VRO+0.5 Note1	
Analog input voltage	VIAN	Pin Group 4			-0.5 to AVREF0+0.5 Note1	V
High level output current	IOH	Pin Group 1x, 2x	1 pin		-4	mA
			Total	(A)	-50	
				(A1)	-20	
				(A2)	-20	
		Pin Group 4	1 pin		-4	
			Total	(A)Note2	-20	
				(A1)Note2	-10	
				(A2)Note3	-10	
Low level output current	IOL	Pin Group 1x, 2x	1 pin		4	mA
			Total	(A)	50	
				(A1)	20	
				(A2)	20	
		Pin Group 4	1 pin		4	
			Total	(A)Note2	20	
				(A1)Note2	10	
				(A2)Note3	10	
Operating ambient temperature	Ta	Normal operating mode		(A)	-40 to +85	°C
		Flash programming mode				
		Normal operating mode		(A1)	-40 to +110	
		Flash programming mode				
		Normal operating mode		(A2)	-40 to +125	
		Flash programming mode				
Storage temperature	Tstg				-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 current.
3. Including ADC IAREF0 current.

2.2 Capacities

(Ta = 25°C, VDD = EVDD = AVREF0 = VSS = EVSS = AVSS = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input/output capacitance	CIO	f=1MHz, Not measured pins is 0V.			10	pF

2.3 Operating condition

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f_{VBCLK})	Supply voltage	Operating Condition
$4.0 \le f_{xx} \le 20$MHz Note1	3.5V≤VDD≤5.5V Note1	Operation of functions is enabled
	3.3V≤VDD<3.5V	The following functions are operable: • CPU • Flash (including programming • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI
	3.3V≤AVRF0≤5.5V	• A/D Converter • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0) • Refer to chapter '2.8 A/D Converter' for details.
32kHz≤f_{XT}≤35kHz (Crystal)	3.3V≤VDD<5.5V Note1	-
12.5kHz≤f_{XT}≤27.5kHz Note2 (RC)		
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note1	-

Notes: 1. VDD = EVDD

2. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Refer to Figure 1	Oscillator frequency (fxt)Note1		32	32.768	35	kHz
		Oscillation stabilization time Note2				10	s

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

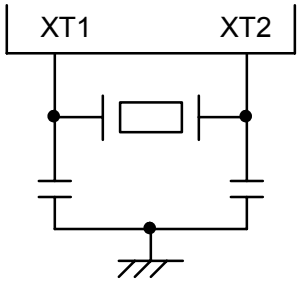
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequencyNote1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	µs

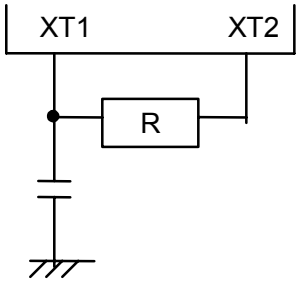
Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided (1/2) internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_{RL}	240kHz Internal-OSC	204	240	276	kHz
	f_{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation stabilization time		240kHz Internal-OSC		10	36	µs
		8MHz Internal-OSC	51	92	256	µs

2.5.4 PLL Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note1	3		6	MHz
Output frequency	fxx		10		20	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	µs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

2.6.2 PIN leakage current

(C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.			Unit
						(A)	(A1)	(A2)	
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.2	0.4	0.5	µA
			Other pins Note1			0.5	0.8	1.0	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins Note1			-0.5	-0.8	-1.0	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.2	0.4	0.5	
			Other pins			0.5	0.8	1.0	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins			-0.5	-0.8	-1.0	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current :
- (A)-Grade 2.0µA
- (A1)-Grade 4.0µA
- (A2)-Grade 5.0µA

Low level input leakage current:
- (A)-Grade -2.0µA
- (A1)-Grade -4.0µA
- (A2)-Grade 5.0µA

Mode	Symbol	Condition			TYP.	MAX. (A)	MAX. (A1)	MAX. (A2)	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4	2.2	2.5	2.8	mA
				f_{xx}=12MHz f_x=12MHz	2.0	3.1	3.4	3.7	mA
				f_{xx}=16MHz f_x=16MHz	2.4	3.6	3.9	4.2	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.5	2.3	2.6	2.9	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.2	-			mA
				f_{xx}=12MHz f_x=12MHz	1.4				mA
				f_{xx}=16MHz f_x=16MHz	1.6				mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.1				mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	0.7	0.9	1.1	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.0	1.2	1.5	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.2	1.4	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.5	0.7	1.0	mA
SUB operating mode Note5	IDD5	Crystal resonator (fxt = 32,768kHz)			80	400	-	-	μA
		RC resonator (fxt=20kHz) Note6			80	400	600	850	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1000	1200	1450	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	-	-	μA
		RC resonator (fxt=20kHz) Note6			40	220	420	670	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	380	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	80	280	530	μA
			240kHz Internal-OSC working		15.5	95	295	545	μA
		POC work	240kHz Internal-OSC stop		10.5	85	285	535	μA
			240kHz Internal-OSC working		18.5	100	300	550	μA

2.7.2 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.3 Key Return Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Timer Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1]			10	MHz

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 CSI Timing

(a) Master mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

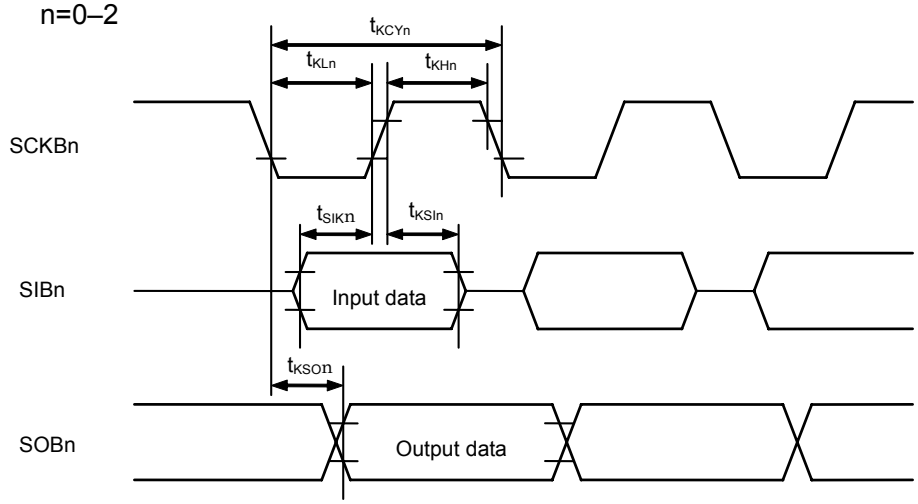
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–2



2.7.6 UART Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

2.7.7 IIC Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter		Symbol	Normal mode		High-speed mode		Unit
			min.	max.	min.	max.	
SCL00 clock frequency		fCLK	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		tBUF	4.7		1.3		µs
Hold time[Note1]		tHD:STA	4.0		0.6		µs
SCL00 clock low-level width		tLOW	4.7		1.3		µs
SCL00 clock high-level width		tHIGH	4.0		0.6		µs
Setup time for start/restart conditions		tSU:STA	4.7		0.6		µs
Data hold time	CBUS compatible master	tHD:DAT	5.0				µs
	IIC mode		0[Note2]		0[Note2]	0.9[Note3]	µs
Data setup time		tSU:DAT	250		100[Note4]		ns
SDA00 and SCL00 signal rise time		tR		1000	20+0.1Cb	300	ns
SDA00 and SCL00 signal fall time		tF		300	20+0.1Cb	300	ns
Stop condition setup time		tSU:STO	4.0		0.6		µs
Pilse width with spike supporessed by input filter		tSP			0	50	ns
Capacitance load of each bus line		Cb		400		400	pF

Notes: 1. At the start condition, the first clock pulse is generated after the hold time

2. The system requires a minimum of 300ns hold time Internally for the SDA signal (at VIH-min. of SCL00 signal)
In order to occupy the undefined area at the falling edge of SCL00.

3. If the system does not extend the SCL00 signal low hold time (tlow), only the maximum data hold time (tHD:DAT) needs to be satisfied.

4. The high-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the high-speed-mode IIC bus so that It meets the following conditions.
- If the system does not extend the SCL00 signal's low state hold time:
SU:DAT?250ns
- If the system extends the SCL00 signal's low state hold time:
Transmit the following data bit to the SDA00 line prior to releasing the SCL00 line (tRmax.+tSU:DAT=1000+250=1250ns: Normal mode IIC bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

2.8 A/D Converter

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 4.0 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.		Unit
					(A),(A1)	(A2)	
Resolution					10		bit
Overall error[Note1]		4.0V≤AVREF0<5.5V		±0.15	±0.3	±0.35	%FSR
Conversion time	tCONV		3.10		16		µs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2				µs
Recovery time for power down mode	tDPU		1				µs
Zero-scale error[Note1]	ZSE				±0.3	±0.35	%FSR
Full-scale error[Note1]	FSE				±0.3	±0.35	%FSR
Integral non-liniearity error[Note2]	INL				±2.5		LSB
Differential non-liniearity error[Note2]	DNL				±1.5		LSB
Analog input voltage	VIAN		AVSS		AVREF0		V
Analog input equivalent circuit capacitance [Note3,4]	CINA				6.19		pF
Analog input equivalent circuit resistance [Note3]	RINA				2.55		kΩ
AVREF0 current	IAREF0	A/D operating		4	7		mA
		A/D operation stop		1	10		µA
Conversion rusult when using Diagnostic function		AVREF0 conversion	3FC		3FF		HEX
		AVSS conversion	000		003		HEX

Notes: 1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.

2. Excluding quantization error (±1/2 LSB)

3. Reference value. Not tested in production.

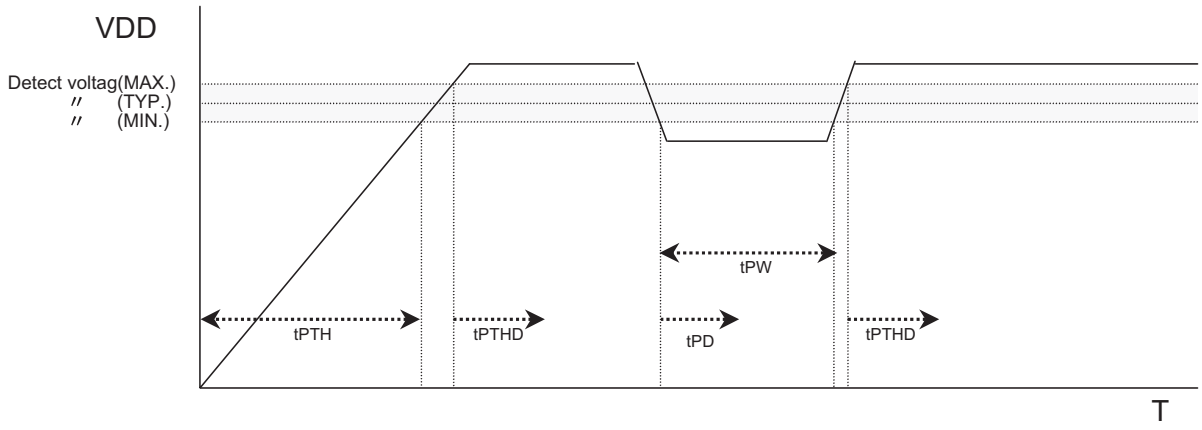
4. Does not include input/output capacitance CIO

2.9 POC

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VPOC0		3.3	3.5	3.7	V
Supply voltage rise time	tPTH	From VDD=0V to VDD=3.3V	0.002			ms
Response time1 Note1	tPTHD	In case of power on. After VDD reaches 3.7V.			2.0	ms
Response time2 Note2	tPD	In case of power off. After VDD drop 3.3V.		0.2	1.0	ms
VDD minimum width	tPW		0.2			ms

Notes: 1. From detect voltage to release reset signal
2. From detect voltage to occurrence of reset signal



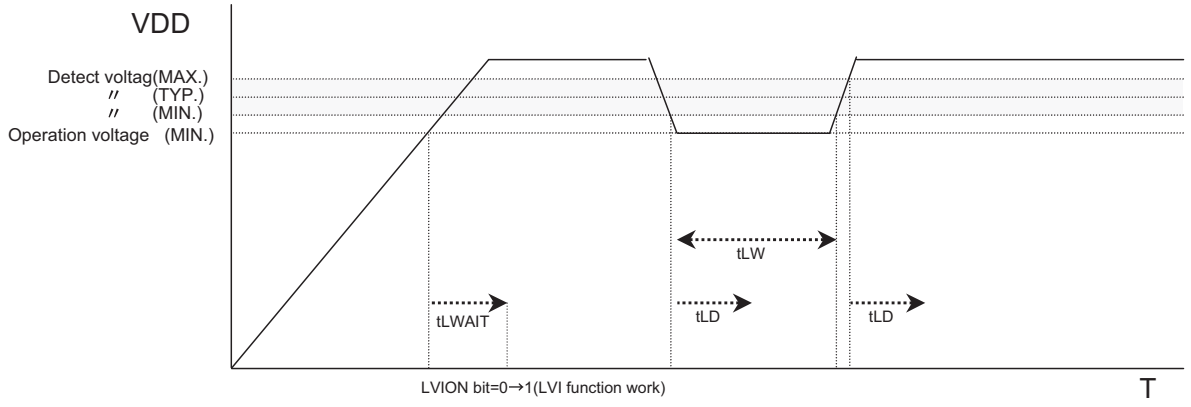
Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3-L User'sManual.

2.10 LVI

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VLVI0		3.8	4.0	4.2	V
	VLVI1		3.5	3.7	3.9	V
Response time Note1	tLD	After VDD reaches VLVI0/1(max). After VDD drop VLVI0/1(min).		0.2	2.0	ms
VDD minimum width	tLW		0.2			ms
Reference voltage stabilization wait time Note2	tLWAIT	After VDD reaches 3.3V. After LVION bit (LVIM.bit7) = 0->1		0.1	0.2	ms

Notes: 1. From detect voltage to occurrence interrupt/reset signal
2. If POC functionality is available, the wait time is not needed.

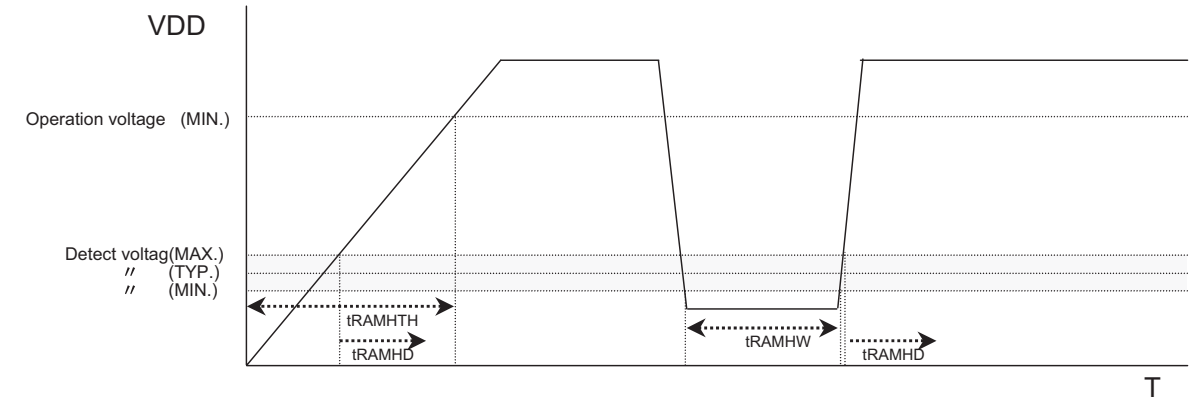


2.11 RAM Retention Flag

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VRAMH		1.9	2.0	2.1	V
Supply voltage rise time	tRAMHTH	From VDD=0V to VDD=3.3V	0.002		1800	ms
Response time Note1	tRAMHD	After VDD reaches 2.1V.		0.2	2.0	ms
VDD minimum width	tRAMHW		0.2			ms

Notes: 1. From detect voltage to set RAMFbit (RAMS.bit0)



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

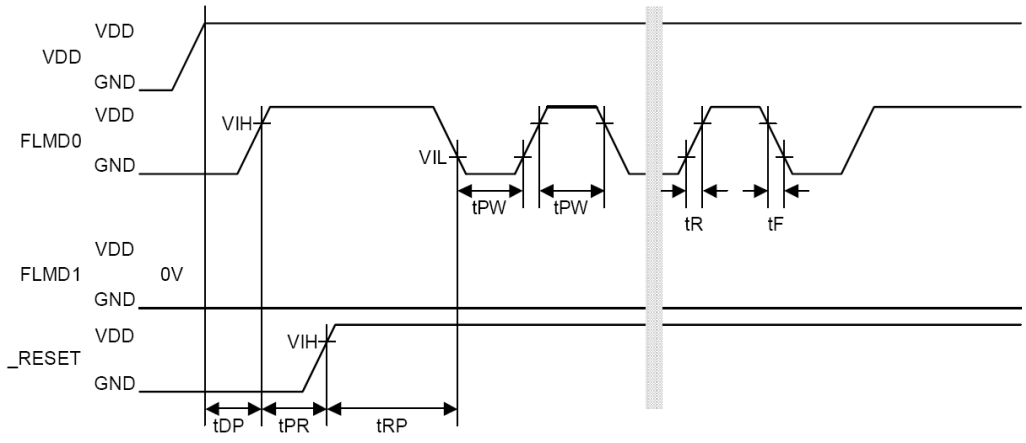
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.			Unit
					(A)	(A1)	(A2)	
Operation frequency	fCPU		4		20			MHz
Supply voltage	VDD		3.3		5.5			V
Number of rewrites	CWRT	Code Flash			1000			count
High level input voltage	VIH	FLMD0	0.8·EVDD		EVDD			V
Low level input voltage	VIL	FLMD0	EVSS		0.2·EVDD			V
Programming temperature	tPRG		-40		+85	+110	+125	°C
Data retention		Code Flash	15					year

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	tDP		1			ms
$\overline{\text{RESET}}$ release (from FLMD0)	tPR		2			ms
FLMD0 pulse input start (from raise edge of _RESET)	tRP		800			µs
FLMD0 high level width / low level width	tPW		10		100	µs
FLMD0 raise time	tR				50	ns
FLMD0 fall time	tF				50	ns



4. Change History

Version	Chapter	Comment
V1.0		Initial release

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