Renesas Electronics America Inc - UPD70F3618M1GKA-GAK-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3618m1gka-gak-ax

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

For further information please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668, Japan
Tel: 044 4355111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554,l
U.S.A.
Tel: 408 5886000
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211 6503-0
http://www.eu.necel.com/

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood
Milton Keynes, MK14 6NP, U.K.
Tel: 01908 691133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01 30675800

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 6387200

Filiale Italiana
Via Fabio Filzi, 25A
20124 Milano, Italy
Tel: 02 667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven,
The Netherlands
Tel: 040 2654010

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27
ZhiChunLu Haidian District,
Beijing 100083, P.R.China
Tel: 010 82351155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2511-2512, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area,
Shanghai 200120, P.R. China
Tel: 021 5888 5400
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
Unit 1601-1613, 16/F., Tower 2
Grand Century Place
193 Prince Edward Road West,
Mongkok, Kowloon, Hong Kong
Tel: 2886 9318
http://www.hk.necel.com/

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R.O.C.
Tel: 02 8175-9600

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

NEC Electronics Korea Ltd.
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku, Seoul,
135-080, Korea
Tel: 02-558-3737
http://www.kr.necel.com/

Table of Contents

1. Pin Group Information

1.1 Device package information

The V850ES/Fx3-L device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
µPD70F3610 µPD70F3611 µPD70F3612 µPD70F3613 µPD70F3614	64	FE3-L
µPD70F3615 µPD70F3616 µPD70F3617 µPD70F3618 µPD70F3619	80	FF3-L
µPD70F3620 µPD70F3621 µPD70F3622	100	FG3-L

This document describes the specification for the V850ES/FF3-L.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3-L)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3-L)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3-L)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3-L)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3-L)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3-L)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3-L)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3-L)

2D: (SHMT3)
- PDL0-7 (FE3-L)
- PDL0-11 (FF3-L)

2. Electrical Specifications

This product has to be used only under the conditions of VDD=EVDD. Operation is not ensured at the time of using this product except this condition.

The operating ambient temperature of each quality grade is as follows:
(A)-Grade: Ta = -40 to +85°C
(A1)-Grade: Ta = -40 to +110°C
(A2)-Grade: Ta = -40 to +125°C

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions			Rating	Unit
Supply voltage	VDD	VDD=EVDD,			-0.5 to +6.5	V
	EVDD	VDD=EVDD			-0.5 to +6.5	
	AVREF0				-0.5 to +6.5	
	VSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	EVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	AVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
Input voltage	VI1	Pin Group 1x, 2x, 6			-0.5 to EVDD+0.5 Note1	V
	VI3	Pin Group 7			-0.5 to VRO+0.5 Note1	
Analog input voltage	VIAN	Pin Group 4			-0.5 to AVREF0+0.5 Note1	V
High level output current	IOH	Pin Group 1x, 2x	1 pin		-4	mA
			Total	(A)	-50	
				(A1)	-20	
				(A2)	-20	
		Pin Group 4	1 pin		-4	
			Total	(A)Note2	-20	
				(A1)Note2	-10	
				(A2)Note3	-10	
Low level output current	IOL	Pin Group 1x, 2x	1 pin		4	mA
			Total	(A)	50	
				(A1)	20	
				(A2)	20	
		Pin Group 4	1 pin		4	
			Total	(A)Note2	20	
				(A1)Note2	10	
				(A2)Note3	10	
Operating ambient temperature	Ta	Normal operating mode		(A)	-40 to +85	°C
		Flash programming mode				
		Normal operating mode		(A1)	-40 to +110	
		Flash programming mode				
		Normal operating mode		(A2)	-40 to +125	
		Flash programming mode				
Storage temperature	Tstg				-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 current.
3. Including ADC IAREF0 current.

2.2 Capacities

(Ta = 25°C, VDD = EVDD = AVREF0 = VSS = EVSS = AVSS = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input/output capacitance	CIO	f=1MHz, Not measured pins is 0V.			10	pF

2.3 Operating condition

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f_{VBCLK})	Supply voltage	Operating Condition
$4.0 \le f_{xx} \le 20$MHz Note1	3.5V≤VDD≤5.5V Note1	Operation of functions is enabled
	3.3V≤VDD<3.5V	The following functions are operable: • CPU • Flash (including programming • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI
	3.3V≤AVRF0≤5.5V	• A/D Converter • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0) • Refer to chapter '2.8 A/D Converter' for details.
32kHz≤f_{XT}≤35kHz (Crystal)	3.3V≤VDD<5.5V Note1	-
12.5kHz≤f_{XT}≤27.5kHz Note2 (RC)		
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note1	-

Notes: 1. VDD = EVDD

2. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Refer to Figure 1	Oscillator frequency (fxt)Note1		32	32.768	35	kHz
		Oscillation stabilization time Note2				10	s

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

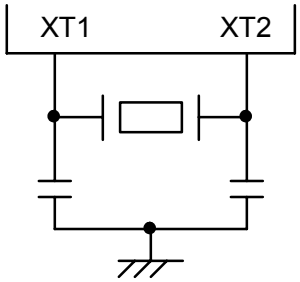
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequencyNote1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	µs

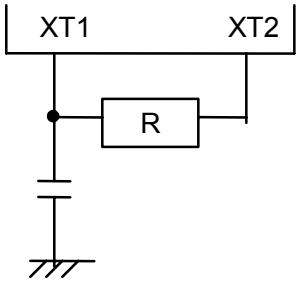
Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided (1/2) internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_{RL}	240kHz Internal-OSC	204	240	276	kHz
	f_{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation stabilization time		240kHz Internal-OSC		10	36	µs
		8MHz Internal-OSC	51	92	256	µs

2.6.2 PIN leakage current

(C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.			Unit
						(A)	(A1)	(A2)	
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.2	0.4	0.5	µA
			Other pins Note1			0.5	0.8	1.0	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins Note1			-0.5	-0.8	-1.0	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.2	0.4	0.5	
			Other pins			0.5	0.8	1.0	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins			-0.5	-0.8	-1.0	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current :
- (A)-Grade 2.0µA
- (A1)-Grade 4.0µA
- (A2)-Grade 5.0µA

Low level input leakage current:
- (A)-Grade -2.0µA
- (A1)-Grade -4.0µA
- (A2)-Grade 5.0µA

Mode	Symbol	Condition				TYP.	MAX.			Unit
							(A)	(A1)	(A2)	
HALT mode	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	10	15			mA
					f_{xx}=20MHz f_x=10MHz	17	25			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	7	11			mA
					f_{xx}=16MHz f_x=16MHz	12	18			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	14	21			mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	7	-			mA
					f_{xx}=20MHz f_x=10MHz	12				mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	5				mA
					f_{xx}=16MHz f_x=16MHz	9				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	11				mA

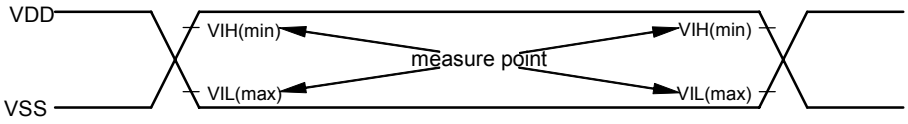
(b) Calculation formulas

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V[Note1])

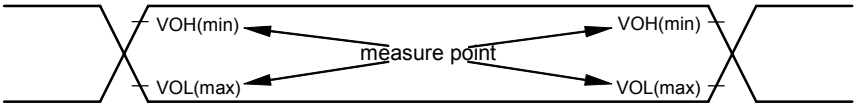
Mode	Symbol	Condition			TYP. [Note8]	MAX. [Note8]			Unit
						(A)	(A1)	(A2)	
Operating mode [Note2]	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.93·f_{xx}+6.3	1.12·f_{xx}+12.6			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.93·f_{xx}+4.7	1.12·f_{xx}+9.7			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.85·f_{xx}+5.2	1.03·f_{xx}+11.3			mA
		All peripherals stopped	Peripheral: ff_{xx-} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.78·f_{xx}+5.4	-			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.80·f_{xx}+4.9				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.76·f_{xx}+5.4				mA
HALT mode	IDD2	All peripherals running	Peripheral: ff_{xx-} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.70·f_{xx}+3.0	0.97*f_{xx}+5.2			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.65·f_{xx}+1.9	0.90*f_{xx}+3.6			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.54·f_{xx}+2.8	0.63*f_{xx}+8.60			mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.46·f_{xx}+2.8	-			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.44·f_{xx}+1.6				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.46·f_{xx}+1.8				mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz	0.092·f_{xx}+0.90	0.128·f_{xx}+ 1.52	0.128·f_{xx}+ 1.82	0.128·f_{xx}+ 2.12	mA
		All peripherals stopped			0.035·f_{xx}+1.01	-			mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz [Note7]			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.43	0.049·f_{xx}+ 0.63	0.049·f_{xx}+ 0.88	mA

2.7 AC Characteristics

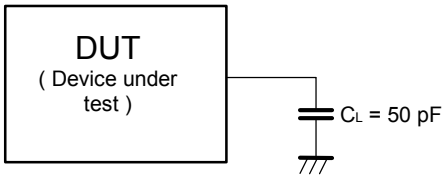
AC test Input measurement points (VDD, AVREF0, EVDD)



AC test output measurement points



Load conditions



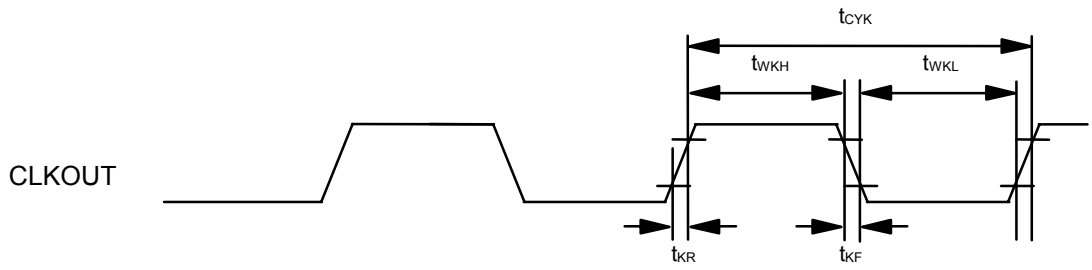
Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

2.7.1 CLKOUT Output Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	tCYK		50ns	80μs	
High level width	tWKH	VDD = EVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = 3.5V ~ 5.5V	tCYK/2-15		
Low level width	tWKL	VDD = EVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = 3.5V ~ 5.5V	tCYK/2-15		
Rise time	tKR	VDD = EVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = 3.5V ~ 5.5V		15	
Fall time	tKF	VDD = EVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = 3.5V ~ 5.5V		15	

CLKOUT output timing



•

2.7.2 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.3 Key Return Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Timer Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1]			10	MHz

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 CSI Timing

(a) Master mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

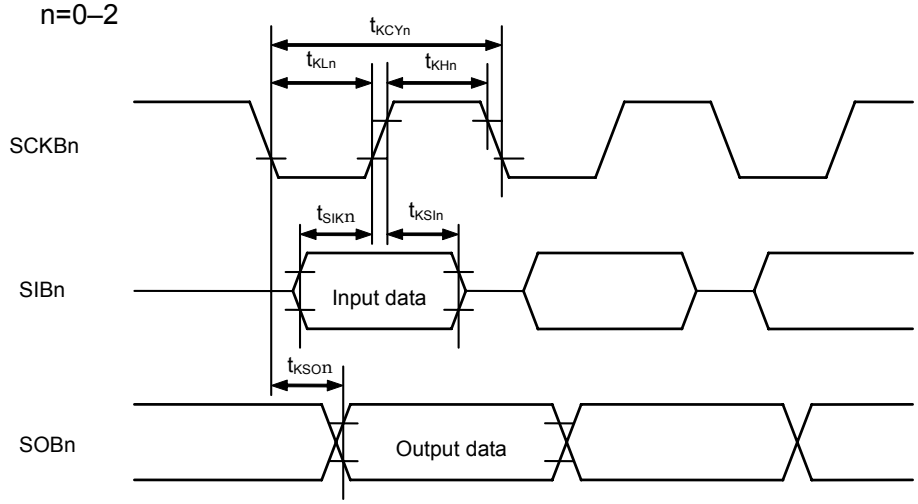
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–2

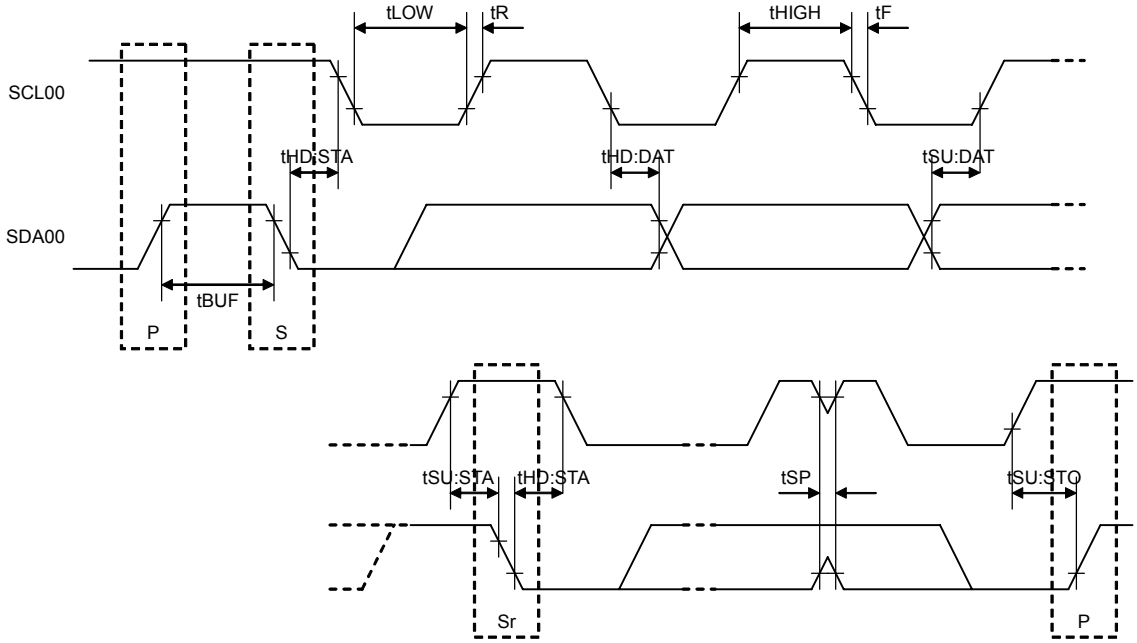


2.7.6 UART Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

IIC bus interface timing

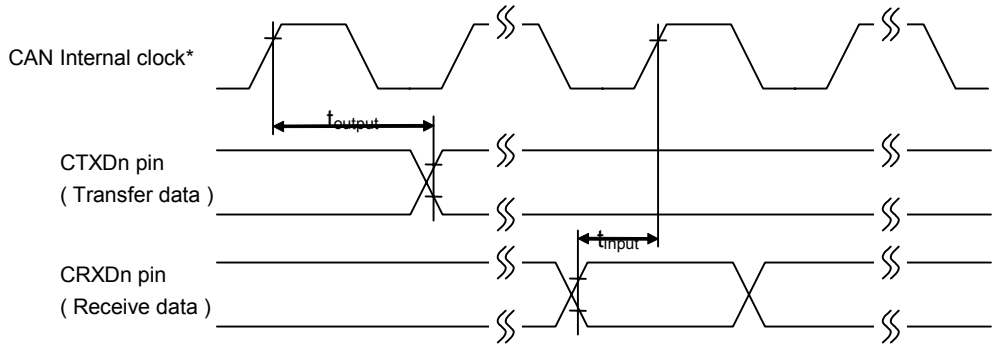


Remark: P: Stop condition
S: Start condition
Sr: Restart condition

2.7.8 CAN Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time					100	ns



Internal delay time (tNODE)= Internal Transfer Delay(t_{output}) + Internal Receive Delay(t_{input})

*) CAN Internal clock (f_{CAN}) :CAN baud rate clock

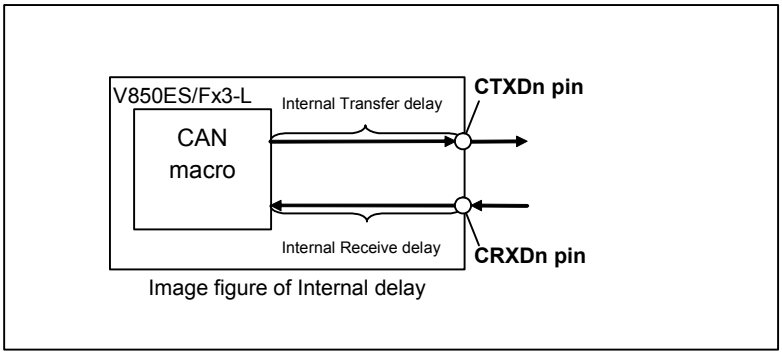


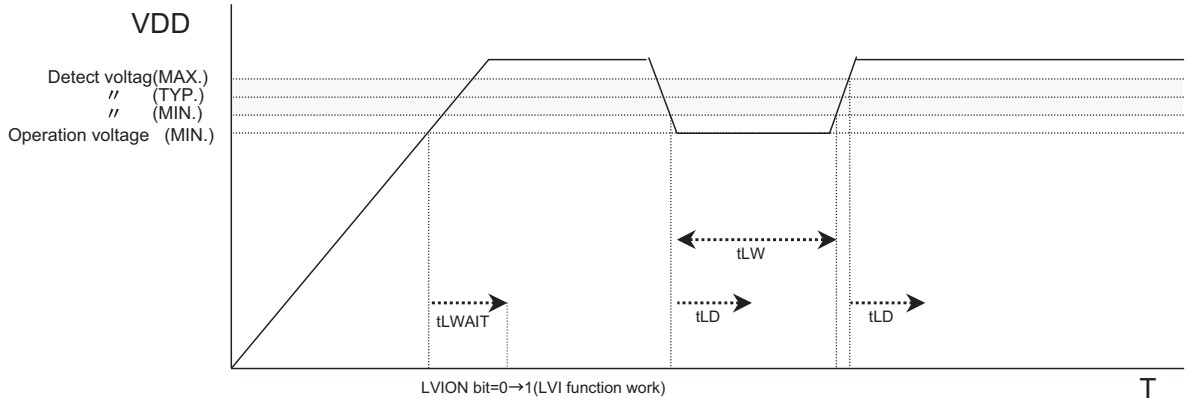
Image figure of Internal delay

2.10 LVI

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VLVI0		3.8	4.0	4.2	V
	VLVI1		3.5	3.7	3.9	V
Response time Note1	tLD	After VDD reaches VLVI0/1(max). After VDD drop VLVI0/1(min).		0.2	2.0	ms
VDD minimum width	tLW		0.2			ms
Reference voltage stabilization wait time Note2	tLWAIT	After VDD reaches 3.3V. After LVION bit (LVIM.bit7) = 0->1		0.1	0.2	ms

Notes: 1. From detect voltage to occurrence interrupt/reset signal
2. If POC functionality is available, the wait time is not needed.

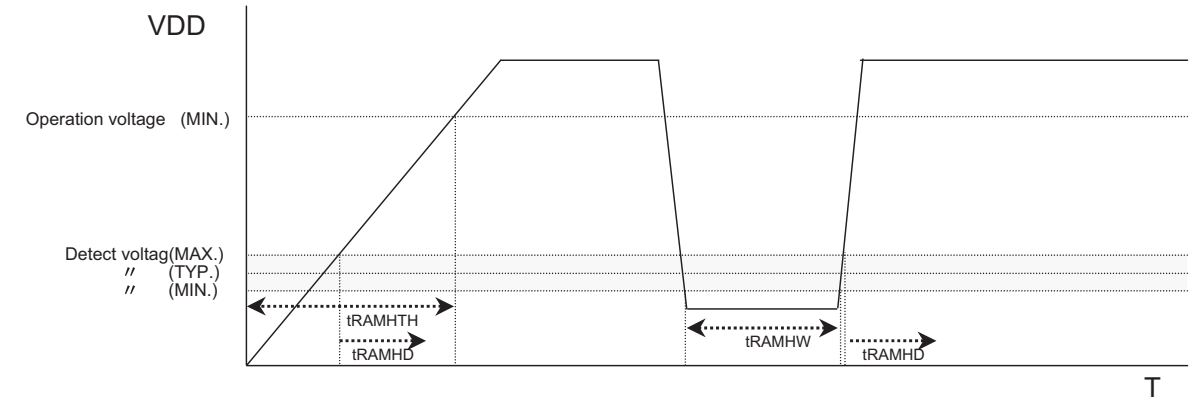


2.11 RAM Retention Flag

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VRAMH		1.9	2.0	2.1	V
Supply voltage rise time	tRAMHTH	From VDD=0V to VDD=3.3V	0.002		1800	ms
Response time Note1	tRAMHD	After VDD reaches 2.1V.		0.2	2.0	ms
VDD minimum width	tRAMHW		0.2			ms

Notes: 1. From detect voltage to set RAMFbit (RAMS.bit0)



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

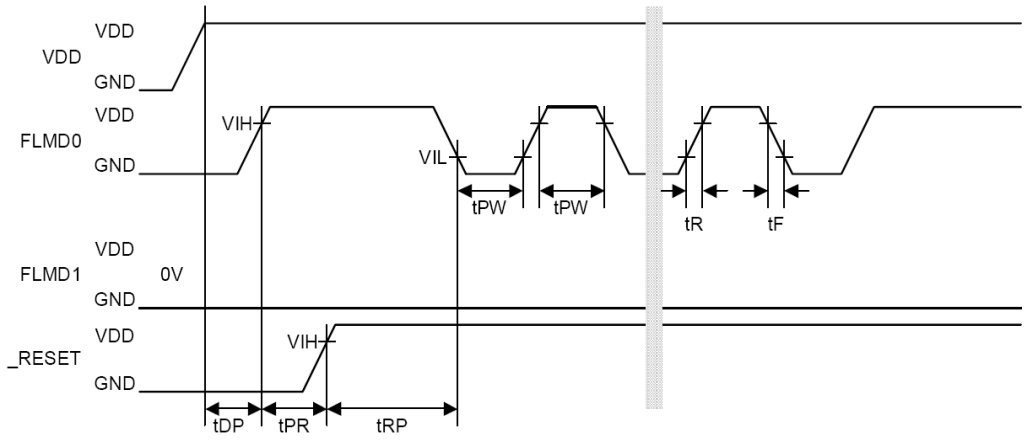
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.			Unit
					(A)	(A1)	(A2)	
Operation frequency	fCPU		4		20			MHz
Supply voltage	VDD		3.3		5.5			V
Number of rewrites	CWRT	Code Flash			1000			count
High level input voltage	VIH	FLMD0	0.8·EVDD		EVDD			V
Low level input voltage	VIL	FLMD0	EVSS		0.2·EVDD			V
Programming temperature	tPRG		-40		+85	+110	+125	°C
Data retention		Code Flash	15					year

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

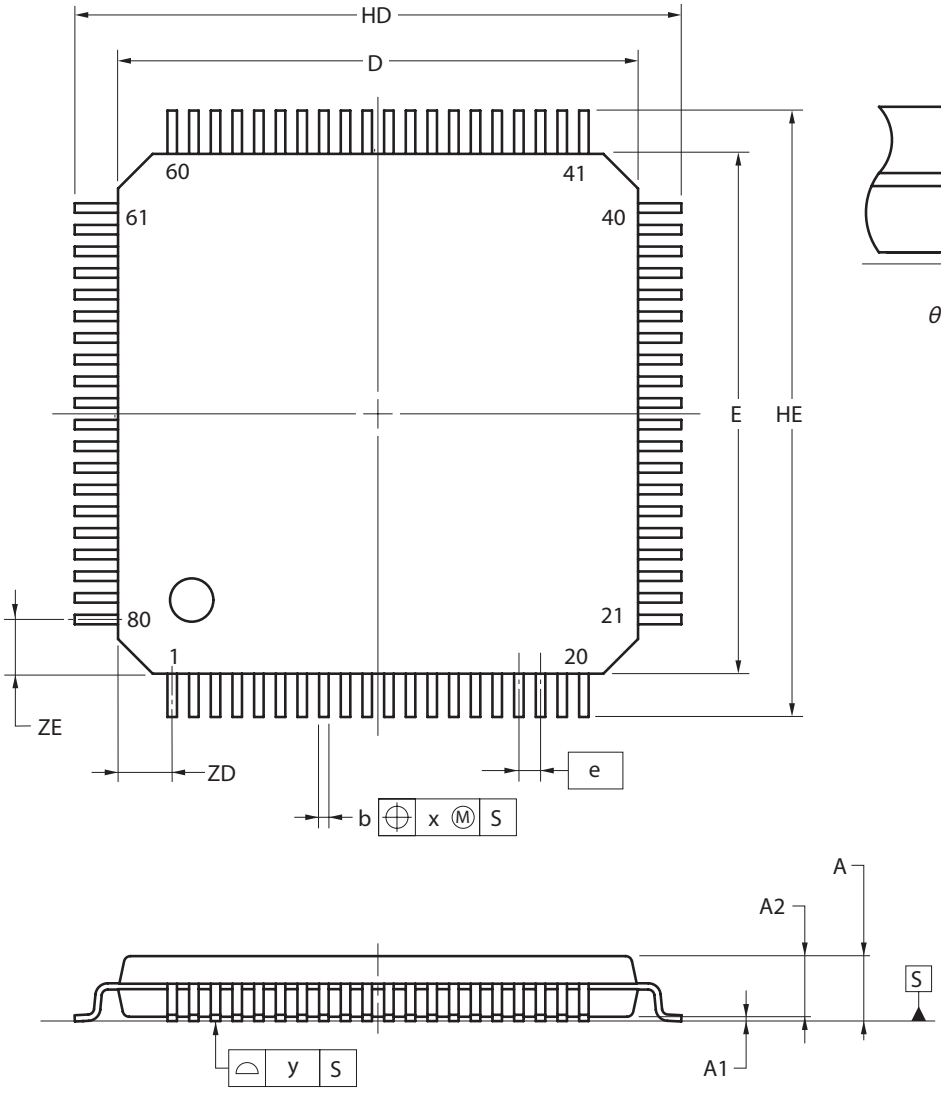
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	tDP		1			ms
$\overline{\text{RESET}}$ release (from FLMD0)	tPR		2			ms
FLMD0 pulse input start (from raise edge of _RESET)	tRP		800			µs
FLMD0 high level width / low level width	tPW		10		100	µs
FLMD0 raise time	tR				50	ns
FLMD0 fall time	tF				50	ns

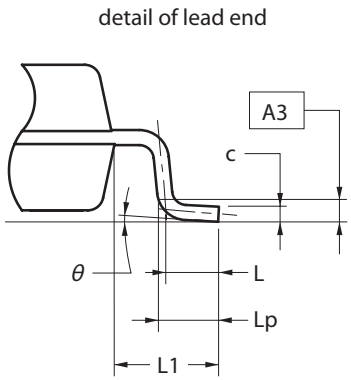


3. Package

3.1 Package Dimension

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)





(UNIT:mm)

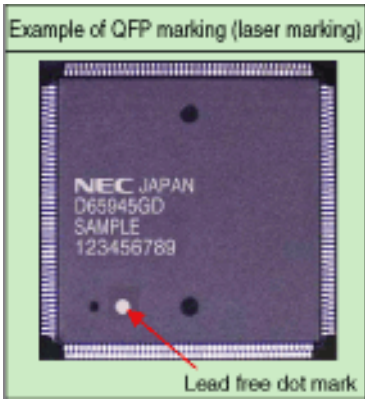
ITEM	DIMENSIONS
D	12.00 ±0.20
E	12.00 ±0.20
HD	14.00 ±0.20
HE	14.00 ±0.20
A	1.60 MAX.
A1	0.10 ±0.05
A2	1.40 ±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P80GK-50-GAK

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

3.2.2 Identification of Lead-Free Products

Lead-Free products are marked with a dot "•". The marking methods are the paint or the laser (It doesn't sink in). The shape of lead-free marks is a circle.
Example:



4. Change History

Version	Chapter	Comment
V1.0		Initial release

[MEMO]