Renesas Electronics America Inc - UPD70F3619M1GKA-GAK-AX Datasheet

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Oscillator Type	-
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Table of Contents

1. Pin Group Information

1.1 Device package information

The V850ES/Fx3-L device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
µPD70F3610 µPD70F3611 µPD70F3612 µPD70F3613 µPD70F3614	64	FE3-L
µPD70F3615 µPD70F3616 µPD70F3617 µPD70F3618 µPD70F3619	80	FF3-L
µPD70F3620 µPD70F3621 µPD70F3622	100	FG3-L

This document describes the specification for the V850ES/FF3-L.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3-L)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3-L)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3-L)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3-L)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3-L)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3-L)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3-L)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3-L)

2D: (SHMT3)
- PDL0-7 (FE3-L)
- PDL0-11 (FF3-L)

2. Electrical Specifications

This product has to be used only under the conditions of VDD=EVDD. Operation is not ensured at the time of using this product except this condition.

The operating ambient temperature of each quality grade is as follows:
(A)-Grade: Ta = -40 to +85°C
(A1)-Grade: Ta = -40 to +110°C
(A2)-Grade: Ta = -40 to +125°C

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions			Rating	Unit
Supply voltage	VDD	VDD=EVDD,			-0.5 to +6.5	V
	EVDD	VDD=EVDD			-0.5 to +6.5	
	AVREF0				-0.5 to +6.5	
	VSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	EVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	AVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
Input voltage	VI1	Pin Group 1x, 2x, 6			-0.5 to EVDD+0.5 Note1	V
	VI3	Pin Group 7			-0.5 to VRO+0.5 Note1	
Analog input voltage	VIAN	Pin Group 4			-0.5 to AVREF0+0.5 Note1	V
High level output current	IOH	Pin Group 1x, 2x	1 pin		-4	mA
			Total	(A)	-50	
				(A1)	-20	
				(A2)	-20	
		Pin Group 4	1 pin		-4	
			Total	(A) Note2	-20	
				(A1) Note2	-10	
				(A2) Note3	-10	
Low level output current	IOL	Pin Group 1x, 2x	1 pin		4	mA
			Total	(A)	50	
				(A1)	20	
				(A2)	20	
		Pin Group 4	1 pin		4	
			Total	(A) Note2	20	
				(A1) Note2	10	
				(A2) Note3	10	
Operating ambient temperature	Ta	Normal operating mode		(A)	-40 to +85	°C
		Flash programming mode				
		Normal operating mode		(A1)	-40 to +110	
		Flash programming mode				
		Normal operating mode		(A2)	-40 to +125	
		Flash programming mode				
Storage temperature	Tstg				-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

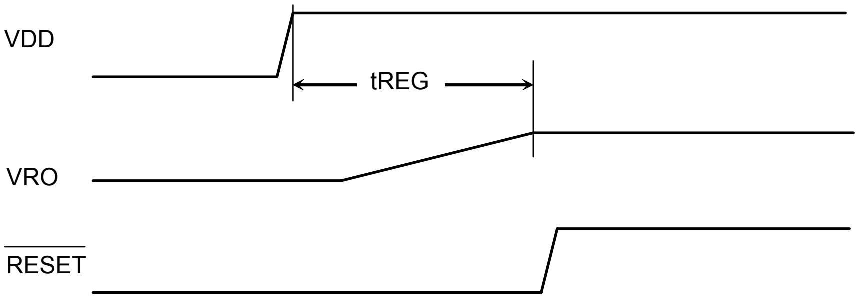
Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 current.
3. Including ADC IAREF0 current.

2.4 Voltage Regulator Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	VDD		3.5		5.5	V
		Limited function see '2.3 Operating condition'	3.3			V
Output voltage	VRO			2.5		V
Output voltage stabilization time	t_{REG}^{Note}	After VDD reaches voltage range min. 3.3V To connect C=4.7uF on REGC terminal			1	ms

Note: In case of non-POC device, be sure to start VDD in the state of $\overline{RESET}$=VSS=0V. For POC devices there is no need to control external $\overline{RESET}$ terminal. For decives with POC function the internal $\overline{RESET}$ signal will automatically controlled until VRO is stable.



2.5 Clock Generator Circuit

2.5.1 Main System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

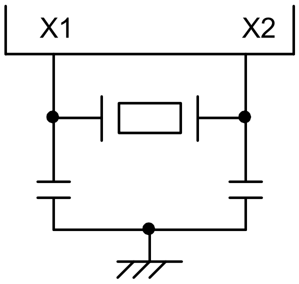
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal / Ceramic resonator	Refer to figure below	Oscillator frequency $(fx)^{Note1}$		4		16	MHz
		Oscillation stabilization time ^{Note2}	After STOP mode	54^{Note4}	Note3		µs
			After IDLE2 mode	54^{Note4}	Note3		µs

Notes: 1. Indicates only oscillation circuit characteristics. Refer to '2.7 AC Characteristics' for CPU operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range MIN. 3.3V

3. Depends on the setting of the oscillation stabilization time select register (OSTS)

4. Minimum time required to stabilize flash. Time has to be secured by setting the oscillation stabilization time select register (OSTS)



2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Refer to Figure 1	Oscillator frequency (fxt)[Note1]		32	32.768	35	kHz
		Oscillation stabilization time [Note2]				10	s

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

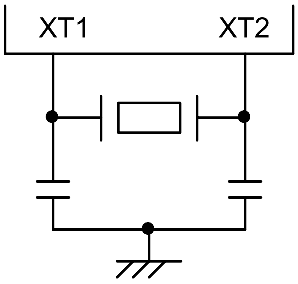
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequency[Note1,4]	R=390KΩ ±5% [Note3], C=47pF±10% [Note3]	25	40	55	kHz
		Oscillation stabilization time [Note2]				100	µs

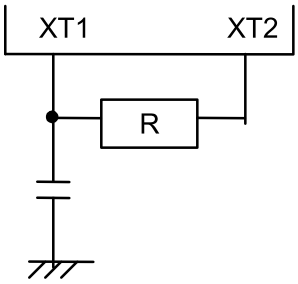
Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided (1/2) internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_{RL}	240kHz Internal-OSC	204	240	276	kHz
	f_{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation stabilization time		240kHz Internal-OSC		10	36	µs
		8MHz Internal-OSC	51	92	256	µs

2.5.4 PLL Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note1	3		6	MHz
Output frequency	fxx		10		20	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	µs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

Mode	Symbol	Condition			TYP.	MAX.			Unit
						(A)	(A1)	(A2)	
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4	2.2	2.5	2.8	mA
				f_{xx}=12MHz f_x=12MHz	2.0	3.1	3.4	3.7	mA
				f_{xx}=16MHz f_x=16MHz	2.4	3.6	3.9	4.2	mA
			fxx=8MHz, 8MHz Internal-OSC^{Note3}		1.5	2.3	2.6	2.9	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.2	-			mA
				f_{xx}=12MHz f_x=12MHz	1.4				mA
				f_{xx}=16MHz f_x=16MHz	1.6				mA
			fxx=8MHz, 8MHz Internal-OSC^{Note3}		1.1				mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	0.7	0.9	1.1	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.0	1.2	1.5	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.2	1.4	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC ^{Note3}			0.2	0.5	0.7	1.0	mA
SUB operating mode^{Note5}	IDD5	Crystal resonator (fxt = 32,768kHz)			80	400	-	-	μA
		RC resonator (fxt=20kHz) ^{Note6}			80	400	600	850	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1000	1200	1450	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	-	-	μA
		RC resonator (fxt=20kHz) ^{Note6}			40	220	420	670	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	380	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	80	280	530	μA
			240kHz Internal-OSC working		15.5	95	295	545	μA
		POC work	240kHz Internal-OSC stop		10.5	85	285	535	μA
			240kHz Internal-OSC working		18.5	100	300	550	μA

Notes: 1. VDD and EVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash is in read mode.
When the device is in programming mode (Self-programming mode) the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]

3. Main OSC is stopped.

4. Do not use SubOSC.

5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.

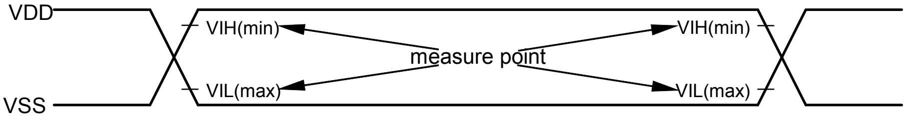
6. RC Oscillation frequency is typ.40kHz. This clock is divided by 1/2 internally.

7. 8MHz Internal-OSC is stopped

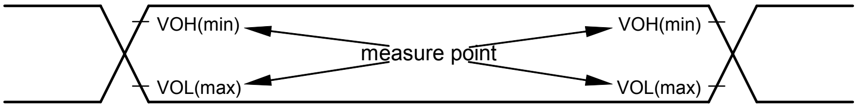
8. The formulas are for reference only. Not all possible values for f_{XX} are tested in the outgoing device inspection.

2.7 AC Characteristics

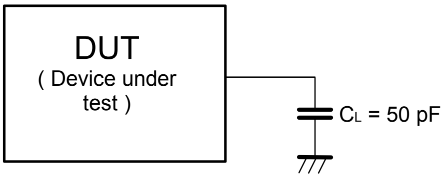
AC test Input measurement points (VDD, AVREF0, EVDD)



AC test output measurement points



Load conditions



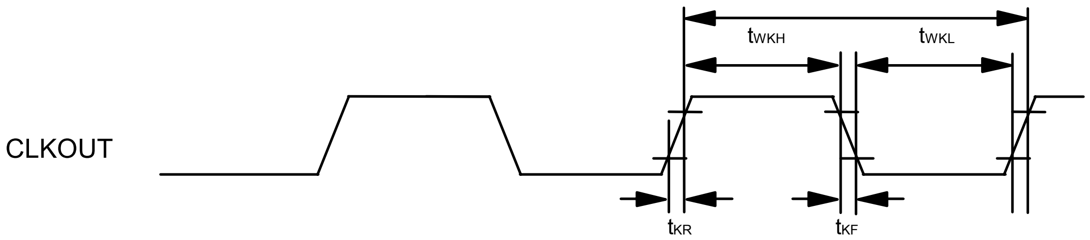
Caution: If the load capacitance exceeds 50pF due to the circuit configuration, reduce the load capacitance of the device to 50pF or less by inserting a buffer or by some other means.

2.7.1 CLKOUT Output Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output cycle	tCYK		50ns	80µs	
High level width	tWKH	VDD = EVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = 3.5V ~ 5.5V	tCYK/2-15		
Low level width	tWKL	VDD = EVDD = 4.0V ~ 5.5V	tCYK/2-13		ns
		VDD = EVDD = 3.5V ~ 5.5V	tCYK/2-15		
Rise time	tKR	VDD = EVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = 3.5V ~ 5.5V		15	
Fall time	tKF	VDD = EVDD = 4.0V ~ 5.5V		13	ns
		VDD = EVDD = 3.5V ~ 5.5V		15	

CLKOUT output timing



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2.7.7 IIC Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade,
VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter		Symbol	Normal mode		High-speed mode		Unit
			min.	max.	min.	max.	
SCL00 clock frequency		fCLK	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		tBUF	4.7		1.3		µs
Hold time[Note1]		tHD:STA	4.0		0.6		µs
SCL00 clock low-level width		tLOW	4.7		1.3		µs
SCL00 clock high-level width		tHIGH	4.0		0.6		µs
Setup time for start/restart conditions		tSU:STA	4.7		0.6		µs
Data hold time	CBUS compatible master	tHD:DAT	5.0				µs
	IIC mode		0[Note2]		0[Note2]	0.9[Note3]	µs
Data setup time		tSU:DAT	250		100[Note4]		ns
SDA00 and SCL00 signal rise time		tR		1000	20+0.1Cb	300	ns
SDA00 and SCL00 signal fall time		tF		300	20+0.1Cb	300	ns
Stop condition setup time		tSU:STO	4.0		0.6		µs
Pilse width with spike supporessed by input filter		tSP			0	50	ns
Capacitance load of each bus line		Cb		400		400	pF

Notes: 1. At the start condition, the first clock pulse is generated after the hold time

2. The system requires a minimum of 300ns hold time Internally for the SDA signal (at VIH-min. of SCL00 signal)
In order to occupy the undefined area at the falling edge of SCL00.

3. If the system does not extend the SCL00 signal low hold time (tlow), only the maximum data hold time (tHD:DAT) needs to be satisfied.

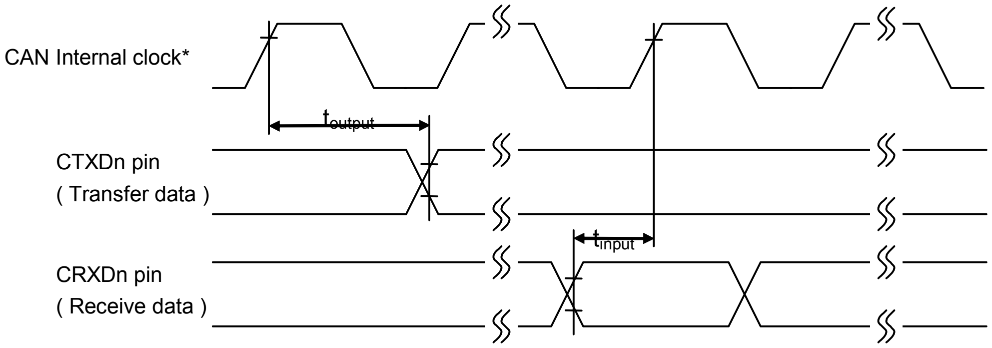
4. The high-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the high-speed-mode IIC bus so that It meets the following conditions.
- If the system does not extend the SCL00 signal's low state hold time:
SU:DAT?250ns
- If the system extends the SCL00 signal's low state hold time:
Transmit the following data bit to the SDA00 line prior to releasing the SCL00 line (tRmax.+tSU:DAT=1000+250=1250ns: Normal mode IIC bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

2.7.8 CAN Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time					100	ns



Internal delay time (tNODE)= Internal Transfer Delay(t_{output}) + Internal Receive Delay(t_{input})

*) CAN Internal clock (f_{CAN}) :CAN baud rate clock

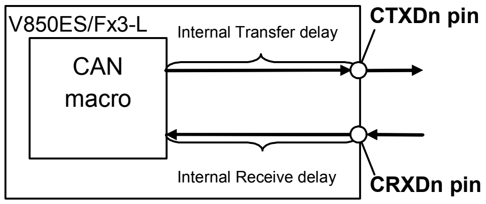


Image figure of Internal delay

2.8 A/D Converter

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 4.0 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.		Unit
					(A),(A1)	(A2)	
Resolution					10		bit
Overall error[Note1]		4.0V≤AVREF0<5.5V		±0.15	±0.3	±0.35	%FSR
Conversion time	tCONV		3.10		16		μs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2				μs
Recovery time for power down mode	tDPU		1				μs
Zero-scale error[Note1]	ZSE				±0.3	±0.35	%FSR
Full-scale error[Note1]	FSE				±0.3	±0.35	%FSR
Integral non-liniearity error[Note2]	INL				±2.5		LSB
Differential non-liniearity error[Note2]	DNL				±1.5		LSB
Analog input voltage	VIAN		AVSS		AVREF0		V
Analog input equivalent circuit capacitance [Note3,4]	CINA				6.19		pF
Analog input equivalent circuit resistance [Note3]	RINA				2.55		kΩ
AVREF0 current	IAREF0	A/D operating		4	7		mA
		A/D operation stop		1	10		μA
Conversion rusult when using Diagnostic function		AVREF0 conversion	3FC		3FF		HEX
		AVSS conversion	000		003		HEX

Notes: 1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.

2. Excluding quantization error (±1/2 LSB)

3. Reference value. Not tested in production.

4. Does not include input/output capacitance CIO

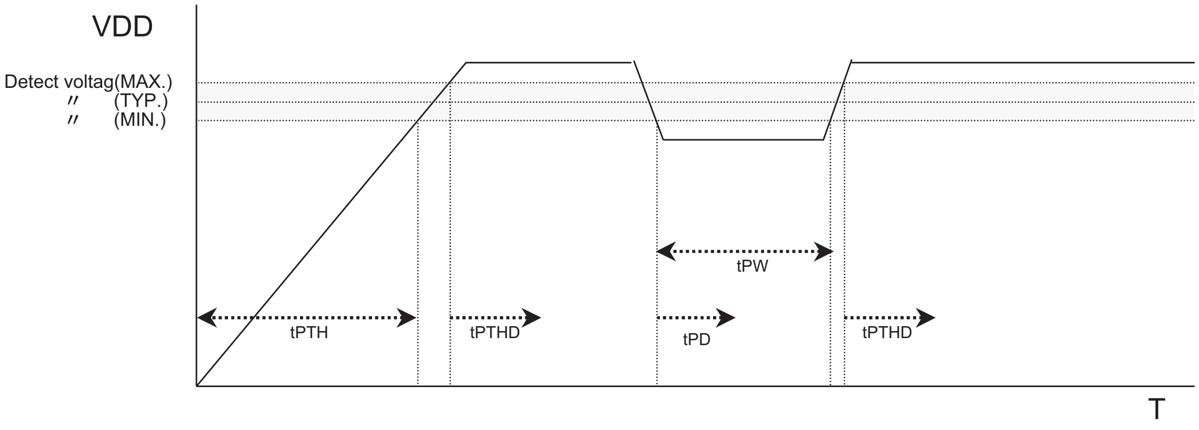
2.9 POC

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VPOC0		3.3	3.5	3.7	V
Supply voltage rise time	tPTH	From VDD=0V to VDD=3.3V	0.002			ms
Response time1 Note1	tPTHD	In case of power on. After VDD reaches 3.7V.			2.0	ms
Response time2 Note2	tPD	In case of power off. After VDD drop 3.3V.		0.2	1.0	ms
VDD minimum width	tPW		0.2			ms

Notes: 1. From detect voltage to release reset signal

2. From detect voltage to occurrence of reset signal



Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3-L User'sManual.

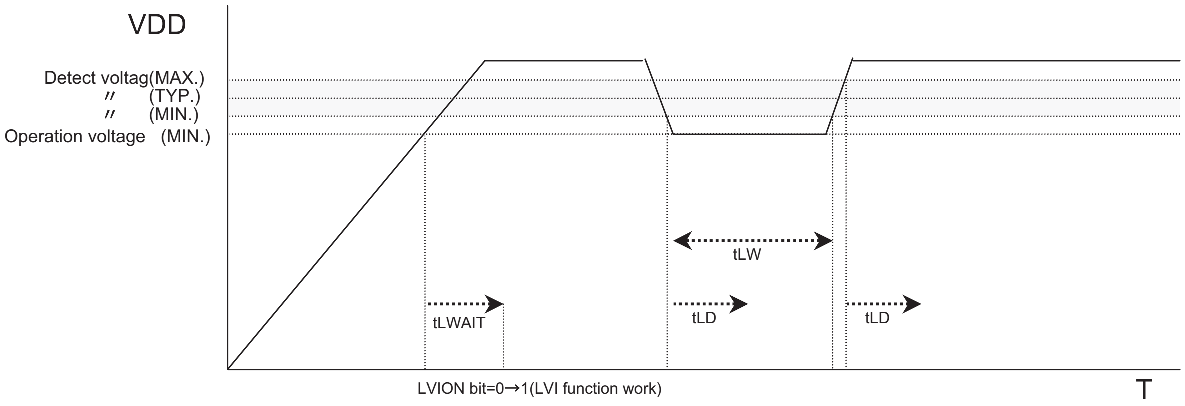
2.10 LVI

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VLVI0		3.8	4.0	4.2	V
	VLVI1		3.5	3.7	3.9	V
Response time [Note1]	tLD	After VDD reaches VLVI0/1(max). After VDD drop VLVI0/1(min).		0.2	2.0	ms
VDD minimum width	tLW		0.2			ms
Reference voltage stabilization wait time [Note2]	tLWAIT	After VDD reaches 3.3V. After LVION bit (LVIM.bit7) = 0->1		0.1	0.2	ms

Notes: 1. From detect voltage to occurrence interrupt/reset signal

2. If POC functionality is available, the wait time is not needed.

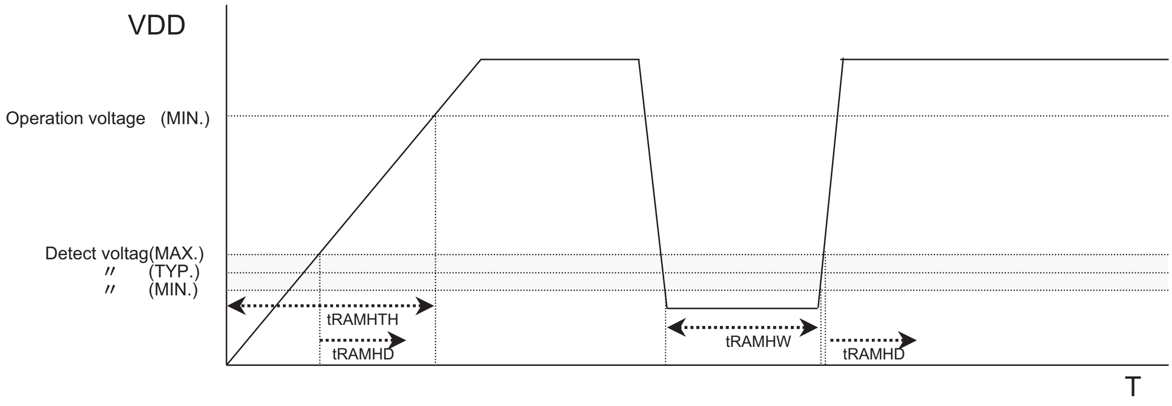


2.11 RAM Retention Flag

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VRAMH		1.9	2.0	2.1	V
Supply voltage rise time	tRAMHTH	From VDD=0V to VDD=3.3V	0.002		1800	ms
Response time [Note1]	tRAMHD	After VDD reaches 2.1V.		0.2	2.0	ms
VDD minimum width	tRAMHW		0.2			ms

Notes: 1. From detect voltage to set RAMFbit (RAMS.bit0)



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

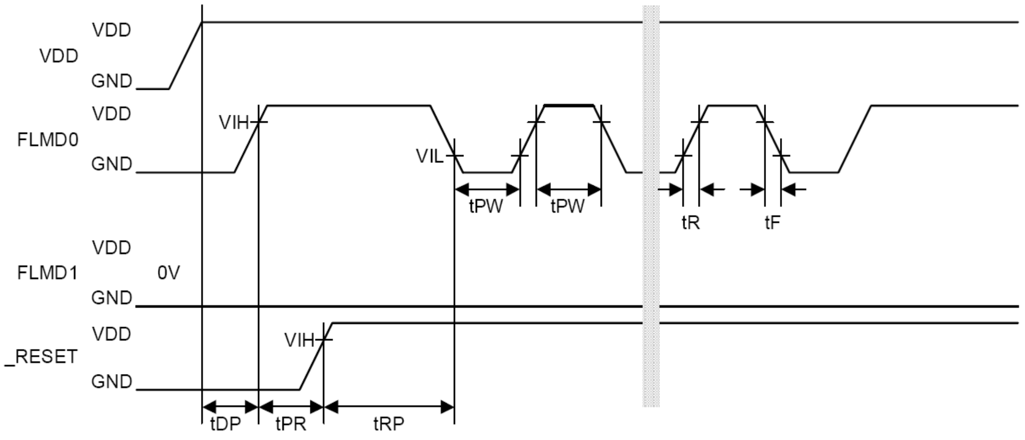
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.			Unit
					(A)	(A1)	(A2)	
Operation frequency	fCPU		4		20			MHz
Supply voltage	VDD		3.3		5.5			V
Number of rewrites	CWRT	Code Flash			1000			count
High level input voltage	VIH	FLMD0	0.8·EVDD		EVDD			V
Low level input voltage	VIL	FLMD0	EVSS		0.2·EVDD			V
Programming temperature	tPRG		-40		+85	+110	+125	°C
Data retention		Code Flash	15					year

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

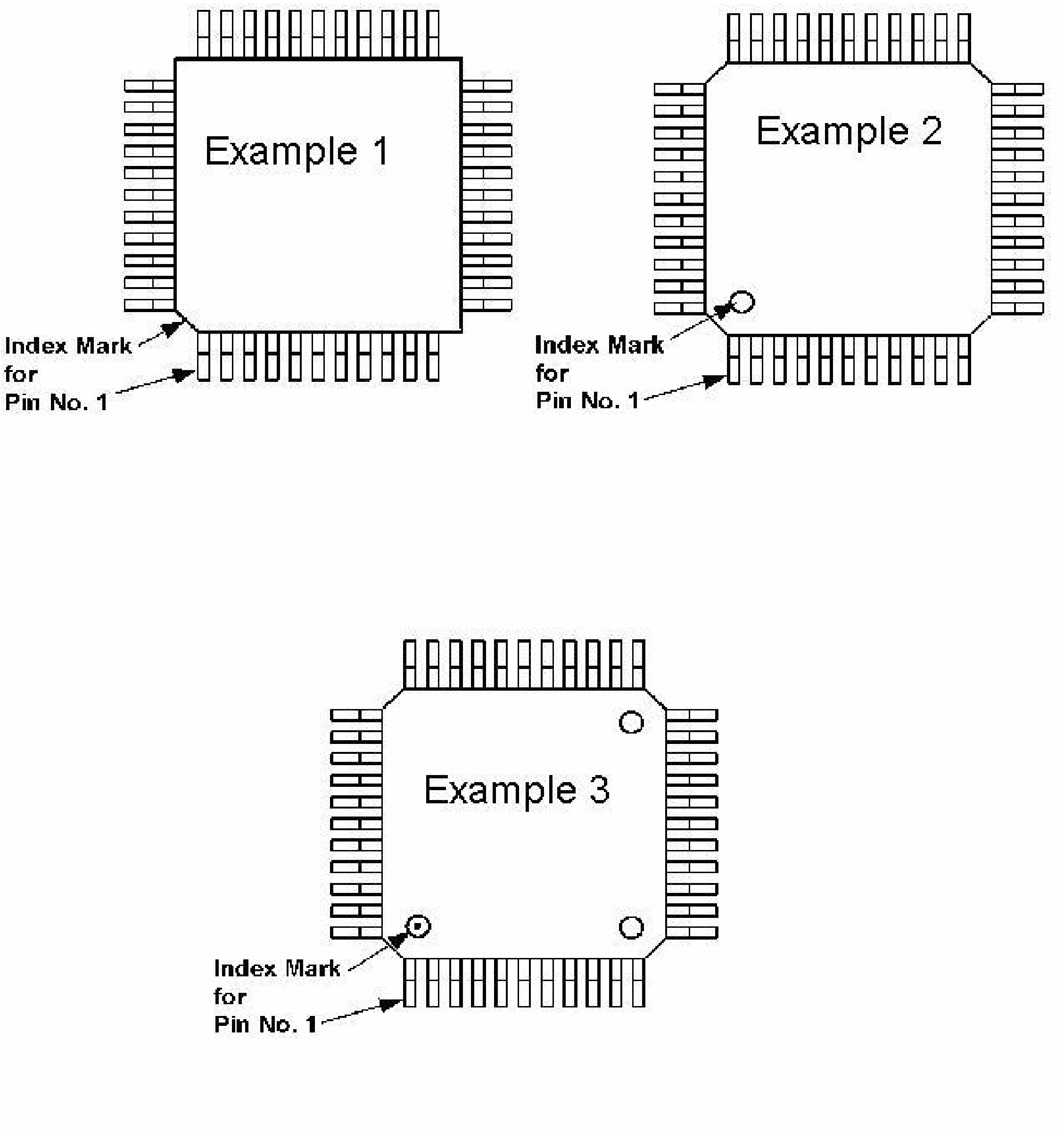
(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	tDP		1			ms
$\overline{\text{RESET}}$ release (from FLMD0)	tPR		2			ms
FLMD0 pulse input start (from raise edge of _RESET)	tRP		800			µs
FLMD0 high level width / low level width	tPW		10		100	µs
FLMD0 raise time	tR				50	ns
FLMD0 fall time	tF				50	ns



3.2 Product Marking

3.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

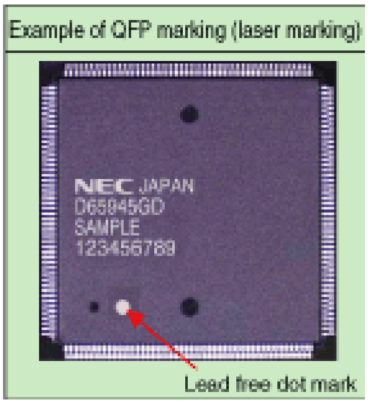
Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 3.2.2 "Identification of Lead-Free Products" on page 34.

3.2.2 Identification of Lead-Free Products

Lead-Free products are marked with a dot "•". The marking methods are the paint or the laser (It doesn't sink in). The shape of lead-free marks is a circle.
Example:



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