Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3620m2gca2-ueu-ax

Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Table of Contents

2. Electrical Specifications

This product has to be used only under the conditions of VDD=EVDD. Operation is not ensured at the time of using this product except this condition.

The operating ambient temperature of each quality grade is as follows:
(A)-Grade: Ta = -40 to +85°C
(A1)-Grade: Ta = -40 to +110°C
(A2)-Grade: Ta = -40 to +125°C

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Conditions			Rating	Unit
Supply voltage	VDD	VDD=EVDD,			-0.5 to +6.5	V
	EVDD	VDD=EVDD			-0.5 to +6.5	
	AVREF0				-0.5 to +6.5	
	VSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	EVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
	AVSS	VSS=EVSS=AVSS			-0.5 to +0.5	
Input voltage	VI1	Pin Group 1x, 2x, 6			-0.5 to EVDD+0.5 Note1	V
	VI3	Pin Group 7			-0.5 to VRO+0.5 Note1	
Analog input voltage	VIAN	Pin Group 4			-0.5 to AVREF0+0.5 Note1	V
High level output current	IOH	Pin Group 1x, 2x	1 pin		-4	mA
			Total	(A)	-50	
				(A1)	-20	
				(A2)	-20	
		Pin Group 4	1 pin		-4	
			Total	(A)Note2	-20	
				(A1)Note2	-10	
				(A2)Note3	-10	
Low level output current	IOL	Pin Group 1x, 2x	1 pin		4	mA
			Total	(A)	50	
				(A1)	20	
				(A2)	20	
		Pin Group 4	1 pin		4	
			Total	(A)Note2	20	
				(A1)Note2	10	
				(A2)Note3	10	
Operating ambient temperature	Ta	Normal operating mode		(A)	-40 to +85	°C
		Flash programming mode				
		Normal operating mode		(A1)	-40 to +110	
		Flash programming mode				
		Normal operating mode		(A2)	-40 to +125	
		Flash programming mode				
Storage temperature	Tstg				-40 to +125	°C

Remarks: 1. The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified

Notes: 1. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.
2. Excluding ADC IAREF0 current.
3. Including ADC IAREF0 current.

2.2 Capacities

(Ta = 25°C, VDD = EVDD = AVREF0 = VSS = EVSS = AVSS = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input/output capacitance	CIO	f=1MHz, Not measured pins is 0V.			10	pF

2.3 Operating condition

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f_{VBCLK})	Supply voltage	Operating Condition
$4.0 \le f_{xx} \le 20$MHz Note1	3.5V≤VDD≤5.5V Note1	Operation of functions is enabled
	3.3V≤VDD<3.5V	The following functions are operable: • CPU • Flash (including programming • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI
	3.3V≤AVRF0≤5.5V	• A/D Converter • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0) • Refer to chapter '2.8 A/D Converter' for details.
32kHz≤f_{XT}≤35kHz (Crystal)	3.3V≤VDD<5.5V Note1	-
12.5kHz≤f_{XT}≤27.5kHz Note2 (RC)		
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note1	-

Notes: 1. VDD = EVDD

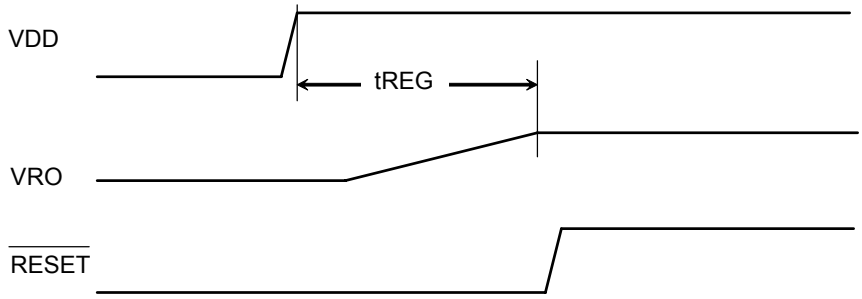
2. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.4 Voltage Regulator Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage	VDD		3.5		5.5	V
		Limited function see '2.3 Operating condition'	3.3			V
Output voltage	VRO			2.5		V
Output voltage stabilization time	t_{REG} Note	After VDD reaches voltage range min. 3.3V To connect C=4.7uF on REGC terminal			1	ms

Note: In case of non-POC device, be sure to start VDD in the state of $\overline{\text{RESET}}$=VSS=0V. For POC devices there is no need to control external $\overline{\text{RESET}}$ terminal. For decives with POC function the internal $\overline{\text{RESET}}$ signal will automatically controlled until VRO is stable.



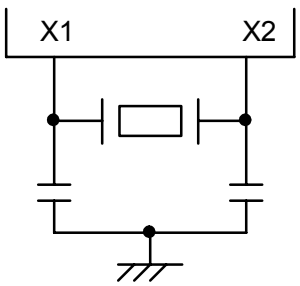
2.5 Clock Generator Circuit

2.5.1 Main System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal / Ceramic resonator	Refer to figure below	Oscillator frequency (fx) Note1		4		16	MHz
		Oscillation stabilization time Note2	After STOP mode	54 Note4	Note3		µs
			After IDLE2 mode	54 Note4	Note3		µs

Notes: 1. Indicates only oscillation circuit characteristics. Refer to '2.7 AC Characteristics' for CPU operation clock.
2. Time required to stabilize oscillation after VDD reaches oscillator voltage range MIN. 3.3V
3. Depends on the setting of the oscillation stabilization time select register (OSTS)
4. Minimum time required to stabilize flash. Time has to be secured by setting the oscillation stabilization time select register (OSTS)



2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Refer to Figure 1	Oscillator frequency (fxt)Note1		32	32.768	35	kHz
		Oscillation stabilization time Note2				10	s

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

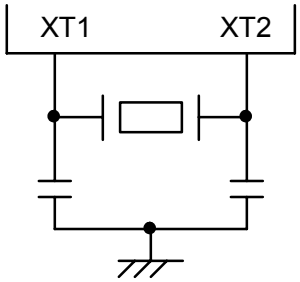
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequencyNote1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	µs

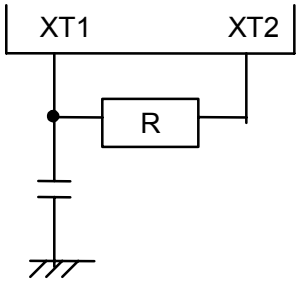
Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided (1/2) internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_{RL}	240kHz Internal-OSC	204	240	276	kHz
	f_{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation stabilization time		240kHz Internal-OSC		10	36	µs
		8MHz Internal-OSC	51	92	256	µs

2.5.4 PLL Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	fx		4		16	MHz
	f_{PLLI}	Note1	3		6	MHz
Output frequency	fxx		10		20	MHz
Lock time	tPLL	After VDD reaches voltage range min. 3.3V			800	µs
Output period jitter Note2	tpj	Peak to peak			2.0	ns

Notes: 1. The input of the PLL (f_{PLLI}) can be set to f_X, $f_X/2$, or $f_X/4$. The divider is set through an option byte in the code flash memory.

2. Not tested in production.

2.6.2 PIN leakage current

(C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.			Unit
						(A)	(A1)	(A2)	
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.2	0.4	0.5	µA
			Other pins Note1			0.5	0.8	1.0	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins Note1			-0.5	-0.8	-1.0	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.2	0.4	0.5	
			Other pins			0.5	0.8	1.0	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins			-0.5	-0.8	-1.0	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current :
- (A)-Grade 2.0µA
- (A1)-Grade 4.0µA
- (A2)-Grade 5.0µA

Low level input leakage current:
- (A)-Grade -2.0µA
- (A1)-Grade -4.0µA
- (A2)-Grade 5.0µA

2.6.3 Power supply current

2.6.3.1 FF3-L µPD70F3615, µPD70F3616, µPD70F3617, µPD70F3618, µPD70F3619

(a) Absolute values

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition				TYP.	MAX.			Unit
							(A)	(A1)	(A2)	
Operating mode Note2	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	16	24			mA
					f_{xx}=20MHz f_x=10MHz	25	35			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	12	19			mA
					f_{xx}=16MHz f_x=16MHz	20	28			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	22	32			mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	13	-			mA
					f_{xx}=20MHz f_x=10MHz	21				mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	11				mA
					f_{xx}=16MHz f_x=16MHz	18				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	21				mA

Mode	Symbol	Condition				TYP.	MAX.			Unit
							(A)	(A1)	(A2)	
HALT mode	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	10	15			mA
					f_{xx}=20MHz f_x=10MHz	17	25			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	7	11			mA
					f_{xx}=16MHz f_x=16MHz	12	18			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	14	21			mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	7	-			mA
					f_{xx}=20MHz f_x=10MHz	12				mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	5				mA
					f_{xx}=16MHz f_x=16MHz	9				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	11				mA

(b) Calculation formulas

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V[Note1])

Mode	Symbol	Condition			TYP. [Note8]	MAX. [Note8]			Unit
						(A)	(A1)	(A2)	
Operating mode [Note2]	IDD1	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.93·f_{xx}+6.3	1.12·f_{xx}+12.6			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.93·f_{xx}+4.7	1.12·f_{xx}+9.7			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.85·f_{xx}+5.2	1.03·f_{xx}+11.3			mA
		All peripherals stopped	Peripheral: ff_{xx-} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.78·f_{xx}+5.4	-			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.80·f_{xx}+4.9				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.76·f_{xx}+5.4				mA
HALT mode	IDD2	All peripherals running	Peripheral: ff_{xx-} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.70·f_{xx}+3.0	0.97*f_{xx}+5.2			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.65·f_{xx}+1.9	0.90*f_{xx}+3.6			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.54·f_{xx}+2.8	0.63*f_{xx}+8.60			mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	0.46·f_{xx}+2.8	-			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	0.44·f_{xx}+1.6				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	0.46·f_{xx}+1.8				mA
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running		PLL: OFF 4MHz≤f_{xx}≤16MHz	0.092·f_{xx}+0.90	0.128·f_{xx}+ 1.52	0.128·f_{xx}+ 1.82	0.128·f_{xx}+ 2.12	mA
		All peripherals stopped			0.035·f_{xx}+1.01	-			mA
IDLE2 mode	IDD4	PLL: OFF 4MHz ≤f_{xx}≤16MHz [Note7]			0.037·f_{xx}+0.21	0.049·f_{xx}+ 0.43	0.049·f_{xx}+ 0.63	0.049·f_{xx}+ 0.88	mA

Notes: 1. VDD and EVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash is in read mode.
When the device is in programming mode (Self-programming mode) the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]

3. Main OSC is stopped.

4. Do not use SubOSC.

5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.

6. RC Oscillation frequency is typ.40kHz. This clock is divided by 1/2 internally.

7. 8MHz Internal-OSC is stopped

8. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.7.2 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.3 Key Return Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Timer Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1]			10	MHz

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 CSI Timing

(a) Master mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

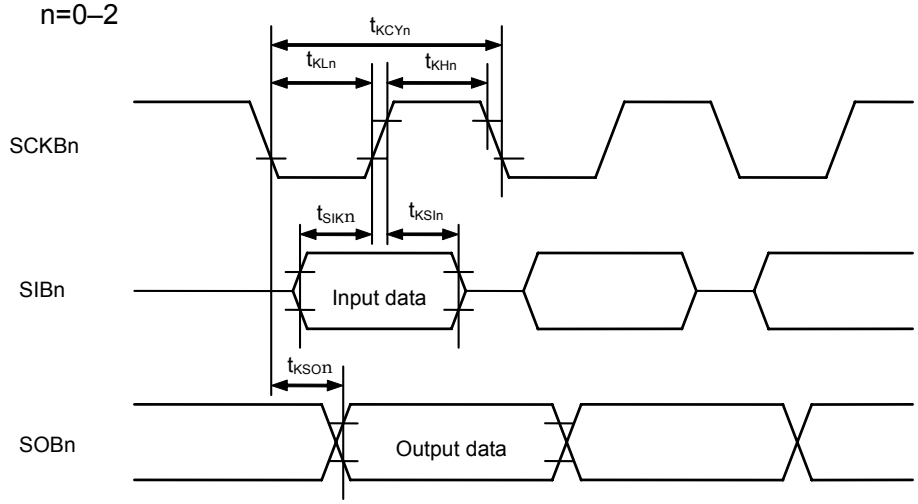
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–2



2.7.6 UART Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

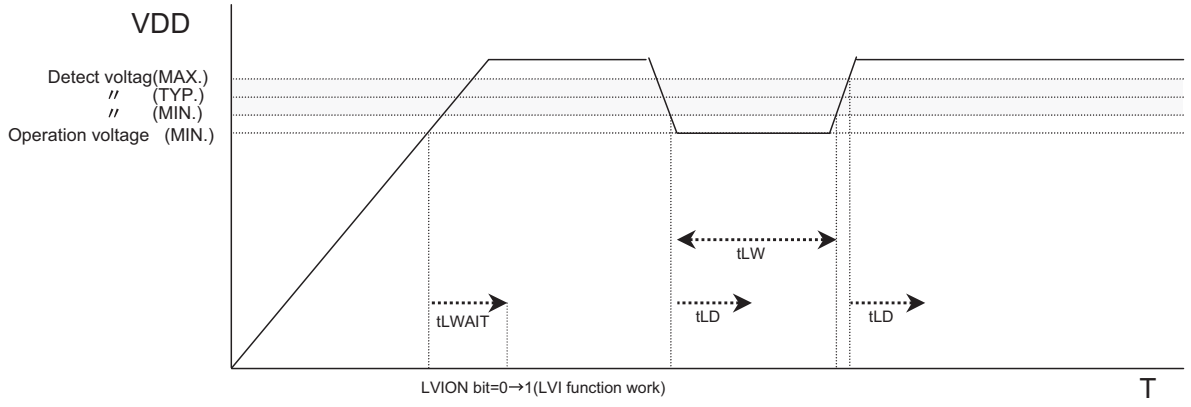
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

2.10 LVI

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VLVI0		3.8	4.0	4.2	V
	VLVI1		3.5	3.7	3.9	V
Response time Note1	tLD	After VDD reaches VLVI0/1(max). After VDD drop VLVI0/1(min).		0.2	2.0	ms
VDD minimum width	tLW		0.2			ms
Reference voltage stabilization wait time Note2	tLWAIT	After VDD reaches 3.3V. After LVION bit (LVIM.bit7) = 0->1		0.1	0.2	ms

Notes: 1. From detect voltage to occurrence interrupt/reset signal
2. If POC functionality is available, the wait time is not needed.

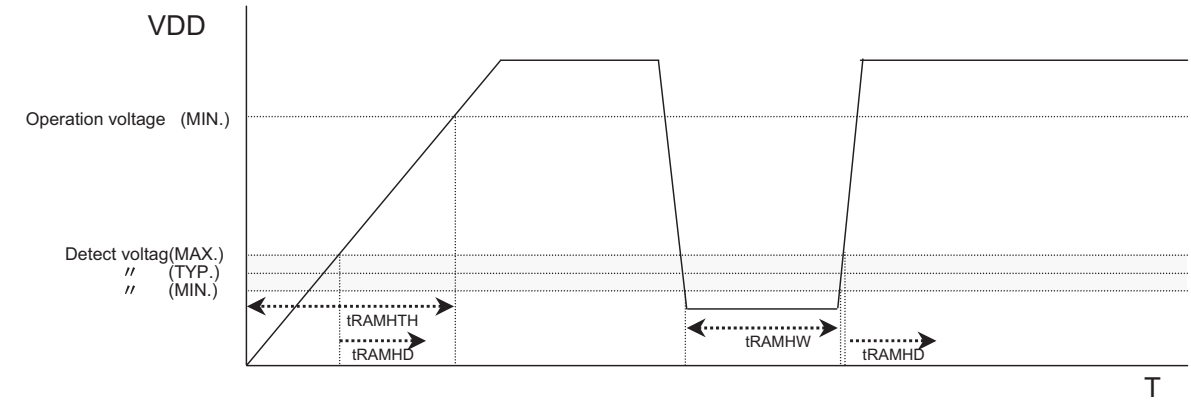


2.11 RAM Retention Flag

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VRAMH		1.9	2.0	2.1	V
Supply voltage rise time	tRAMHTH	From VDD=0V to VDD=3.3V	0.002		1800	ms
Response time Note1	tRAMHD	After VDD reaches 2.1V.		0.2	2.0	ms
VDD minimum width	tRAMHW		0.2			ms

Notes: 1. From detect voltage to set RAMFbit (RAMS.bit0)

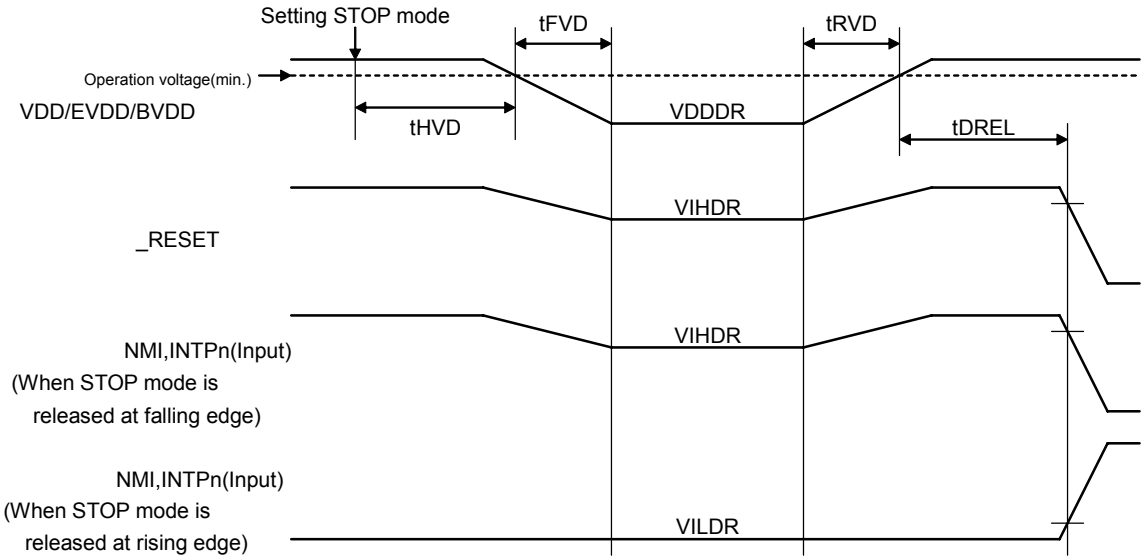


2.12 Data Retention Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V) (

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	VDDDR	STOP mode (All function is stopped)	1.9		5.5	V
Data retention power supply current	IDDDR	VDDDR=2.0V(All function is stopped)		6.5	70	μA
Supply voltage rise time	tRVD		1			μs
Supply voltage fall time	tFVD		1			μs
Supply voltage hold time	tHVD	After STOP mode	0			ms
STOP release signal input time	tDREL	After VDD reaches operating voltage range MIN. 3.3V	0			ms
Data retention high-level input voltage	VIHDR	All input port	0.9·VDDDR		VDDDR	V
Data retention low-level input voltage	VILDR	All input port	0		0.1·VDDDR	V

Remark: When STOP mode is entered/released operation voltage range must be controlled.



2.13 Flash Memory Programming Characteristics

(a) Basic Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V)

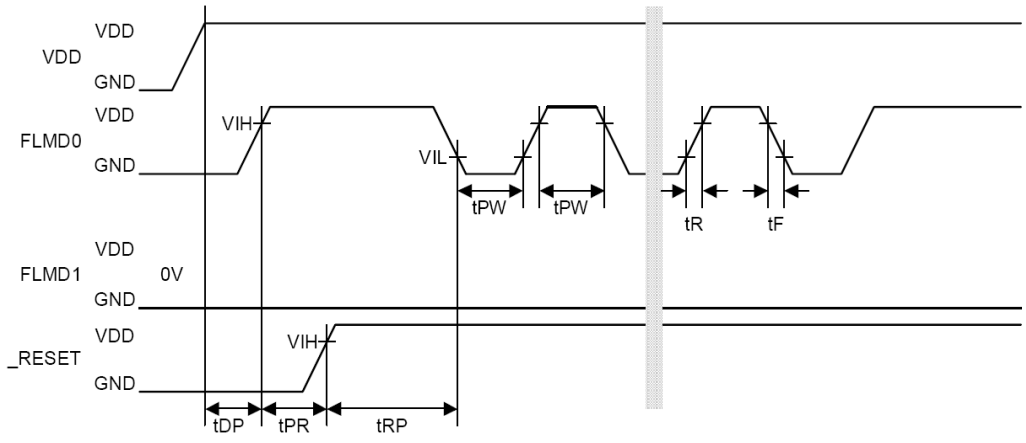
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.			Unit
					(A)	(A1)	(A2)	
Operation frequency	fCPU		4		20			MHz
Supply voltage	VDD		3.3		5.5			V
Number of rewrites	CWRT	Code Flash			1000			count
High level input voltage	VIH	FLMD0	0.8·EVDD		EVDD			V
Low level input voltage	VIL	FLMD0	EVSS		0.2·EVDD			V
Programming temperature	tPRG		-40		+85	+110	+125	°C
Data retention		Code Flash	15					year

Remark: The initial write when the product is shipped, any erase → write set of operations, or any programming operation is counted as one rewrite.
Example: P: Program(write) E: Erase
Product is shipped → P → E → P → E → P : Rewrite count: 3
Product is shipped → E → P → E → P → E → P : Rewrite count: 3

(b) Serial Writing Operation Characteristics

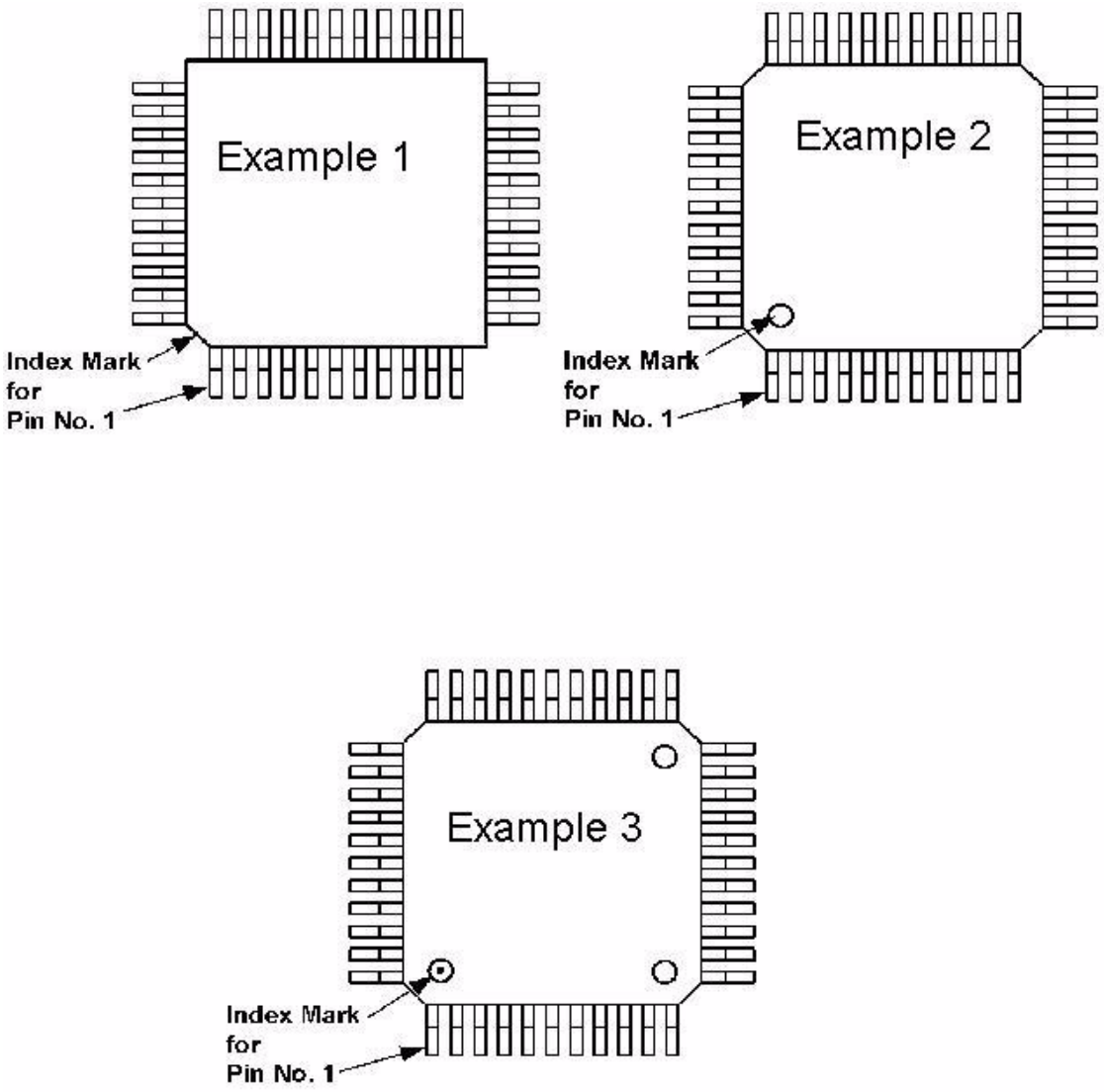
(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0 setup time (from VDD)	tDP		1			ms
$\overline{\text{RESET}}$ release (from FLMD0)	tPR		2			ms
FLMD0 pulse input start (from raise edge of _RESET)	tRP		800			µs
FLMD0 high level width / low level width	tPW		10		100	µs
FLMD0 raise time	tR				50	ns
FLMD0 fall time	tF				50	ns



3.2 Product Marking

3.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 3.2.2 "Identification of Lead-Free Products" on page 34.

4. Change History

Version	Chapter	Comment
V1.0		Initial release

[MEMO]