Renesas Electronics America Inc - UPD70F3621M2GCA-UEU-AX Datasheet

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1. Pin Group Information

1.1 Device package information

The V850ES/Fx3-L device series comprises several members. An overview with the pin and package information is given in the following table:

Series Member	# Pins	Device package information
µPD70F3610 µPD70F3611 µPD70F3612 µPD70F3613 µPD70F3614	64	FE3-L
µPD70F3615 µPD70F3616 µPD70F3617 µPD70F3618 µPD70F3619	80	FF3-L
µPD70F3620 µPD70F3621 µPD70F3622	100	FG3-L

This document describes the specification for the V850ES/FF3-L.

1.2 Pin Groups 1x: Pins supplied by EVDD

1B: (SHMT1)
- P04, P30-31, P34; P40, P91, P913-915 (FE3-L)
- P04, P30-31, P34; P38-39, P40, P91, P913-915 (FF3-L)
- P04, P30-31, P34; P36-39, P40, P91, P911, P913-915 (FG3-L)

1D: (SHMT3)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FE3-L)
- P00-03, P05-P06, P32-33, P35, P41-42, P50-55, P90, P96-99 (FF3-L)
- P00-03, P05-P06, P10-11, P32-33, P35, P41-42, P50-55, P90, P92-910, P912 (FG3-L)

1.3 Pin Groups 2x: Pins supplied by EVDD

2A: (CMOS)
- PCM0-1 (FE3-L)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FF3-L)

2D: (SHMT3)
- PDL0-7 (FE3-L)
- PDL0-11 (FF3-L)

1.4 Pin Groups 3x: Pins supplied by BVDD

3A: (CMOS)
- PCM0-3, PCS0-1, PCT0-1, PCT4, PCT6 (FG3-L)

3D: (SHMT3)
- PDL0-13 (FG3-L)

1.5 Pin Groups 4: Pins supplied by AVREF0

4: (CMOS)
- P70-79 (FE3-L)
- P70-711 (FF3-L)
- P70-715 (FG3-L)

1.6 Pin Groups 6: Pins supplied by EVDD

- RESET (SHMT2)
- IC, FLMD0

1.7 Pin Groups 7: Pins supplied by VRO

- X1, X2, XT1, XT2

2.2 Capacities

(Ta = 25°C, VDD = EVDD = AVREF0 = VSS = EVSS = AVSS = 0V)

Parameter	**Symbol**	Conditions	MIN.	TYP.	MAX.	Unit
Input/output capacitance	CIO	f=1MHz, Not measured pins is 0V.			10	pF

2.3 Operating condition

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Internal System clock frequency (f_{VBCLK})	Supply voltage	Operating Condition
$4.0 \le f_{xx} \le 20$MHz Note1	3.5V≤VDD≤5.5V Note1	Operation of functions is enabled
	3.3V≤VDD<3.5V	The following functions are operable: • CPU • Flash (including programming • RAM • IO Buffer • Port • WT • WDT • INT • CLM • POC • LVI
	3.3V≤AVRF0≤5.5V	• A/D Converter • stop ADC for AVREF0 < 4.0V (ADA0CE bit =0) • Refer to chapter '2.8 A/D Converter' for details.
32kHz≤f_{XT}≤35kHz (Crystal)	3.3V≤VDD<5.5V Note1	-
12.5kHz≤f_{XT}≤27.5kHz Note2 (RC)		
f_{RL} (240kHz Internal-OSC)	3.3V≤VDD<5.5V Note1	-

Notes: 1. VDD = EVDD

2. RC Oscillation frequency is min. 25kHz max. 55kHz. This clock is divided by 2 internally.

2.5.2 Sub System Clock Oscillation Circuit Characteristics

(Ta = -40 to +85°C, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	Refer to Figure 1	Oscillator frequency (fxt)Note1		32	32.768	35	kHz
		Oscillation stabilization time Note2				10	s

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

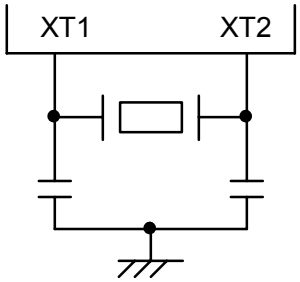
Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator	Refer to Figure 2	Oscillator frequencyNote1,4	R=390KΩ ±5% Note3, C=47pF±10% Note3	25	40	55	kHz
		Oscillation stabilization time Note2				100	µs

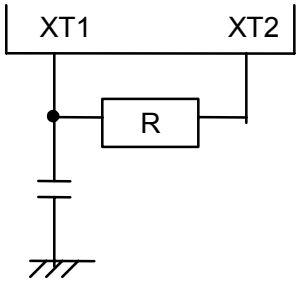
Notes: 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristic" for cpu operation clock.

2. Time required to stabilize oscillation after VDD reaches oscillator voltage range min. 3.3V

3. In order to avoid the influence of wiring capacity, shorten wiring as much as possible.

4. RC Oscillation frequency is typ. 40kHz. This clock is divided (1/2) internally. In case of RC Oscillator, internal system clock frequency (fxt) is min. 12.5kHz, typ. 20kHz, max. 27.5kHz.





2.5.3 Internal-OSC Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output frequency	f_{RL}	240kHz Internal-OSC	204	240	276	kHz
	f_{RH}	8MHz Internal-OSC	7.2	8.0	8.8	MHz
Oscillation stabilization time		240kHz Internal-OSC		10	36	µs
		8MHz Internal-OSC	51	92	256	µs

2.6.2 PIN leakage current

(C=4.7uF, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.			Unit
						(A)	(A1)	(A2)	
High level input leakage current	ILIH1	VI=VDD	Analog pins			0.2	0.4	0.5	µA
			Other pins Note1			0.5	0.8	1.0	
Low level input leakage current	ILIL1	VI=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins Note1			-0.5	-0.8	-1.0	
High level output leakage current	ILOH1	VO=VDD	Analog pins			0.2	0.4	0.5	
			Other pins			0.5	0.8	1.0	
Low level output leakage current	ILOL1	VO=0V	Analog pins			-0.2	-0.4	-0.5	
			Other pins			-0.5	-0.8	-1.0	

Notes: 1. The input leakage current of FLMD0 is as follows:
High level input leakage current :
- (A)-Grade 2.0µA
- (A1)-Grade 4.0µA
- (A2)-Grade 5.0µA

Low level input leakage current:
- (A)-Grade -2.0µA
- (A1)-Grade -4.0µA
- (A2)-Grade 5.0µA

Mode	Symbol	Condition				TYP.	MAX.			Unit
							(A)	(A1)	(A2)	
HALT mode	IDD2	All peripherals running	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	10	15			mA
					f_{xx}=20MHz f_x=10MHz	17	25			mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	7	11			mA
					f_{xx}=16MHz f_x=16MHz	12	18			mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	14	21			mA
		All peripherals stopped	Peripheral: f_{xx} PRSI option: 0	PLL: ON 16MHz≤f_{xx}≤20MHz	f_{xx}=10MHz f_x=5MHz	7	-			mA
					f_{xx}=20MHz f_x=10MHz	12				mA
				PLL: OFF 4MHz≤f_{xx}≤16MHz	f_{xx}=8MHz 8MHz Internal-OSC Note3	5				mA
					f_{xx}=16MHz f_x=16MHz	9				mA
			Peripheral: f_{xx}/2 PRSI option: 1	PLL: ON 10MHz≤f_{xx}≤20MHz	f_{xx}=20MHz f_x=10MHz	11				mA

Mode	Symbol	Condition			TYP.	MAX. (A)	MAX. (A1)	MAX. (A2)	Unit
IDLE1 mode	IDD3	Peripheral (TAA, UARTD) running	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.4	2.2	2.5	2.8	mA
				f_{xx}=12MHz f_x=12MHz	2.0	3.1	3.4	3.7	mA
				f_{xx}=16MHz f_x=16MHz	2.4	3.6	3.9	4.2	mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.5	2.3	2.6	2.9	mA
		All peripherals stopped	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7	f_{xx}=5MHz f_x=5MHz	1.2	-			mA
				f_{xx}=12MHz f_x=12MHz	1.4				mA
				f_{xx}=16MHz f_x=16MHz	1.6				mA
			fxx=8MHz, 8MHz Internal-OSC Note3		1.1				mA
IDLE2 mode	IDD4	PLL: OFF 4MHz≤f_{xx}≤16MHz Note7		f_{xx}=5MHz f_x=5MHz	0.4	0.7	0.9	1.1	mA
				f_{xx}=12MHz f_x=12MHz	0.7	1.0	1.2	1.5	mA
				f_{xx}=16MHz f_x=16MHz	0.8	1.2	1.4	1.7	mA
		fxx=8MHz, 8MHz Internal-OSC Note3			0.2	0.5	0.7	1.0	mA
SUB operating mode Note5	IDD5	Crystal resonator (fxt = 32,768kHz)			80	400	-	-	μA
		RC resonator (fxt=20kHz) Note6			80	400	600	850	μA
		240 kHz Internal-OSC (SubOSC stopped)			220	1000	1200	1450	μA
SubIDLE mode Note3,5	IDD6	Crystal resonator (fxt = 32,768kHz)			20	190	-	-	μA
		RC resonator (fxt=20kHz) Note6			40	220	420	670	μA
		240kHz Internal-OSC (SubOSC stopped)			25	180	380	630	μA
STOP mode Note3,4	IDD7	POC stop	240kHz Internal-OSC stop		7.5	80	280	530	μA
			240kHz Internal-OSC working		15.5	95	295	545	μA
		POC work	240kHz Internal-OSC stop		10.5	85	285	535	μA
			240kHz Internal-OSC working		18.5	100	300	550	μA

Notes: 1. VDD and EVDD total current. (Ports are stopped).
AVREF0 current, port buffer current (including a current flowing in the on-chip pull-up/pull-down resistor) are not included.

2. The code flash is in read mode.
When the device is in programming mode (Self-programming mode) the current value (MAX. value) adds by the following value:

- Self-programming mode:
  + In case of PLL OFF: 7-(0.33*fxx+0.1) [mA]
  + In case of PLL ON: 7-(0.18*fxx+3.0) [mA]

3. Main OSC is stopped.

4. Do not use SubOSC.

5. POC is working. 240kHz Internal-OSC is working. 8MHz Internal-OSC is stopped.

6. RC Oscillation frequency is typ.40kHz. This clock is divided by 1/2 internally.

7. 8MHz Internal-OSC is stopped

8. The formulas are for reference only. Not all possible values for f_{xx} are tested in the outgoing device inspection.

2.7.2 RESET, Interrupt, ADTRG Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
_RESET input low level width	tWRSL	analog filter	250			ns
NMI input high level width	tWNIH	analog filter	250			ns
NMI input low level width	tWNIL	analog filter	250			ns
INTPn[Note1] input high level width	tWITH	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns
INTPn [Note1] input low level width	tWITL	analog filter ,n=0-8	250			ns
		digital filter ,n=3	Note2			ns

Notes: 1. ADTRG is same spec (P03/INTP0/ADTRG). $\overline{\text{DRST}}$ is same spec (P05/INTP2/$\overline{\text{DRST}}$)

2. 2Tsamp+20 or 3Tsamp+20 ("Tsamp" is Noise reject sampling clock (NF macro))

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. $\overline{\text{RESET}}$, NMI, INTPn, ADTRG and $\overline{\text{DRST}}$ have analog noise filter. The typical filter time is typ=60ns.

2.7.3 Key Return Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.3 to 5.5V, AVREF0 = 3.3 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
KRn input high level width	tWKRH	analog filter ,n=0-7	250			ns
KRn input low level width	tWKRL	analog filter ,n=0-7	250			ns

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. KRn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.4 Timer Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TI input high level width	tTIH	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TI input low level width	tTIL	TIAA00-01,10-11,20-21,30-31,40-41 [Note1]	250			ns
TO output cycle	tTCYK	TIAA00-01,10-11,20-21,30-31, 40-41 [Note1]			10	MHz

Notes: 1. Except for the external trigger and external event function.

Remarks: 1. The above minimum values show pulse widths that are surely detected as an effective edge. An effective may also be detected even if the input pulse width is less than the above minimum specification.

2. TIAAn inputs have analog noise filter. The typical filter time is typ=60ns.

2.7.5 CSI Timing

(a) Master mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

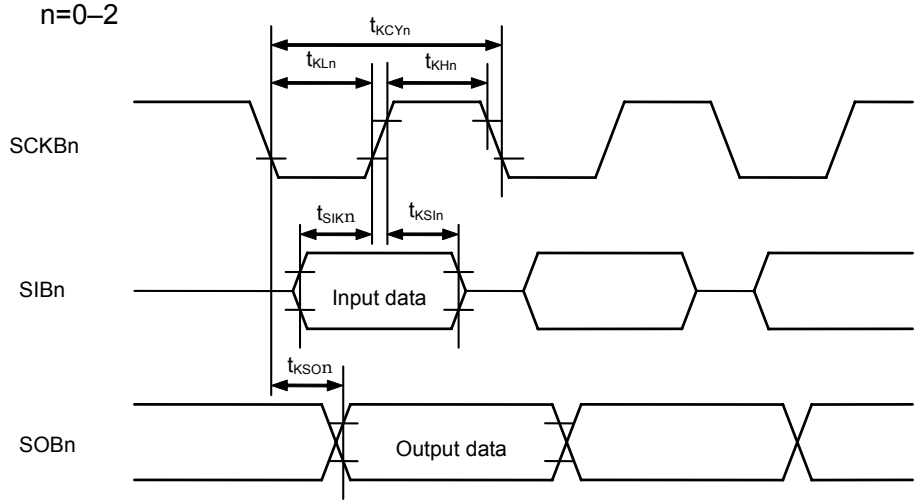
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		125		ns
SCKBn high level width	tKH1		tKCY1/2-15		ns
SCKBn low level width	tKL1		tKCY1/2-15		ns
SIBn setup time (to SCKBn)	tSIK1		30		ns
SIBn hold time (from SCKBn)	tKSI1		25		ns
Delay time from SCKBn to SOBn	tKSO1			25	ns

(b) Slave mode

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKBn cycle time	tKCY1		200		ns
SCKBn high level width	tKH1		90		ns
SCKBn low level width	tKL1		90		ns
SIBn setup time (to SCKBn)	tSIK1		50		ns
SIBn hold time (from SCKBn)	tKSI1		50		ns
Delay time from SCKBn to SOBn	tKSO1			50	ns

CSIBn n=0–2



2.7.6 UART Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					1.5	Mbps
ASCK0 frequency					10	MHz

2.7.7 IIC Timing

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 3.5 to 5.5V, VSS = EVSS = AVSS = 0V, CL=50pF)

Parameter		Symbol	Normal mode		High-speed mode		Unit
			min.	max.	min.	max.	
SCL00 clock frequency		fCLK	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		tBUF	4.7		1.3		µs
Hold time[Note1]		tHD:STA	4.0		0.6		µs
SCL00 clock low-level width		tLOW	4.7		1.3		µs
SCL00 clock high-level width		tHIGH	4.0		0.6		µs
Setup time for start/restart conditions		tSU:STA	4.7		0.6		µs
Data hold time	CBUS compatible master	tHD:DAT	5.0				µs
	IIC mode		0[Note2]		0[Note2]	0.9[Note3]	µs
Data setup time		tSU:DAT	250		100[Note4]		ns
SDA00 and SCL00 signal rise time		tR		1000	20+0.1Cb	300	ns
SDA00 and SCL00 signal fall time		tF		300	20+0.1Cb	300	ns
Stop condition setup time		tSU:STO	4.0		0.6		µs
Pilse width with spike supporessed by input filter		tSP			0	50	ns
Capacitance load of each bus line		Cb		400		400	pF

Notes: 1. At the start condition, the first clock pulse is generated after the hold time

2. The system requires a minimum of 300ns hold time Internally for the SDA signal (at VIH-min. of SCL00 signal)
In order to occupy the undefined area at the falling edge of SCL00.

3. If the system does not extend the SCL00 signal low hold time (tlow), only the maximum data hold time (tHD:DAT) needs to be satisfied.

4. The high-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the high-speed-mode IIC bus so that It meets the following conditions.
- If the system does not extend the SCL00 signal's low state hold time:
SU:DAT?250ns
- If the system extends the SCL00 signal's low state hold time:
Transmit the following data bit to the SDA00 line prior to releasing the SCL00 line (tRmax.+tSU:DAT=1000+250=1250ns: Normal mode IIC bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

2.8 A/D Converter

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 3.5 to 5.5V, AVREF0 = 4.0 to 5.5V, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.		Unit
					(A),(A1)	(A2)	
Resolution					10		bit
Overall error[Note1]		4.0V≤AVREF0<5.5V		±0.15	±0.3	±0.35	%FSR
Conversion time	tCONV		3.10		16		µs
Stabilization time	tSTA	After ADA0PS bit = 0 -> 1	2				µs
Recovery time for power down mode	tDPU		1				µs
Zero-scale error[Note1]	ZSE				±0.3	±0.35	%FSR
Full-scale error[Note1]	FSE				±0.3	±0.35	%FSR
Integral non-liniearity error[Note2]	INL				±2.5		LSB
Differential non-liniearity error[Note2]	DNL				±1.5		LSB
Analog input voltage	VIAN		AVSS		AVREF0		V
Analog input equivalent circuit capacitance [Note3,4]	CINA				6.19		pF
Analog input equivalent circuit resistance [Note3]	RINA				2.55		kΩ
AVREF0 current	IAREF0	A/D operating		4	7		mA
		A/D operation stop		1	10		µA
Conversion rusult when using Diagnostic function		AVREF0 conversion	3FC		3FF		HEX
		AVSS conversion	000		003		HEX

Notes: 1. Overall error excluding quantization error (±0.05%FSE). It is indicated as a ratio to the full-scale value.

2. Excluding quantization error (±1/2 LSB)

3. Reference value. Not tested in production.

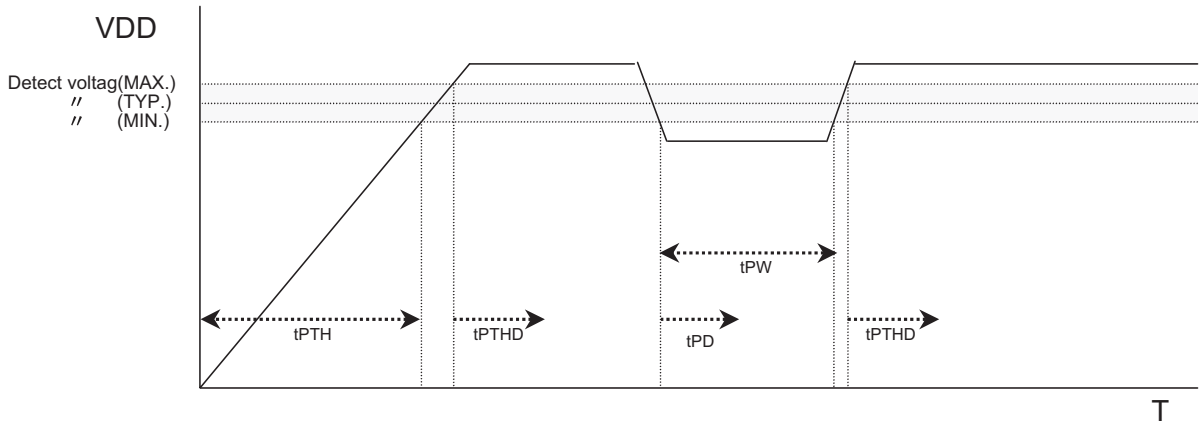
4. Does not include input/output capacitance CIO

2.9 POC

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD, VSS = EVSS = AVSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detect voltage	VPOC0		3.3	3.5	3.7	V
Supply voltage rise time	tPTH	From VDD=0V to VDD=3.3V	0.002			ms
Response time1 Note1	tPTHD	In case of power on. After VDD reaches 3.7V.			2.0	ms
Response time2 Note2	tPD	In case of power off. After VDD drop 3.3V.		0.2	1.0	ms
VDD minimum width	tPW		0.2			ms

Notes: 1. From detect voltage to release reset signal
2. From detect voltage to occurrence of reset signal



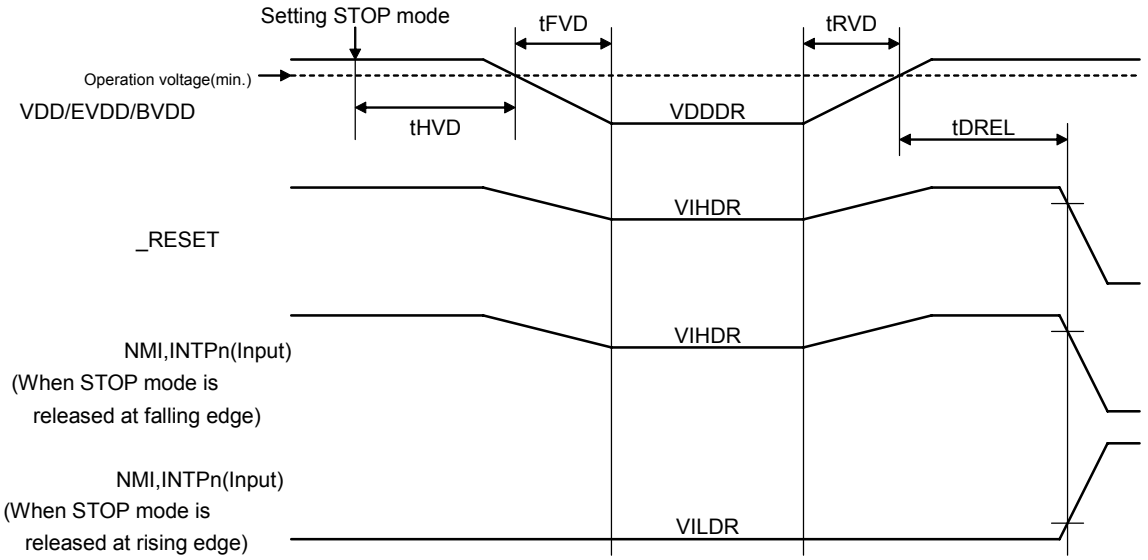
Note: POC is available only in M2 devices. Refer to 'Ordering information' in the V850ES/Fx3-L User'sManual.

2.12 Data Retention Characteristics

(Ta = -40 to +85°C for (A)-Grade, Ta = -40 to +110°C for (A1)-Grade, Ta = -40 to +125°C for (A2)-Grade, C=4.7uF, VDD = EVDD = 1.9 to 5.5V, VSS = EVSS = AVSS = 0V) (

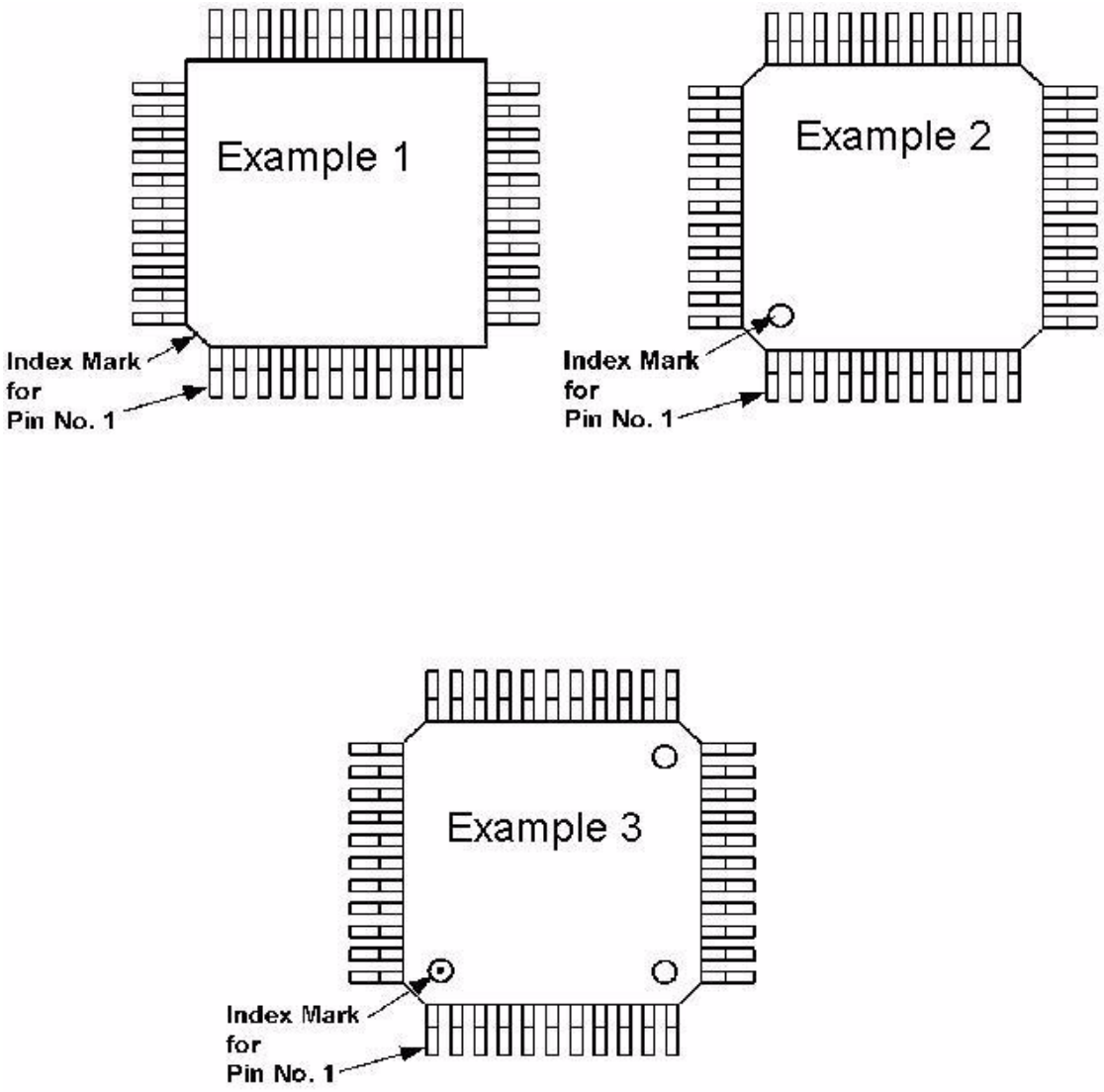
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	VDDDR	STOP mode (All function is stopped)	1.9		5.5	V
Data retention power supply current	IDDDR	VDDDR=2.0V(All function is stopped)		6.5	70	μA
Supply voltage rise time	tRVD		1			μs
Supply voltage fall time	tFVD		1			μs
Supply voltage hold time	tHVD	After STOP mode	0			ms
STOP release signal input time	tDREL	After VDD reaches operating voltage range MIN. 3.3V	0			ms
Data retention high-level input voltage	VIHDR	All input port	0.9·VDDDR		VDDDR	V
Data retention low-level input voltage	VILDR	All input port	0		0.1·VDDDR	V

Remark: When STOP mode is entered/released operation voltage range must be controlled.



3.2 Product Marking

3.2.1 Marking of pin 1 at a QFP (Quad Flat Package)



Example 1: The index mark for pin 1 is the beveled edge of the package

Example 2: The index mark for pin 1 is a round notch at one of the 4 edges. In this case, the shape of all edges is identical (usually beveled).

Example 3: For production reasons, two or more similar notches may be located at the top of the package. In such a case the index marker for pin 1 is a round notch with an additional mark in it.

Note: RoHS compliant devices have an additional dot at the top side. Do not mix it up with the marking for pin 1. For details see 3.2.2 "Identification of Lead-Free Products" on page 34.

4. Change History

Version	Chapter	Comment
V1.0		Initial release

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