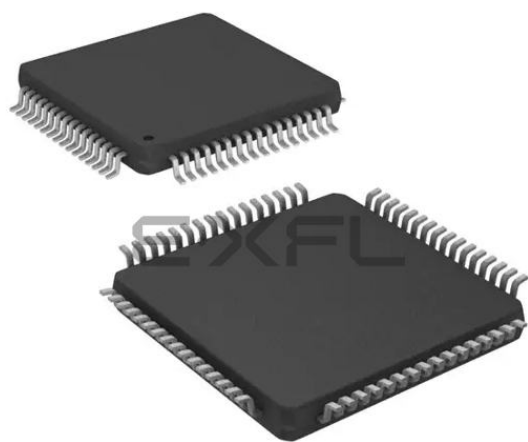




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.85V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg842f512-qfp64

1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32GG842 devices.

Table 1.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32GG842F512G-E-QFP64	512	128	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32GG842F1024G-E-QFP64	1024	128	48	1.98 - 3.8	-40 - 85	TQFP64

Adding the suffix 'R' to the part number (e.g. EFM32GG842F512G-E-QFP64R) denotes tape and reel.

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process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART[™], the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

2.1.16 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

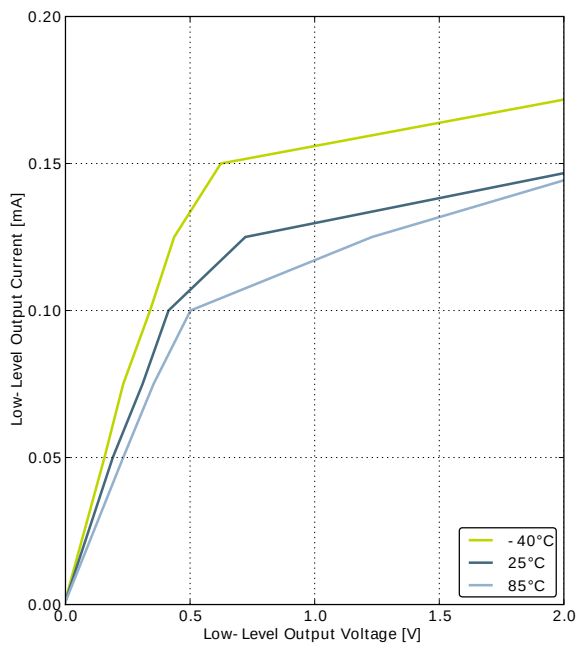
2.1.17 Low Energy Timer (LETIMER)

The unique LETIMER[™], the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

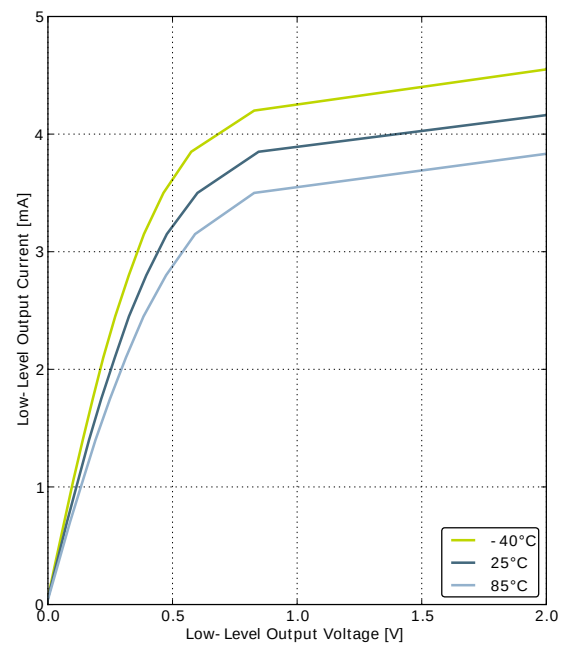
2.1.18 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

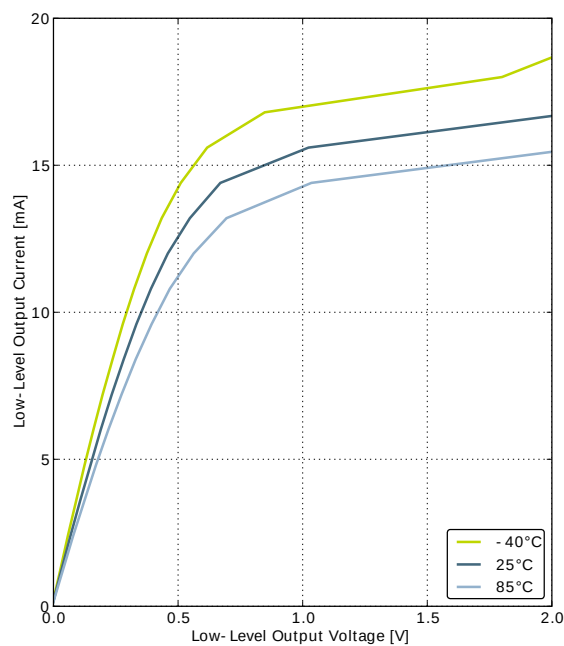
Figure 3.4. Typical Low-Level Output Current, 2V Supply Voltage



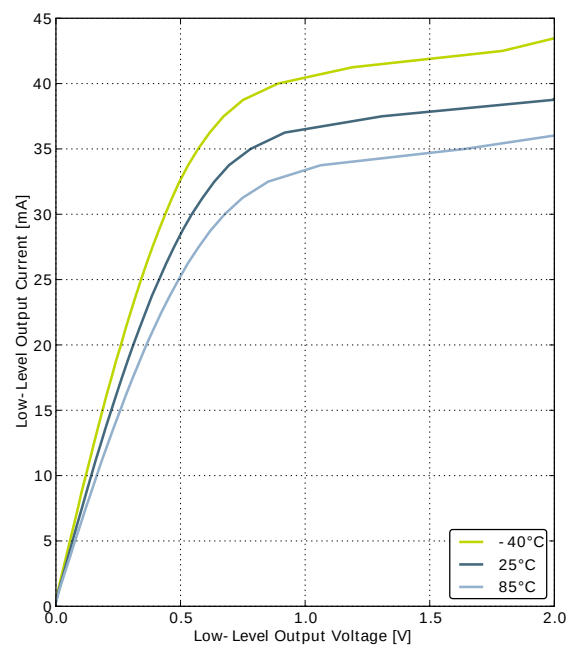
GPIO_Px_CTRL DRIVEMODE = LOWEST



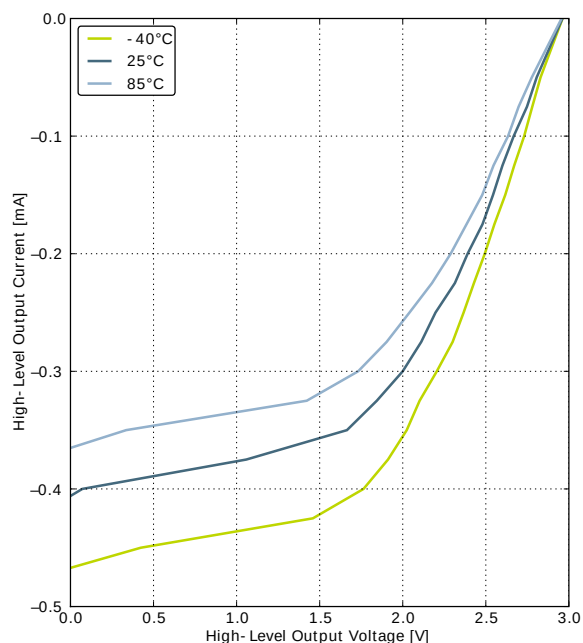
GPIO_Px_CTRL DRIVEMODE = LOW



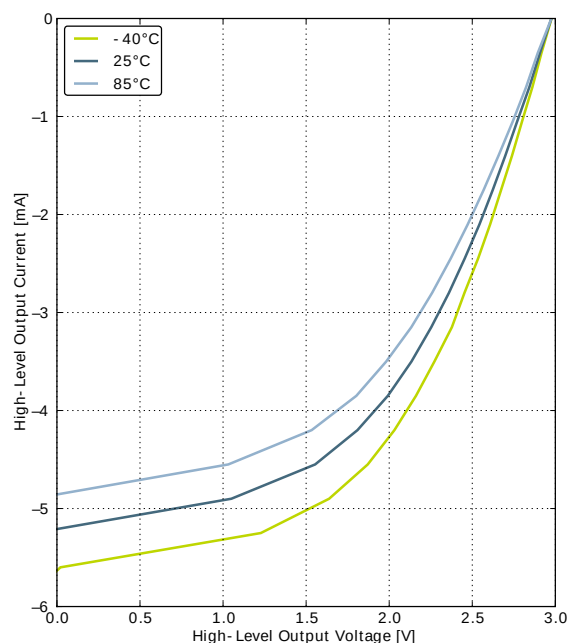
GPIO_Px_CTRL DRIVEMODE = STANDARD



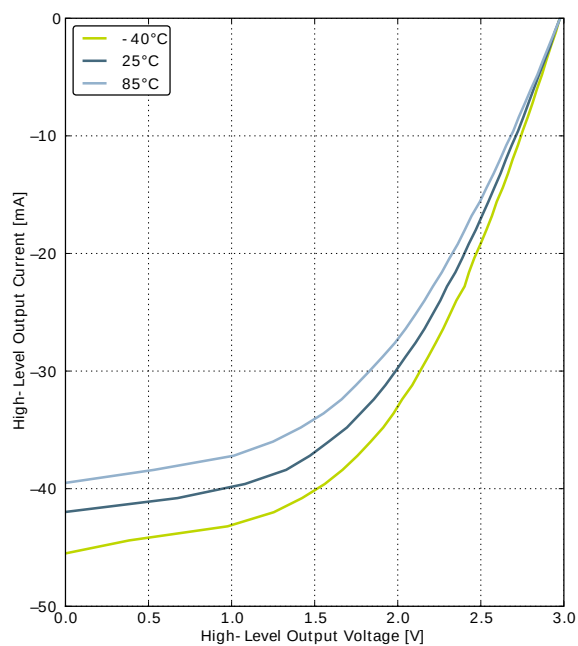
GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.7. Typical High-Level Output Current, 3V Supply Voltage

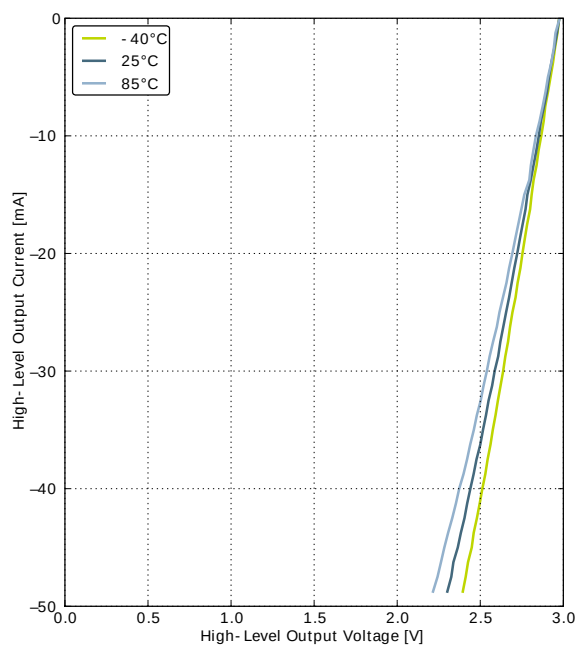
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

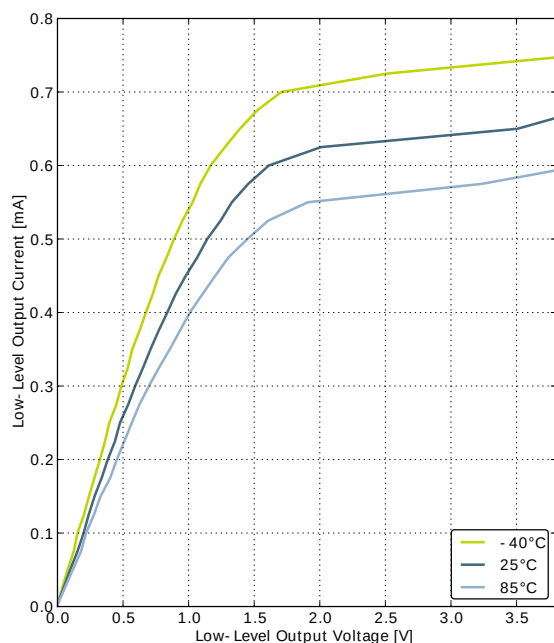


GPIO_Px_CTRL DRIVEMODE = STANDARD

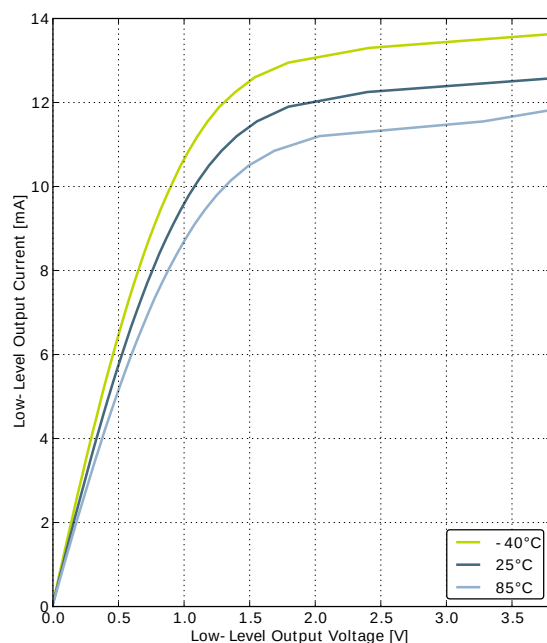


GPIO_Px_CTRL DRIVEMODE = HIGH

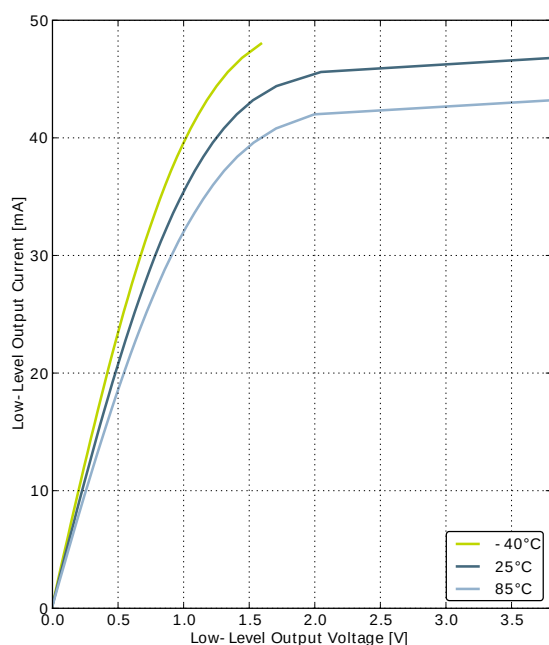
Figure 3.8. Typical Low-Level Output Current, 3.8V Supply Voltage



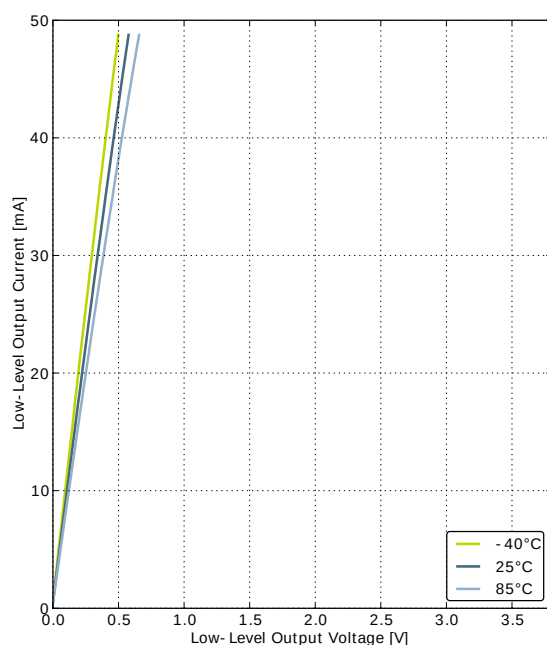
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

3.9.6 ULFRCO

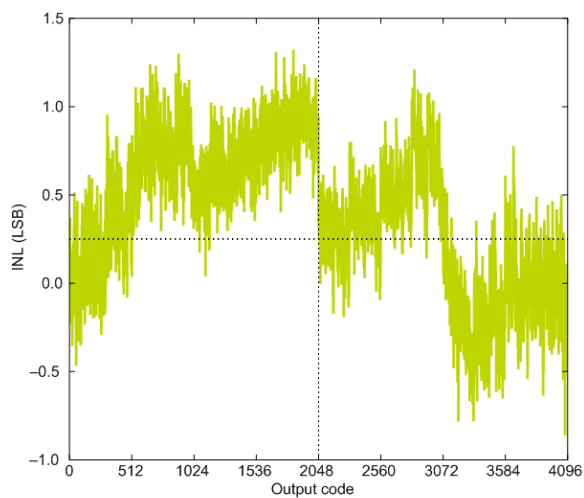
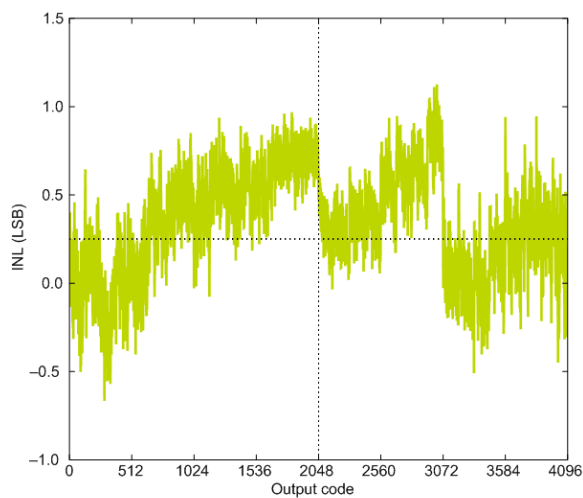
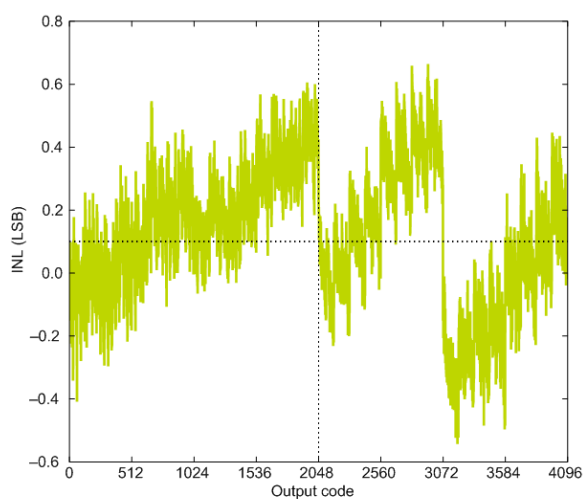
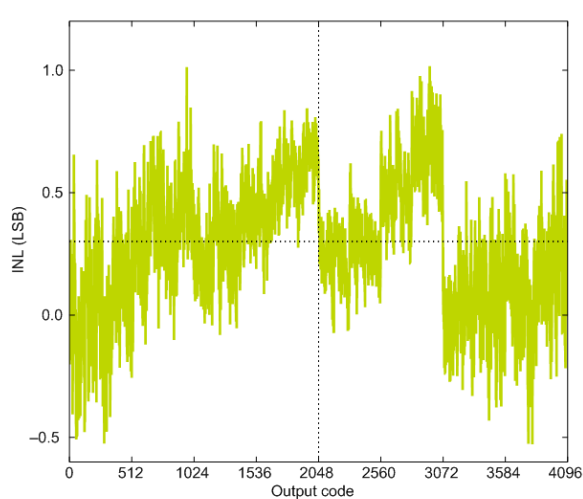
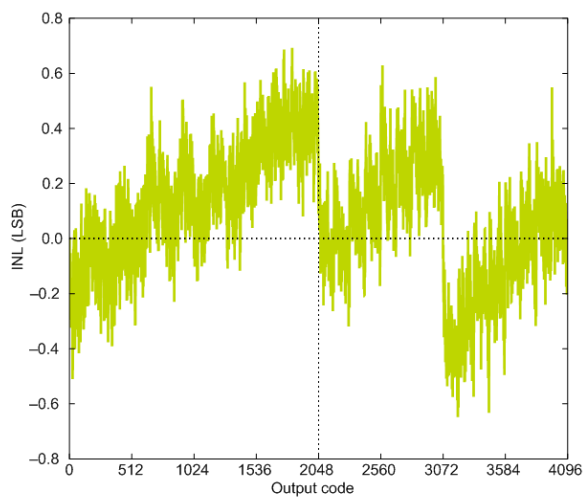
Table 3.13. ULFRCO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{ULFRCO}	Oscillation frequency	25°C, 3V	0.70		1.75	kHz
TC_{ULFRCO}	Temperature coefficient			0.05		%/°C
VC_{ULFRCO}	Supply voltage coefficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.14. ADC

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ADCIN}	Input voltage range	Single ended	0		V_{REF}	V
		Differential	$-V_{REF}/2$		$V_{REF}/2$	V
$V_{ADCREFIN}$	Input range of external reference voltage, single ended and differential		1.25		V_{DD}	V
$V_{ADCREFIN_CH7}$	Input range of external negative reference voltage on channel 7	See $V_{ADCREFIN}$	0		$V_{DD} - 1.1$	V
$V_{ADCREFIN_CH6}$	Input range of external positive reference voltage on channel 6	See $V_{ADCREFIN}$	0.625		V_{DD}	V
$V_{ADCCMIN}$	Common mode input range		0		V_{DD}	V
I_{ADCIN}	Input current	2pF sampling capacitors		<100		nA
$CMRR_{ADC}$	Analog input common mode rejection ratio			65		dB
I_{ADC}	Average active current	1 MSamples/s, 12 bit, external reference		351		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00		67		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01		63		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10		64		μA
I_{ADCREF}	Current consumption of internal voltage reference	Internal voltage reference		65		μA

Figure 3.20. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		58		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		59		dB
SNDR _{DAC}	Signal to Noise-pulse Distortion Ratio (SNDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		57		dB
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		54		dB
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		56		dB
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		53		dB
		500 kSamples/s, 12 bit, differential, V_{DD} reference		55		dB
SFDR _{DAC}	Spurious-Free Dynamic Range(SFDR)	500 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference		56		dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference		61		dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference		55		dBc
		500 kSamples/s, 12 bit, differential, V_{DD} reference		60		dBc
V _{DACOFFSET}	Offset voltage	After calibration, single ended		2	12	mV
		After calibration, differential		2		mV
DNL _{DAC}	Differential non-linearity			±1		LSB
INL _{DAC}	Integral non-linearity			±5		LSB
MC _{DAC}	No missing codes			12		bits

¹ Measured with a static input code and no loading on the output.

3.12 Operational Amplifier (OPAMP)

The electrical characteristics for the Operational Amplifiers are based on simulations.

Table 3.16. OPAMP

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{OPAMP}	Active Current	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, Unity Gain		350	405	μA
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, Unity Gain		95	115	μA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		196		μV_{RMS}
		$V_{out}=1V$, RESSEL=0, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		229		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=0		1230		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <10 kHz, OPAXHCMDIS=1		2130		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=0		1630		μV_{RMS}
		RESSEL=7, 0.1 Hz< f <1 MHz, OPAXHCMDIS=1		2590		μV_{RMS}

Figure 3.25. OPAMP Common Mode Rejection Ratio

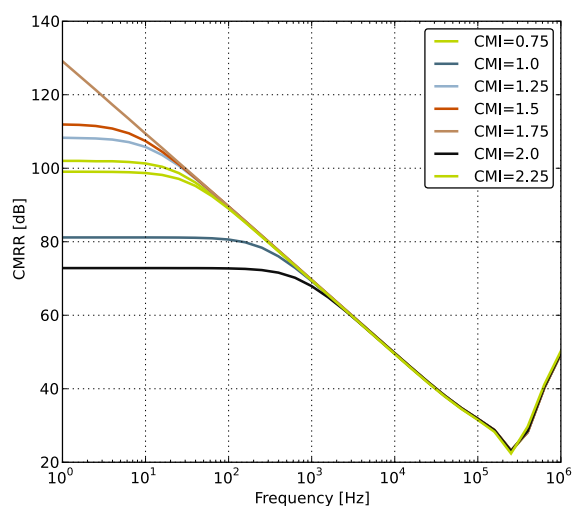


Figure 3.26. OPAMP Positive Power Supply Rejection Ratio

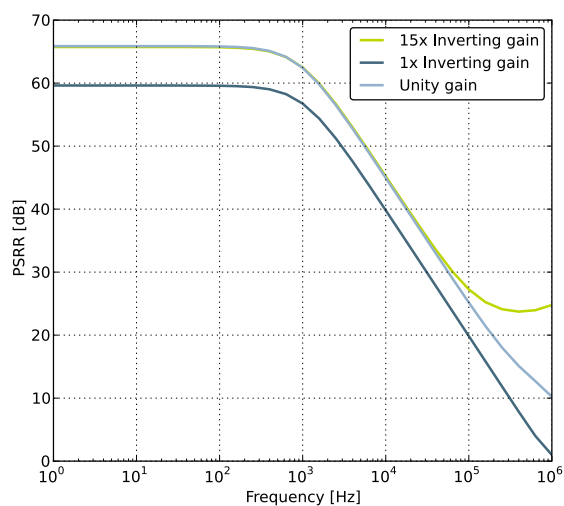
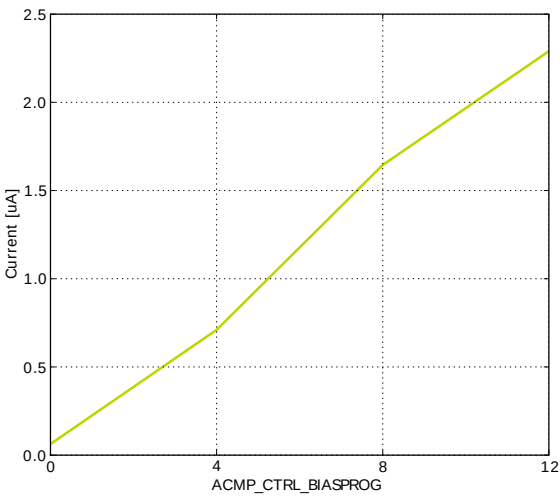
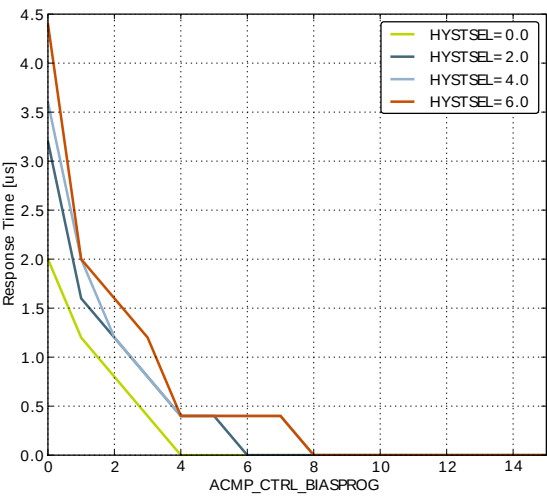


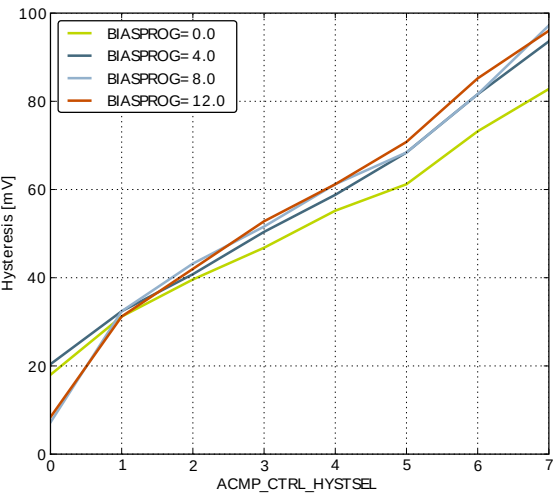
Figure 3.30. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



Current consumption, HYSTSEL = 4



Response time



Hysteresis

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	-	-
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	-	0.20	θ1	0°	-	-
C1	0.09	-	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1	10.0 BSC						
e	0.50 BSC						
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see:

<http://www.silabs.com/support/quality/pages/default.aspx>

5 PCB Layout and Soldering

5.1 Recommended PCB Layout

Figure 5.1. TQFP64 PCB Land Pattern

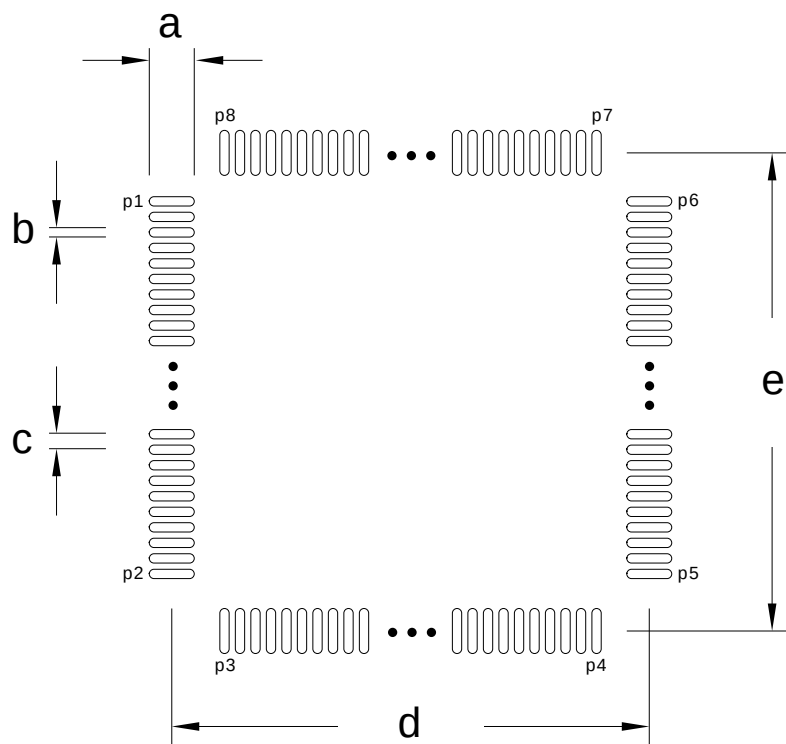


Table 5.1. QFP64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin number	Symbol	Pin number
a	1.60	P1	1	P6	48
b	0.30	P2	16	P7	49
c	0.50	P3	17	P8	64
d	11.50	P4	32	-	-
e	11.50	P5	33	-	-

Updated GPIO information.

Updated LFRCO information.

Updated HFRCO information.

Updated ULFRCO information.

Updated ADC information.

Updated DAC information.

Updated OPAMP information.

Updated ACMP information.

Updated VCMP information.

Added AUXHFRCO information.

7.3 Revision 1.21

November 21st, 2013

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

Re-added missing DAC-data.

7.4 Revision 1.20

September 30th, 2013

Added I2C characterization data.

Added SPI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

Updated that the EM2 current consumption test was carried out with only one RAM block enabled.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.5 Revision 1.10

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.98

May 25th, 2012

Corrected EM3 current consumption in the Electrical Characteristics section.

7.8 Revision 0.96

February 28th, 2012

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.9 Revision 0.95

September 28th, 2011

Flash configuration for Giant Gecko is now 1024KB or 512KB. For flash sizes below 512KB, see the Leopard Gecko Family.

Corrected operating voltage from 1.8 V to 1.85 V.

Added rising POR level to Electrical Characteristics section.

Updated Minimum Load Capacitance (C_{LFXOL}) Requirement For Safe Crystal Startup.

Added Gain error drift and Offset error drift to ADC table.

Added Opamp pinout overview.

Added reference to errata document.

Corrected TQFP64 package drawing.

Updated PCB land pattern, solder mask and stencil design.

7.10 Revision 0.90

June 29th, 2011

Initial preliminary release.

A Disclaimer and Trademarks

A.1 Disclaimer

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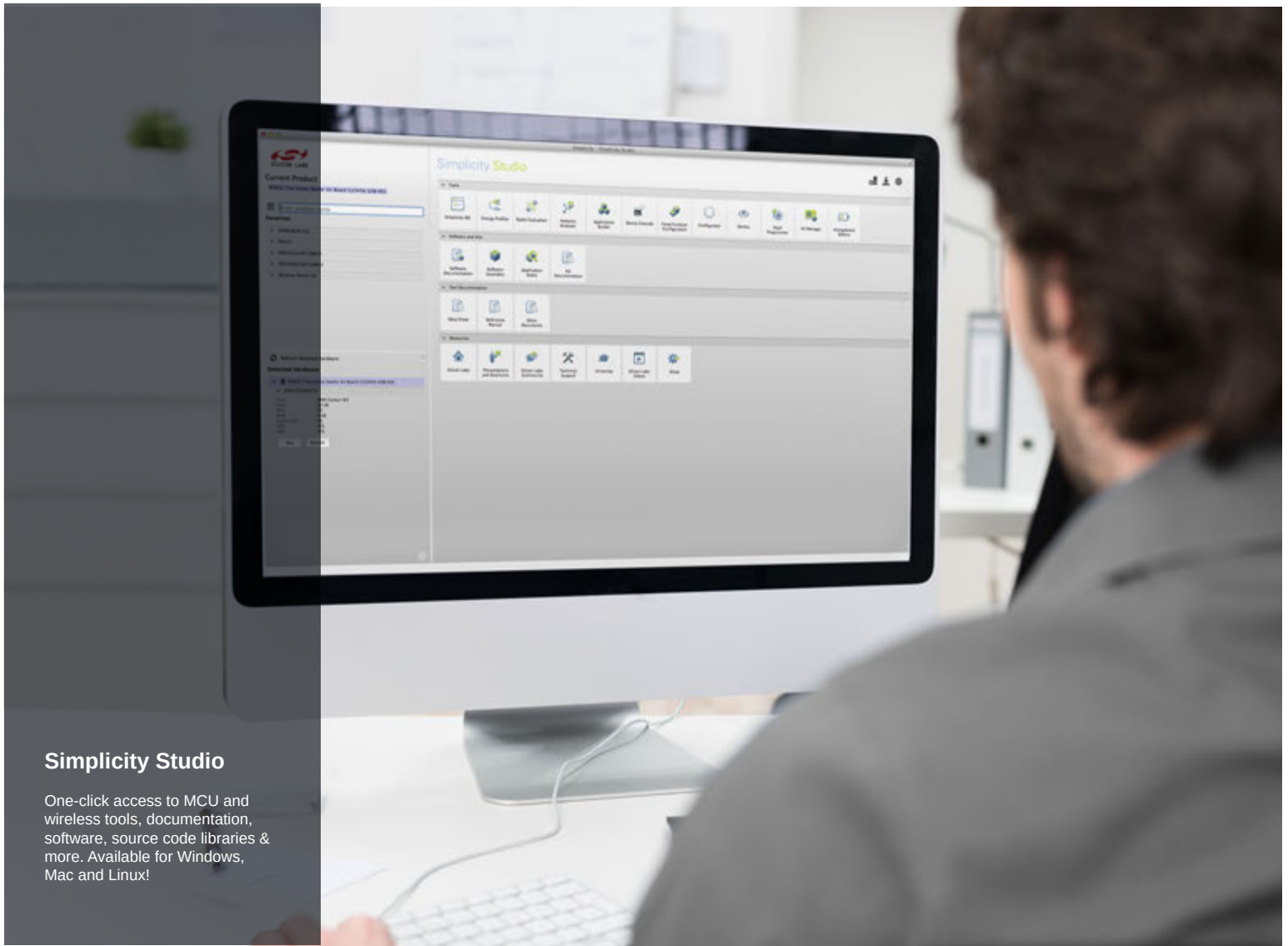
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