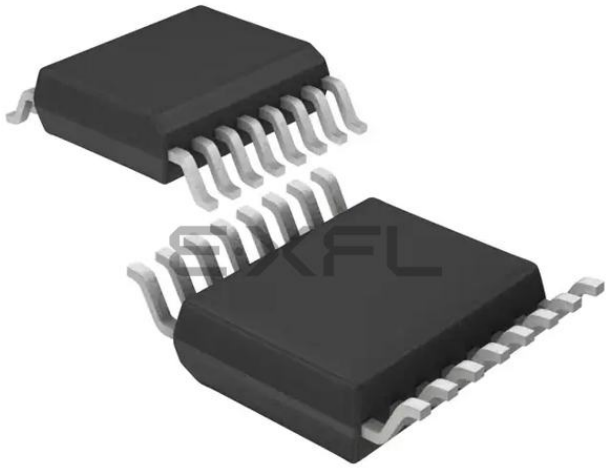


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	LINbus, SCI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08sc4e0ctg

Table of Contents

Chapter 2
Pins and Connections

This section describes signals that connect to package pins. It includes pinout diagrams, recommended system connections, and detailed discussions of signals.

2.1 Device Pin Assignment

The following figure shows the pin assignments for the MC9S08SC4 device.

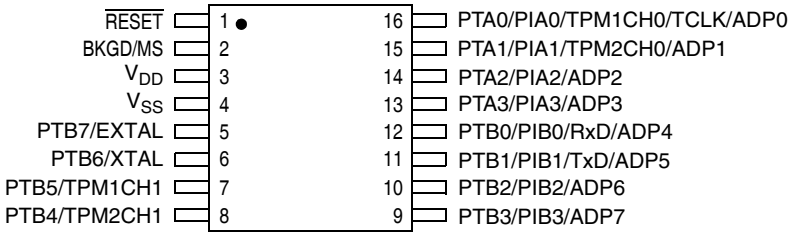


Table 2-1. Pin Function Priority

Pin Number	Priority ← Lowest … Highest →				
16-pin	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1					$\overline{\text{RESET}}$
2				BKGD	MS
3					V_{DD}
4					V_{SS}
5	PTB7		EXTAL		
6	PTB6		XTAL		
7	PTB5	TPM1CH1			
8	PTB4	TPM2CH1			
9	PTB3	PIB3			ADP7
10	PTB2	PIB2			ADP6
11	PTB1	PIB1	TxD		ADP5

Table 2-1. Pin Function Priority (continued)

Pin Number	Priority ← Lowest … Highest →				
16-pin	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
12	PTB0	PIB0	RxD		ADP4
13	PTA3	PIA3			ADP3
14	PTA2	PIA2			ADP2
15	PTA1	PIA1	TPM2CH0		ADP1
16	PTA0	PIA0	TPM1CH0	TCLK	ADP0

Chapter 3
Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MC9S08SC4 Series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3-1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 3-2 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 3-2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +5.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 3-3. Thermal Characteristics

Num	C	Rating	Symbol	Value	Unit
1	—	Operating temperature range (packaged)	T_A	T_L to T_H	°C
		C		–40 to 85	
		V		–40 to 105	
		M		–40 to 125	
2	D	Maximum junction temperature	T_{JM}	—	°C
		C		95	
		V		115	
		M		135	
3	D	Thermal resistance [1,2] Single-layer board 16-pin TSSOP	θ_{JA}	130	°C/W
4	D	Thermal resistance[1,2] Four-layer board 16-pin TSSOP	θ_{JA}	87	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 3-1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 3-2}$$

Solving Equation 3-1 and Equation 3-2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3-3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 3-1 and Equation 3-2 iteratively for any value of T_A

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3-4. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 3-6. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
15	D	DC injection current [4, 5, 6, 7] Single pin limit	I_{IC}	$V_{IN} > V_{DD}$	0	—	2	mA
				$V_{IN} < V_{SS}$,	0	—	–0.2	mA
		Total MCU limit, includes sum of all stressed pins		$V_{IN} > V_{DD}$	0	—	25	mA
				$V_{IN} < V_{SS}$,	0	—	–5	mA
16	D	Input Capacitance, all pins	C_{In}	—	—	—	8	pF
17	D	RAM retention voltage	V_{RAM}	—	—	0.6	1.0	V
18	D	POR re-arm voltage[8]	V_{POR}	—	0.9	1.4	2.0	V
19	D	POR re-arm time[9]	t_{POR}	—	10	—	—	µs
20	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	—	 3.85 3.95	 4.0 4.1	 4.15 4.25	V
21	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	—	 4.45 4.55	 4.6 4.7	 4.75 4.85	V
22	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	—	 4.15 4.25	 4.3 4.4	 4.45 4.55	V
23	T	Low-voltage inhibit reset/recover hysteresis	V_{hys}	—	—	100	—	mV
24	P	Bandgap Voltage Reference[10]	V_{BG}	—	1.17	1.20	1.22	V

1 Typical values are measured at 25°C. Characterized, not tested.

2 When a pin interrupt is configured to detect rising edges, pull-down resistors are used in place of pull-up resistors.

3 The specified resistor value is the actual value internal to the device. The pull-up value may measure higher when measured externally on the pin.

4 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

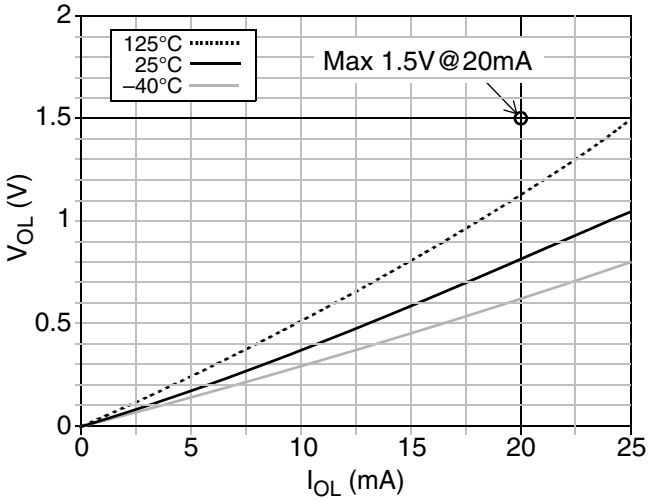
6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

8 Maximum is highest voltage that POR will occur.

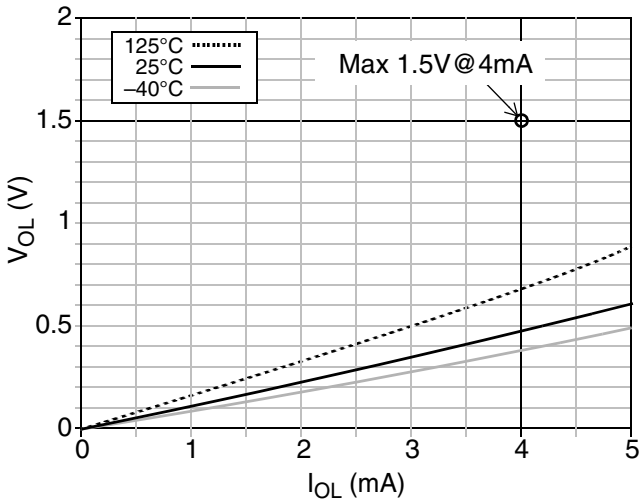
9 Simulated, not tested

10 Factory trimmed at V_{DD} = 5.0 V, Temp = 25°C



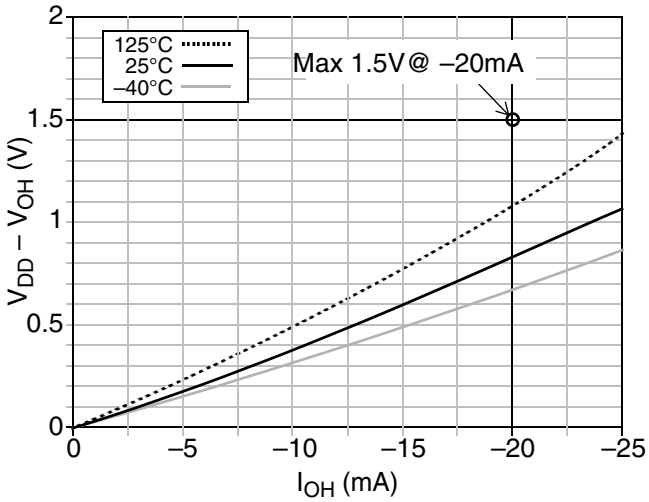
a) V_{DD} = 5V, High Drive

Figure 3-1. Typical V_{OL} vs I_{OL}, High Drive Strength



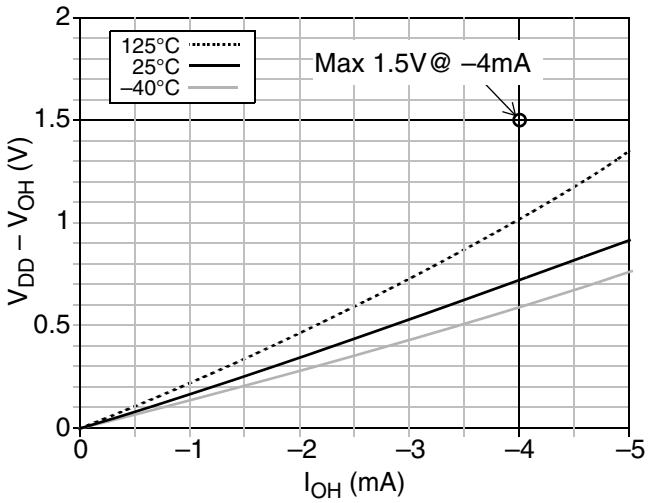
a) V_{DD} = 5V, Low Drive

Figure 3-2. Typical V_{OL} vs I_{OL}, Low Drive Strength



a) V_{DD} = 5V, High Drive

Figure 3-3. Typical $V_{DD} – V_{OH}$ vs I_{OH}, High Drive Strength



a) V_{DD} = 5V, Low Drive

Figure 3-4. Typical $V_{DD} – V_{OH}$ vs I_{OH}, Low Drive Strength

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

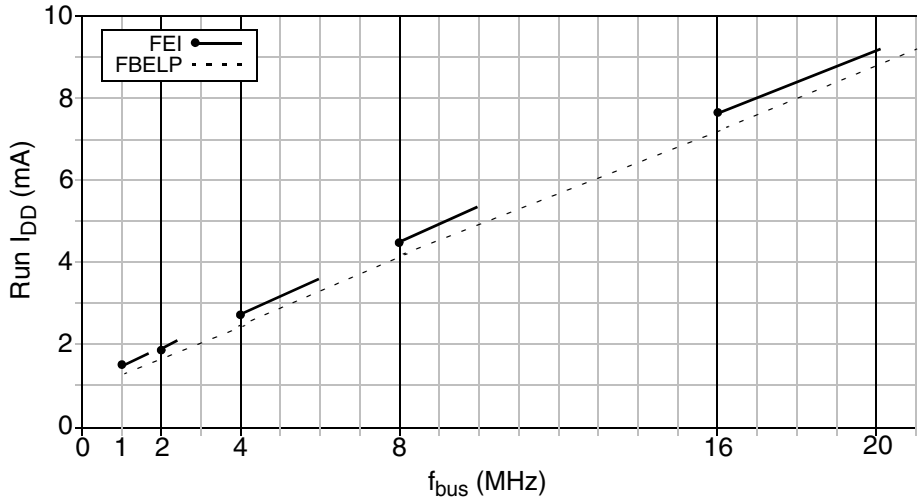
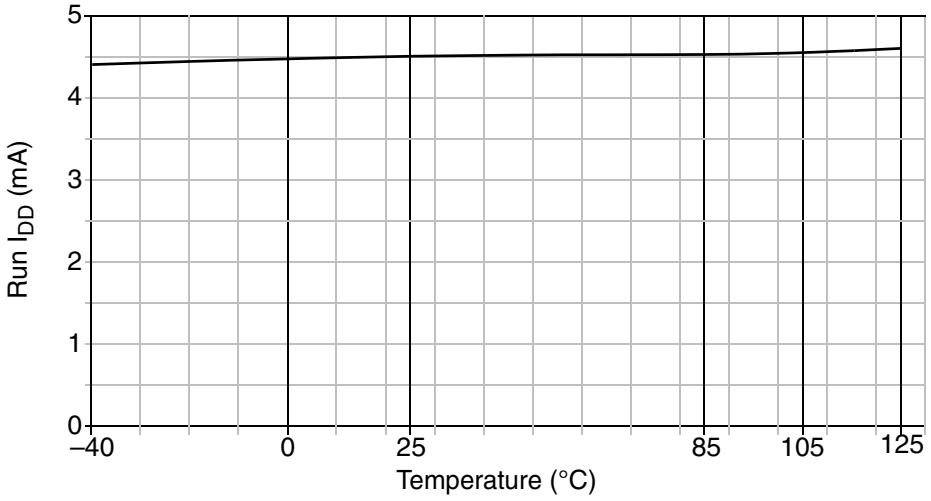


Figure 3-5. Typical Run I_{DD} vs. Bus Frequency (V_{DD} = 5V)



Note: ICS is configured to FEI.

Figure 3-6. Typical Run I_{DD} vs. Temperature (V_{DD} = 5V; f_{bus} = 8MHz)

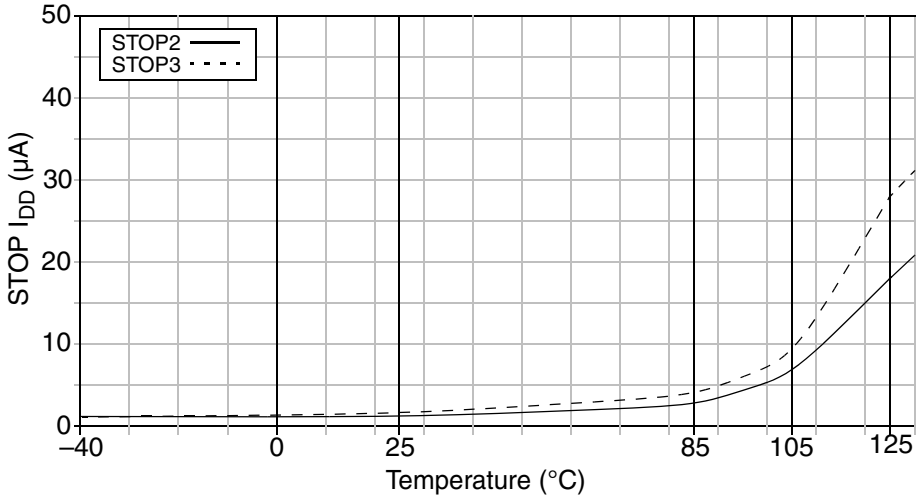
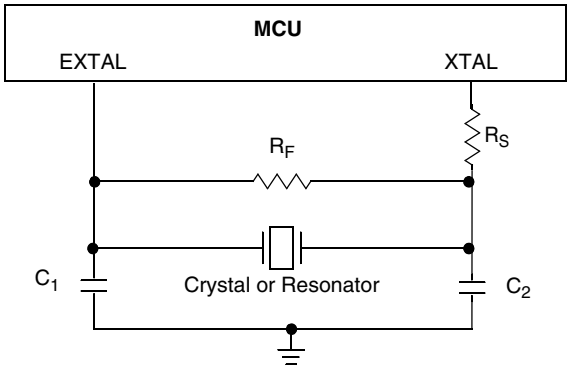


Figure 3-7. Typical Stop I_{DD} vs. Temperature (V_{DD} = 5V)

3.8 External Oscillator (XOSC) Characteristics

NOTE

The MC9S08SC4 series supports a narrower low frequency external reference range than the standard ICS specification. All references to range "31.25 kHz to 39.0625 kHz" in this section should be limited to " 32.0 kHz to 38.4 kHz".



3.9 Internal Clock Source (ICS) Characteristics

Table 3-9. ICS Frequency Specifications (Temperature Range = –40 to 125°C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25°C	f_{int_ft}	—	31.25	—	kHz
2	T	Internal reference frequency - untrimmed[1]	f_{int_ut}	25	36	41.66	kHz
3	P	Internal reference frequency - user trimmed	f_{int_t}	31.25	—	39.0625	kHz
4	T	Internal reference startup time	t_{irefst}	—	—	6	µs
5	—	DCO output frequency range - untrimmed[1] value provided for reference assumes: fdco_ut = 1024 x f_{int_ut}	f_{dco_ut}	25.6	36.86	42.66	MHz
6	D	DCO output frequency range - trimmed	f_{dco_t}	32	—	40	MHz
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$
8	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
9	D	Total deviation from actual trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 – 1.0	± 2.0	$\%f_{dco}$
10	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
11	D	FLL acquisition time [2]	$t_{acquire}$	—	—	1	ms
12	D	DCO output clock long term jitter (over 2mS interval) [3]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3.10 ADC Characteristics

Table 3-10. ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}[2]	2.7	—	5.5	V	—
Input Voltage	—	V_{ADIN}	V_{REFL}[2]	—	V_{REFH}[2]	V	—
Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
Input Resistance	—	R_{ADIN}	—	3	5	kΩ	—
Analog Source Resistance	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 5 10	kΩ	External to MCU
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Frequency	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume VDDA = 5.0 V, Temp = 25°C, fADCK=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 V_{DDA}/V_{REFH} and V_{SSA}/V_{REFL}, are derived from V_{DD} and V_{SS} respectively.

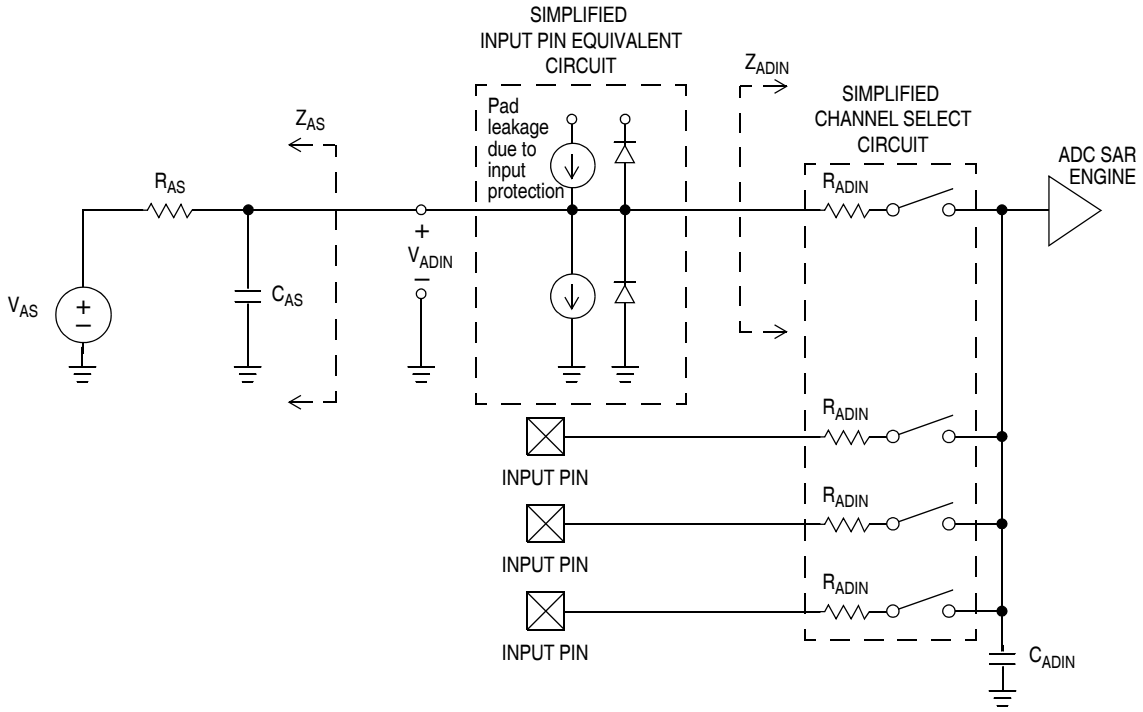


Figure 3-8. ADC Input Impedance Equivalency Diagram

Table 3-11. ADC Characteristics

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1	—	T	I_{DDA}	—	133	—	μA	—
Supply Current ADLPC=1 ADLSMP=0 ADCO=1	—	T	I_{DDA}	—	218	—	μA	—
Supply Current ADLPC=0 ADLSMP=1 ADCO=1	—	T	I_{DDA}	—	327	—	μA	—
Supply Current ADLPC=0 ADLSMP=0 ADCO=1	—	T	I_{DDA}	—	0.582	1	mA	—
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)			1.25	2	3.3		
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles	See ADC chapter in MC9S08SC4 Reference Manual for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	10 bit mode	P	E_{TUE}	—	±1.5	±3.5	LSB	Includes quantization
	8 bit mode			—	±0.7	±1.5		
Differential Non-Linearity	10 bit mode	P	DNL	—	±0.5	±1.0	LSB	
	8 bit mode			—	±0.3	±0.5		
	Monotonicity and No-Missing-Codes guaranteed							
Integral Non-Linearity	10 bit mode	C	INL	—	±0.5	±1.0	LSB	
	8 bit mode			—	±0.3	±0.5		
Zero-Scale Error	10 bit mode	P	E_{ZS}	—	±1.5	±2.5	LSB	$V_{ADIN} = V_{SSA}$
	8 bit mode			—	±0.5	±0.7		
Full-Scale Error	10 bit mode	P	E_{FS}	—	±1	±1.5	LSB	$V_{ADIN} = V_{DDA}$
	8 bit mode			—	±0.5	±0.5		

Table 3-11. ADC Characteristics

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Quantization Error	10 bit mode	D	E_Q	—	—	±0.5	LSB	—
	8 bit mode			—	—	±0.5		
Input Leakage Error	10 bit mode	D	E_{IL}	—	±0.2	±2.5	LSB	Pad leakage[2] * R_{AS}
	8 bit mode			—	±0.1	±1		
Temp Sensor Slope	–40°C– 25°C	D	m	—	3.266	—	mV/°C	—
	25°C– 125°C			—	3.638	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	—

1 Typical values assume V_{DDA} = 5.0V, Temp = 25C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 Based on input pad leakage current. Refer to pad electricals.

3.11 AC Characteristics

This section describes AC timing characteristics for each peripheral system.

3.11.1 Control Timing

Table 3-12. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
2	P	Internal low power oscillator period	t_{LPO}	700	975	1500	μs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive[3]	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	Pin interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
6	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 40 75	 — —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF)[6] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	 — —	 11 35	 — —	ns

1 Typical values are based on characterization data at V_{DD} = 5.0V, 25°C unless otherwise stated.

Chapter 4
Ordering Information and Mechanical Drawings

4.1 Ordering Information

This section contains ordering information for MC9S08SC4 device.

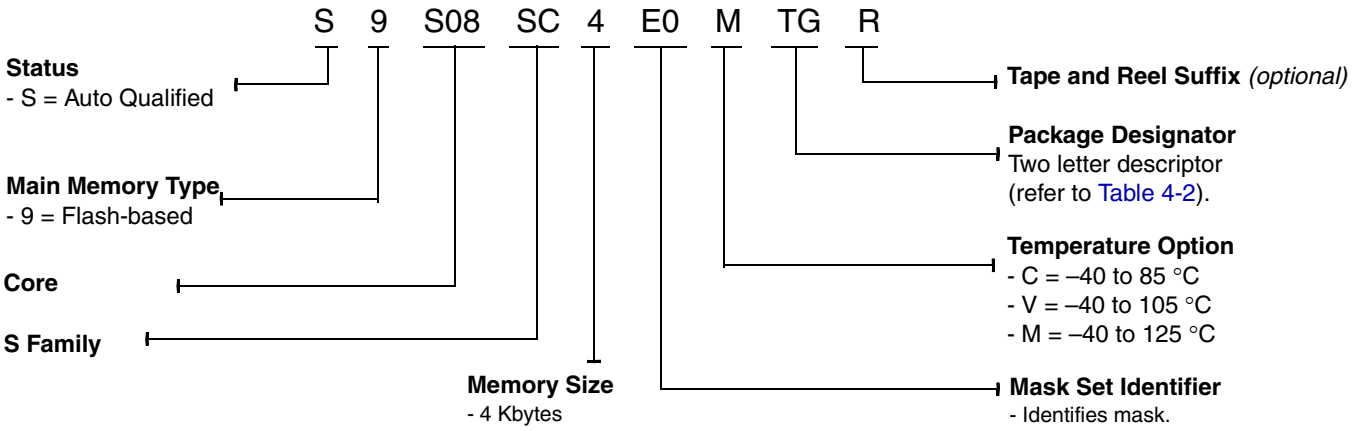
Table 4-1. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	FLASH	RAM	
S9S08SC4E0MTG	4K	256	16 TSSOP

1 See MC9S08SC4 Reference Manual for a complete description of modules. included on each device.

2 See Table 4-2 for package information.

4.1.1 Device Numbering Scheme



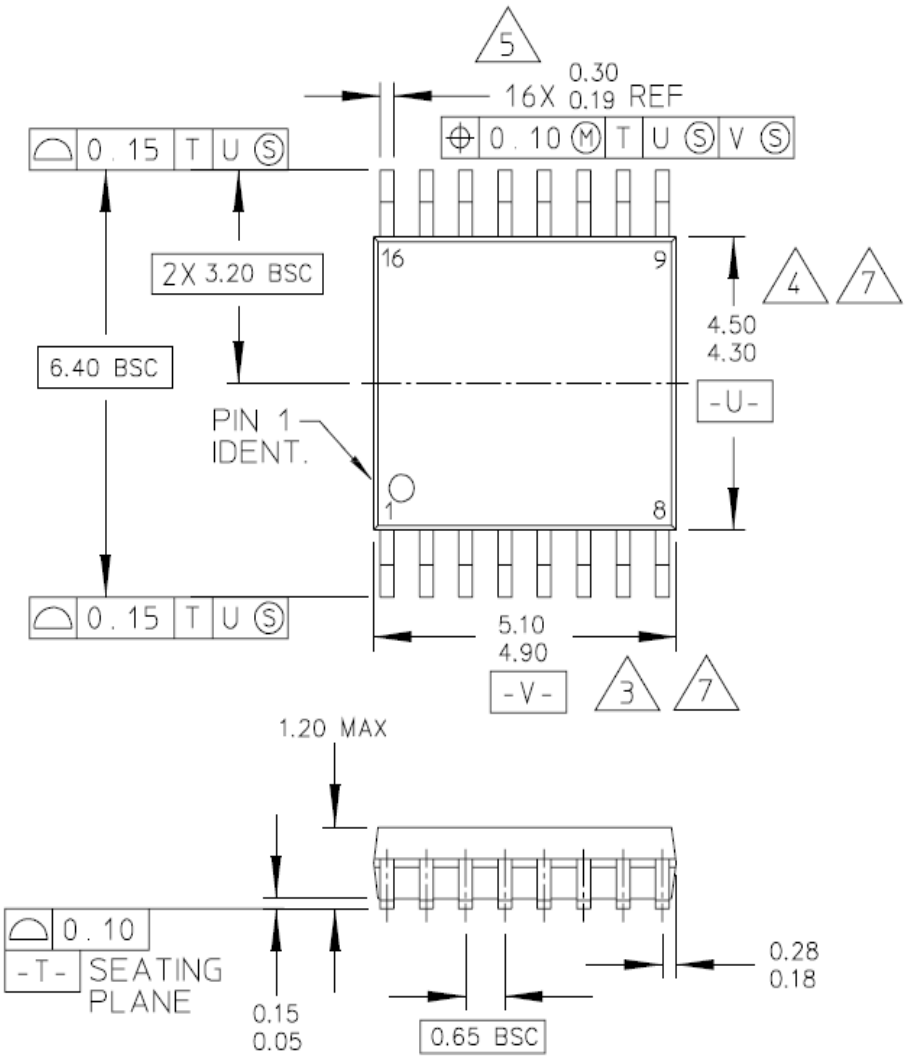
4.2 Package Information

Table 4-2. Package Information

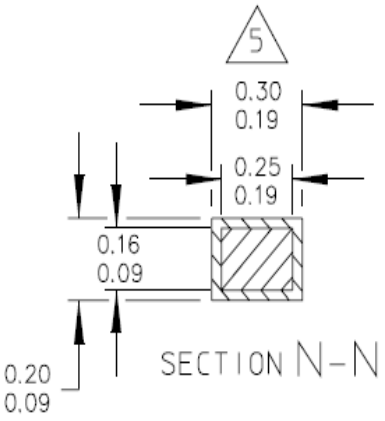
Pin Count	Type	Designator	Case Number	Document No.
16	TSSOP	TG	948F-01	98ASH70247A

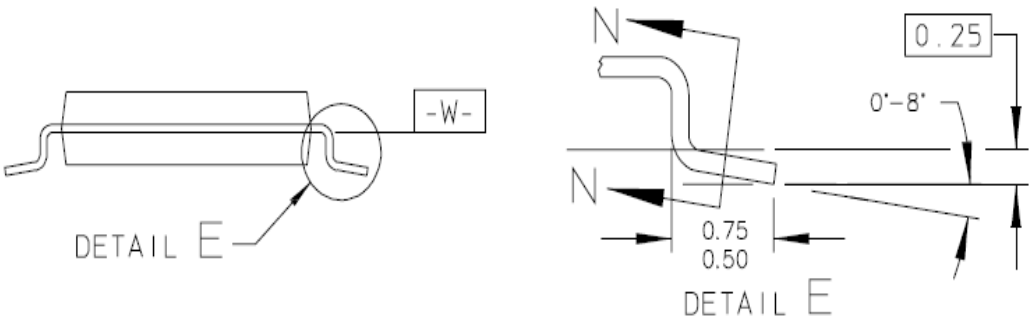
4.3 Mechanical Drawings

The following pages are mechanical drawings for the package described in Table 4-2.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	





© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 16 LD TSSOP, PITCH 0.65MM	DOCUMENT NO: 98ASH70247A	REV: B
	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

MC9S08SC4
Rev.4
6/2010