

Welcome to [E-XFL.COM](https://www.e-xfl.com)

#### Understanding Embedded - PLDs (Programmable Logic Devices)

Embedded - PLDs, or Programmable Logic Devices, are a type of digital electronic component used to build reconfigurable digital circuits. Unlike fixed-function logic devices, PLDs can be programmed to perform specific functions by the user. This flexibility allows designers to customize the logic to meet the exact needs of their applications, making PLDs a crucial component in modern embedded systems.

#### Applications of Embedded - PLDs (Programmable Logic Devices)

The versatility of PLDs makes them suitable for a wide range of applications. In consumer electronics, PLDs are used to enhance the functionality and performance of

#### Details

Product Status	Active
Programmable Type	EPLD
Number of Macrocells	10
Voltage - Input	5V
Speed	15 ns
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.51x11.51)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atv750bl-15lm-883">https://www.e-xfl.com/product-detail/microchip-technology/atv750bl-15lm-883</a>

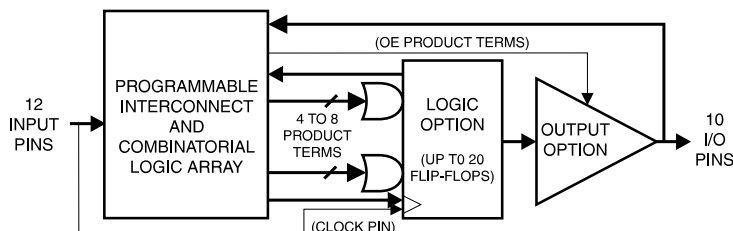
## Features

- **Advanced, High-speed Programmable Logic Device – Superset of 22V10**
  - Improved Performance - 7.5 ns  $t_{PD}$ , 95 MHz External Operation
  - Enhanced Logic Flexibility
  - Backward Compatible with ATV750(L) Software and Hardware
- **New Flip-flop Features**
  - D- or T-type
  - Product Term or Direct Input Pin Clocking
- **High-speed Erasable Programmable Logic Devices**
  - 7.5 ns Maximum Pin-to-pin Delay

Device	$I_{CC}$ , Standby
ATV750B	125 mA
ATV750BL	15 mA

- **Highest Density Programmable Logic Available in a 24-pin Package**
- **Increased Logic Flexibility**
  - 42 Array Inputs, 20 Sum Terms and 20 Flip-flops
- **Enhanced Output Logic Flexibility**
  - All 20 Flip-flops Feed Back Internally
  - 10 Flip-flops are Also Available as Outputs
- **Full Military, Commercial and Industrial Temperature Ranges**

## Logic Diagram

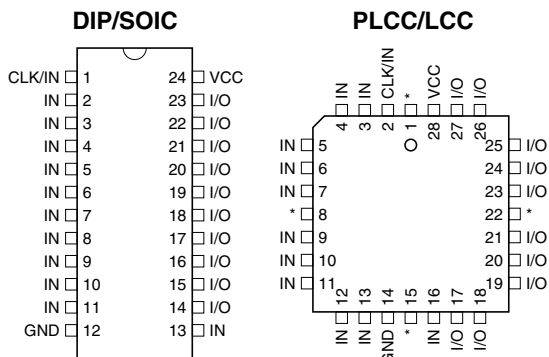


## Description

The ATV750B(L) is twice as powerful as most other 24-pin programmable logic devices. Increased product terms, sum terms, flip-flops and output logic configurations translate into more usable gates. High-speed logic and uniform, predictable delays guarantee fast in-system performance.

## Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
*	No Internal Connection
$V_{CC}$	+5V Supply



## High-speed UV Erasable Programmable Logic Device

### ATV750B ATV750BL

Commercial and industrial versions are obsolete. Please use ATF750C.

Military versions continue to be available, but please do not use for new designs. For new military applications, recommend multiple ATF22V10s.



Each of the ATV750B(L) 22 logic pins can be used as an input. Ten of these can be used as inputs, outputs or bi-directional I/O pins. Each flip-flop is individually configurable as either D- or T-type. Each flip-flop output is fed back into the array independently. This allows burying of all the sum terms and flip-flops.

There are 171 total product terms available. A variable format is used to assign between four to eight product terms per sum term. There are two sum terms per output, providing added flexibility. Much more logic can be replaced by this device than by any other 24-pin PLD. With 20 sum terms and flip-flops, complex state machines are easily implemented with logic to spare.

Product terms provide individual clocks and asynchronous resets for each flip-flop. Each flip-flop may also be individually configured to have direct input pin controlled clocking. Each output has its own enable product term. One product term provides a common synchronous preset for all flip-flops. Register preload functions are provided to simplify testing. All registers automatically reset upon power-up.

The ATV750BL is a low-power device with speeds as fast as 15 ns. The ATV750BL provides the optimum low-power PLD solution, with full CMOS output levels. This device significantly reduces total system power, thereby allowing battery-powered operation.

## Absolute Maximum Ratings\*

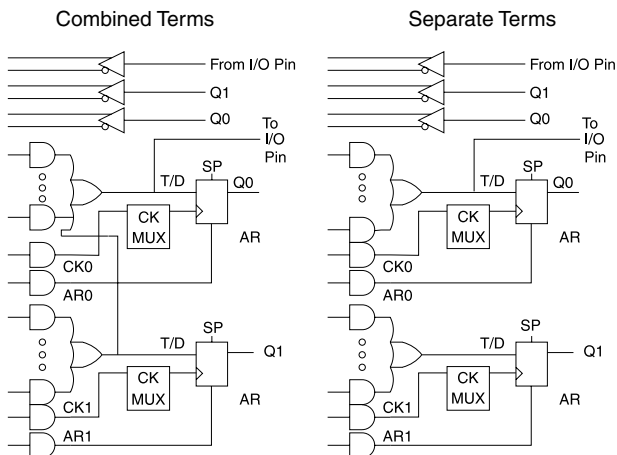
Temperature Under Bias.....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
Integrated UV Erase Dose.....	7258 W·sec/cm <sup>2</sup>

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

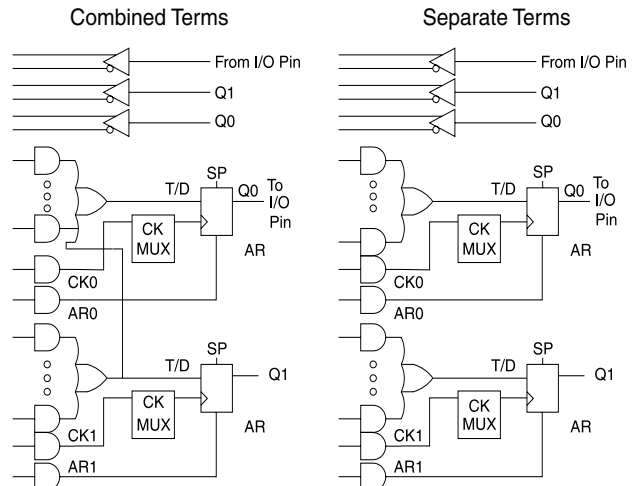
**Note:** 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC which may overshoot to +7.0V for pulses of less than 20 ns.

## Logic Options

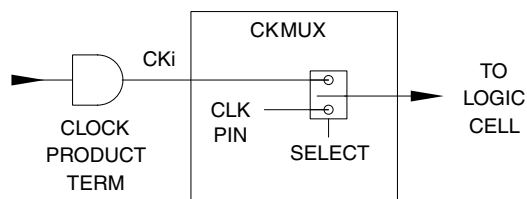
### Combinatorial Output



### Registered Output



## Clock Mux



## Output Options



## DC and AC Operating Conditions<sup>(1)</sup>

	Commercial -7, -10, -15	Commercial -25	Industrial	Military
Operating Temperature	0°C - 70°C (Ambient)	0°C - 70°C (Ambient)	-40°C - 85°C (Ambient)	-55°C - 125°C (Case)
V <sub>CC</sub> Power Supply	5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

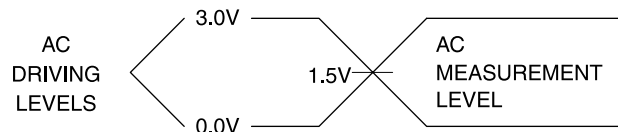
Note: 1. See ordering information for valid speed and temperature combination.

## DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = -0.1V to V <sub>CC</sub> + 1V					10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = -0.1V to V <sub>CC</sub> + 0.1V					10	μA
I <sub>CC</sub>	Power Supply Current, Standby	V <sub>CC</sub> = MAX, V <sub>IN</sub> = MAX, Outputs Open	B-7, -10	Com.		125	180	mA
				Ind., Mil.		125	190	mA
			B-15, -25	Com.		125	180	mA
				Ind., Mil.		125	190	mA
			BL-15	Com.		15	30	mA
				Ind., Mil.		15	30	mA
I <sub>OS</sub> <sup>(1)</sup>	Output Short Circuit Current	V <sub>OUT</sub> = 0.5V					-120	mA
V <sub>IL</sub>	Input Low Voltage	4.5 ≤ V <sub>CC</sub> ≤ 5.5V			-0.6		0.8	V
V <sub>IH</sub>	Input High Voltage				2.0		V <sub>CC</sub> + 0.75	V
V <sub>OL</sub>	Output Low Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = MIN	I <sub>OL</sub> = 16 mA	Com., Ind.			0.5	V
			I <sub>OL</sub> = 12 mA	Mil.			0.5	V
			I <sub>OL</sub> = 24 mA	Com.			0.8	V
V <sub>OH</sub>	Output High Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>CC</sub> = MIN	I <sub>OH</sub> = -100 μA		V <sub>CC</sub> - 0.3			V
			I <sub>OH</sub> = -4.0 mA		2.4			V

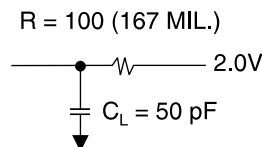
Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

## Input Test Waveforms and Measurement Levels

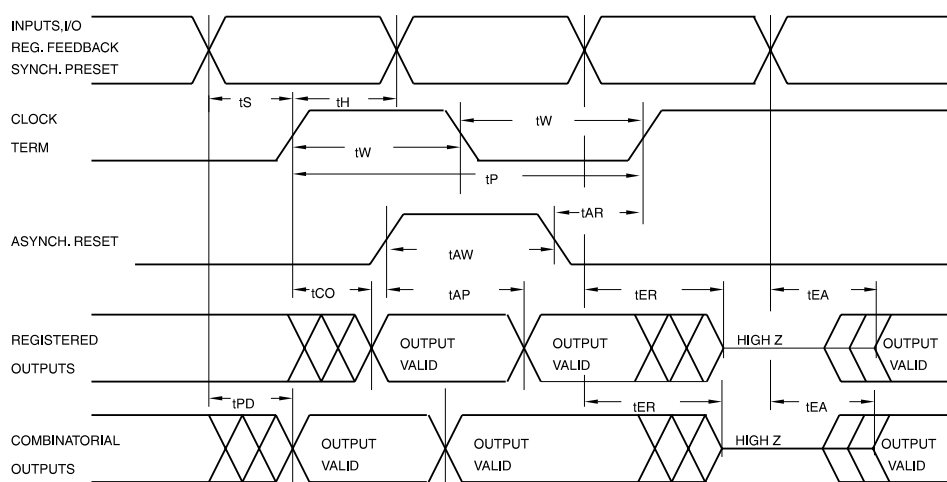


$$t_R, t_F < 3\text{ ns (10\% to 90\%)}$$

## Output Test Load



## AC Waveforms, Product Term Clock<sup>(1)</sup>



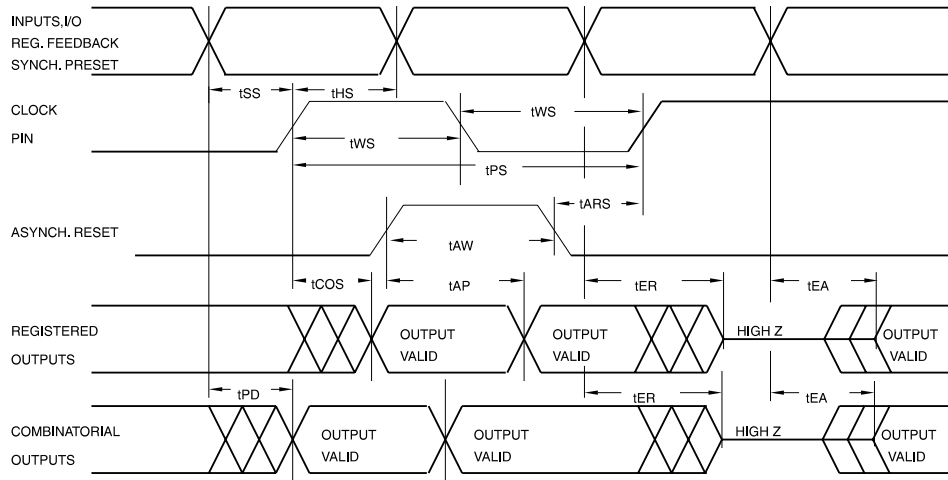
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

## AC Characteristics, Product Term Clock<sup>(1)</sup>

Symbol	Parameter	-7		-10		B/BL-15		B/BL-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD}$	Input or Feedback to Non-Registered Output		7.5		10		15		25	ns
$t_{EA}$	Input to Output Enable		7.5		10		15		25	ns
$t_{ER}$	Input to Output Disable		7.5		10		15		25	ns
$t_{CO}$	Clock to Output	3	7.5	4	10	5	12	6	20	ns
$t_{CF}$	Clock to Feedback	1	5	4	7.5	5	9	5	10	ns
$t_S$	Input Setup Time	3		4		8/12		14		ns
$t_{SF}$	Feedback Setup Time	3		4		7		7		ns
$t_H$	Hold Time	1		2		5/7		5/7		ns
$t_P$	Clock Period	7		11		14		17		ns
$t_W$	Clock Width	3.5		5.5		7		8.5		ns
$f_{MAX}$	External Feedback $1/(t_S+t_{CO})$		95		71		50/41		29	MHz
	Internal Feedback $1/(t_{SF}+t_{CF})$		125		86		62		58	MHz
	No Feedback $1/(t_P)$		142		90		71		58	MHz
$t_{AW}$	Asynchronous Reset Width	5		10		15		20		ns
$t_{AR}$	Asynchronous Reset Recovery Time	3		10		15		20		ns
$t_{AP}$	Asynchronous Reset to Registered Output Reset		8		12		15		25	ns
$t_{SP}$	Setup Time, Synchronous Preset	4		7		8		15		ns

Note: 1. See ordering information for valid part numbers.

## AC Waveforms, Input Pin Clock<sup>(1)</sup>

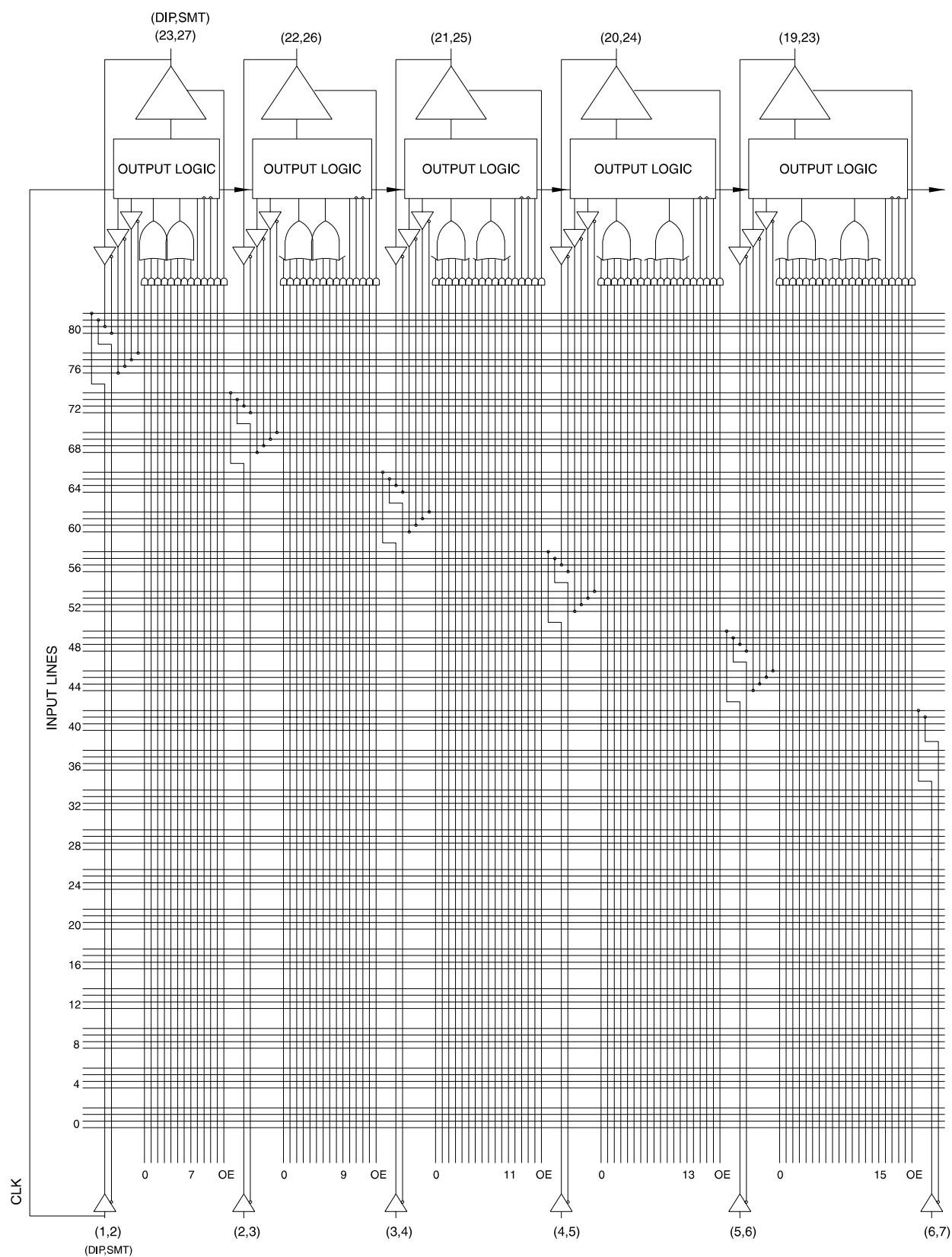


Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

## AC Characteristics, Input Pin Clock

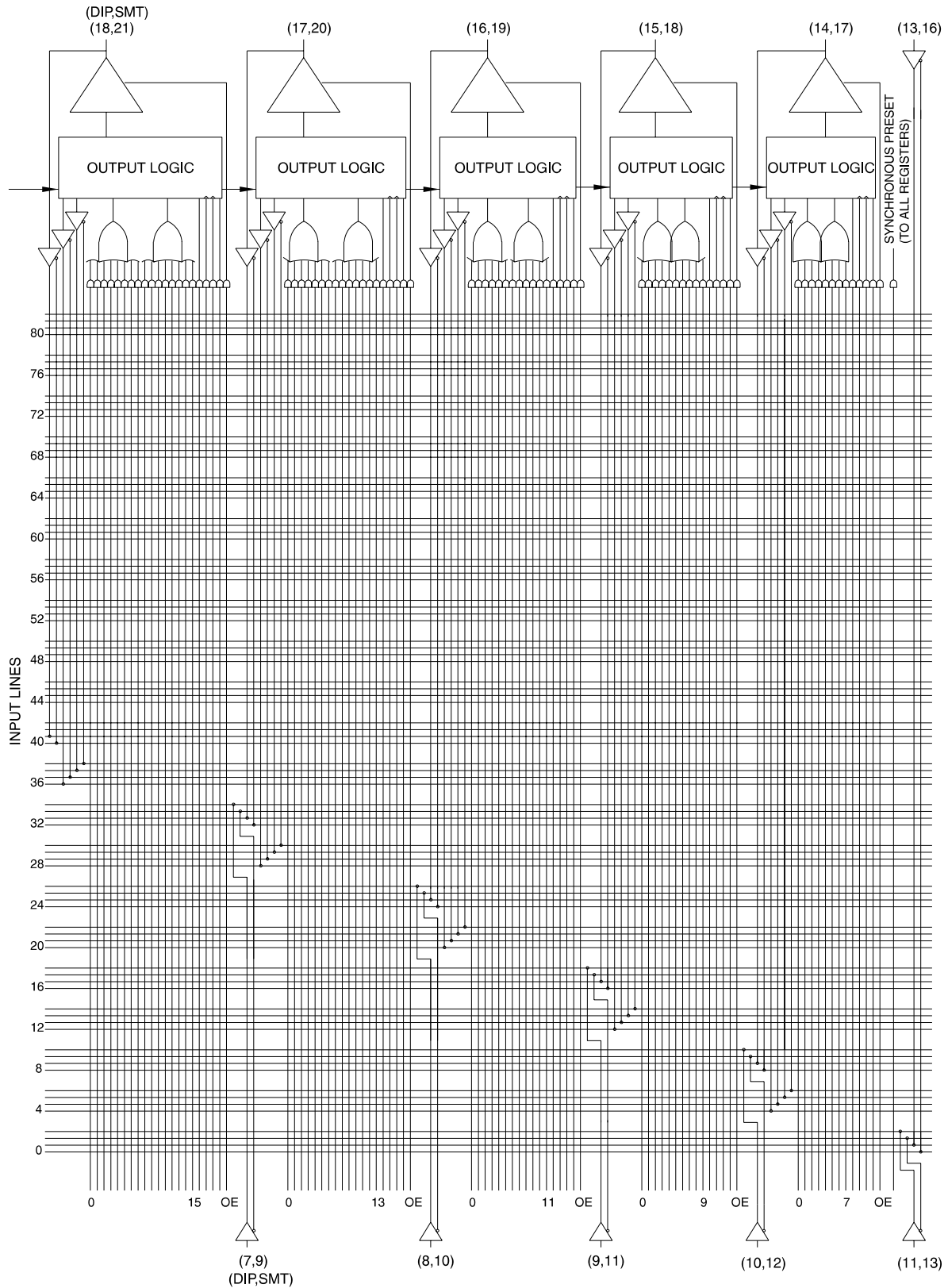
Symbol	Parameter	-7		-10		B/BL -15		B/BL -25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD}$	Input or Feedback to Non-Registered Output		7.5		10		15		25	ns
$t_{EA}$	Input to Output Enable		7.5		10		15		25	ns
$t_{ER}$	Input to Output Disable		7.5		10		15		25	ns
$t_{COS}$	Clock to Output	0	6.5	0	7	0	10	0	12	ns
$t_{CFS}$	Clock to Feedback	0	3.5	0	5	0	5.5	0	7	ns
$t_{SS}$	Input Setup Time	4		6.5		8/12.5		9/15		ns
$t_{SFS}$	Feedback Setup Time	4		5		7		9		ns
$t_{HS}$	Hold Time	0		0		0		0		ns
$t_{PS}$	Clock Period	7		10		12		16		ns
$t_{WS}$	Clock Width	3.5		5		6		8		ns
$f_{MAXS}$	External Feedback $1/(t_{SS}+t_{COS})$		95		74		55/44		48/37	MHz
	Internal Feedback $1/(t_{SFS}+t_{CFS})$		133		100		80		62	MHz
	No Feedback $1/(t_{PS})$		142		100		83		62	MHz
$t_{AW}$	Asynchronous Reset Width	5		10		15		20		ns
$t_{ARS}$	Asynchronous Reset Recovery Time	5		10		15		25		ns
$t_{AP}$	Asynchronous Reset to Registered Output Reset		8		10		15		25	ns
$t_{SPS}$	Setup Time, Synchronous Preset	5		5/9		11		15		ns

# Functional Logic Diagram ATV750B, Upper Half



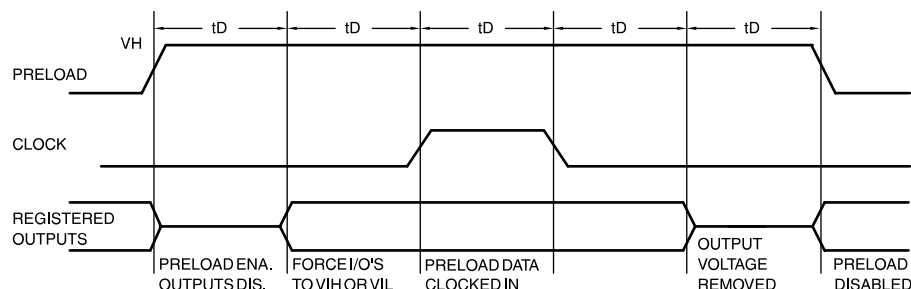


## Functional Logic Diagram ATV750B, Lower Half



## Preload of Registered Outputs

The ATV750B(L) registers are provided with circuitry to allow loading of each register asynchronously with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A  $V_{IH}$  level on the I/O pin will force the register high; a  $V_{IL}$  will force it low, independent of the output polarity. The PRELOAD state is entered by placing a 10.25V to 10.75V signal on pin 8 on DIPs, and lead 10 on SMDs. When the clock term is pulsed high, the data on the I/O pins is placed into the register chosen by the Select Pin.



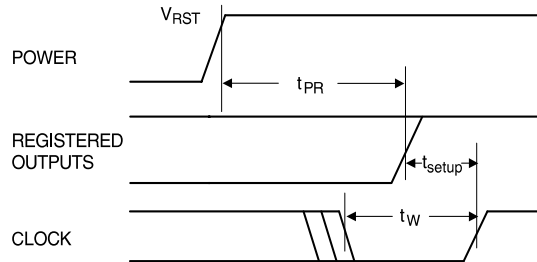
Level Forced on Registered Output Pin during PRELOAD Cycle	Select Pin State	Register #0 State after Cycle	Register #1 State after Cycle
$V_{IH}$	Low	High	X
$V_{IL}$	Low	Low	X
$V_{IH}$	High	X	High
$V_{IL}$	High	X	Low

## Power-up Reset

The registers in the ATV750B(L) is designed to reset during power-up. At a point delayed slightly from  $V_{CC}$  crossing  $V_{RST}$ , all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how  $V_{CC}$  actually rises in the system, the following conditions are required:

1. The  $V_{CC}$  rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock terms or pin high, and
3. The clock pin, or signals from which clock terms are derived, must remain stable during  $t_{PR}$ .



Parameter	Description	Typ	Max	Units
$t_{PR}$	Power-up Reset Time	600	1000	ns
$V_{RST}$	Power-up Reset Voltage	3.8	4.5	V

## Pin Capacitance

$f = 1 \text{ MHz}$ ,  $T = 25^\circ\text{C}^{(1)}$

	Typ	Max	Units	Conditions
$C_{IN}$	5	8	pF	$V_{IN} = 0V$
$C_{OUT}$	6	8	pF	$V_{OUT} = 0V$

## Using the ATV750B(L) Many Advanced Features

The ATV750B(L) advanced flexibility packs more usable gates into 24-pins than any other logic device. The ATV750B(L) starts with the popular 22V10 architecture, and add several enhanced features:

- **Selectable D- and T-type Registers** – Each ATV750B flip-flop can be individually configured as either D- or T-type. Using the T-type configuration, JK and SR flip-flops are also easily created. These options allow more efficient product term usage.
- **Selectable Asynchronous Clocks** – Each of the ATV750B(L) flip-flops may be clocked by its own clock product term or directly from Pin 1 (SMD Lead 2). This removes the constraint that all registers must use the same clock. Buried state machines, counters and registers can all coexist in one device while running on separate clocks. Individual flip-flop clock source selection further allows mixing higher performance pin clocking and flexible product term clocking within one design.
- **A Full Bank of Ten More Registers** – The ATV750B provides two flip-flops per output logic cell for a total of 20. Each register has its own sum term, its own reset term and its own clock term.
- **Independent I/O Pin and Feedback Paths** – Each I/O pin on the ATV750B has a dedicated input path. Each of the 20 registers has its own feedback terms into the array as well. This feature, combined with individual product terms for each I/O's output enable, facilitates true bi-directional I/O design.

## Programming Software Support

As with all other Atmel PLDs, several third-party development software products support the ATV750B(L). Several third-party programmers support the ATV750B as well. Additionally, the ATV750B may be programmed to perform the ATV750(L)'s functional subset (no T-type flip-flops or pin clocking) using the ATV750(L) JEDEC file. In this case, the ATV750B becomes a direct replacement or speed upgrade for the ATV750(L). The ATV750(L) programming algorithm is different from the ATV750B algorithm. Choose the appropriate device in your programmer menu to ensure proper programming. Please refer to the *Programmable Logic Development Tools* section for a complete PLD software and programmer listing.

## Synchronous Preset and Asynchronous Reset

One synchronous preset line is provided for all 20 registers in the ATV750B. The appropriate input signals to cause the internal clocks to go to a high state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the switching waveform diagram.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both master and slave halves of the flip-flops are reset when the input signals received force the internal resets high.

## Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATV750B fuse patterns. Once the security fuse is programmed, all fuses will appear programmed during verify.

The security fuse should be programmed last, as its effect is immediate.

## **Erase Characteristics**

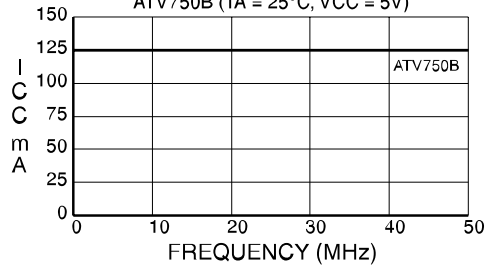
The entire memory array of an ATV750B is erased after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000  $\mu\text{W}/\text{cm}^2$  intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15  $\text{W}\cdot\text{sec}/\text{cm}^2$ . To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV-erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

## **Atmel CMOS PLDs**

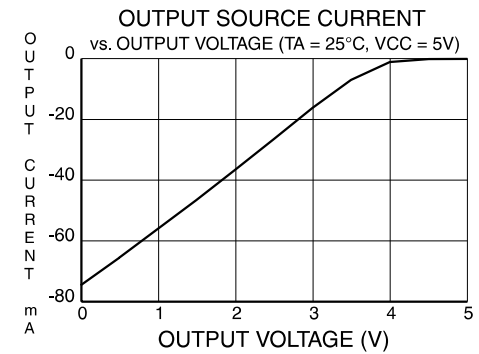
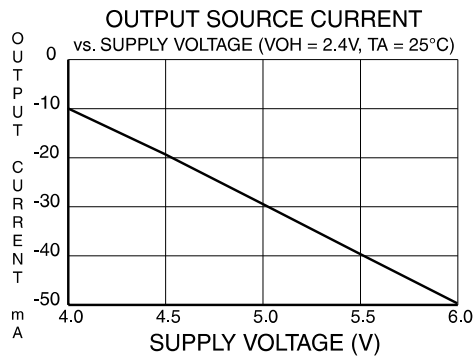
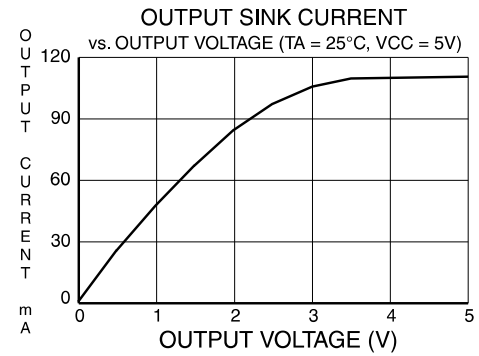
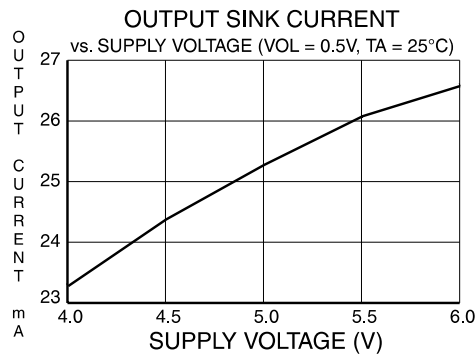
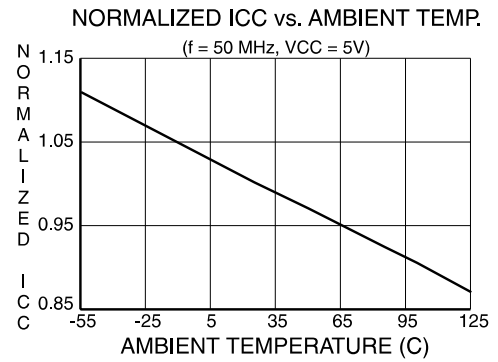
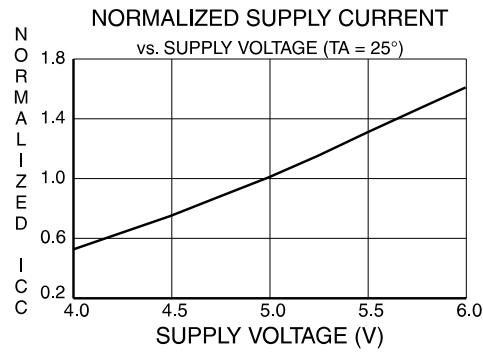
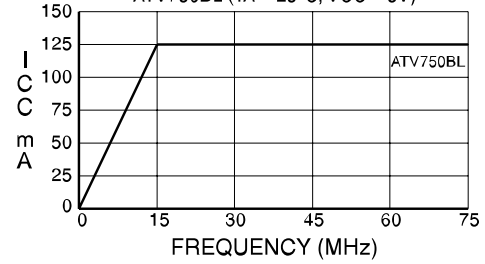
The ATV750B utilizes an advanced 0.65-micron CMOS EPROM technology. This technology's state-of-art features are the optimum combination for PLDs:

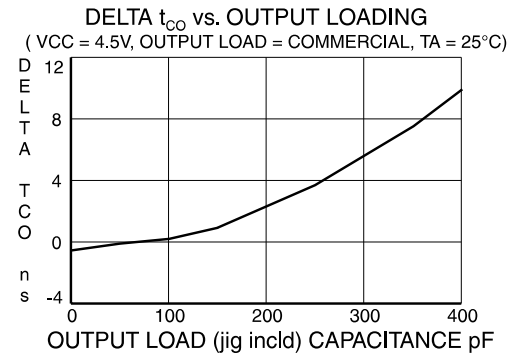
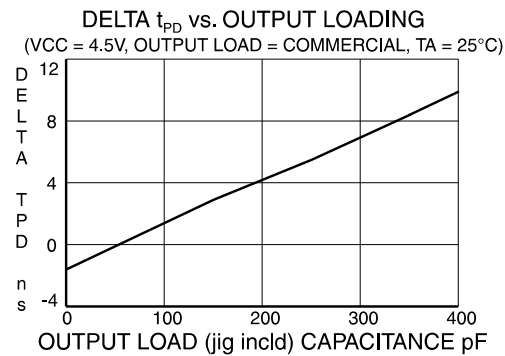
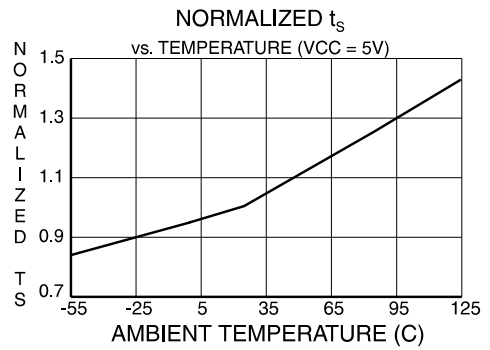
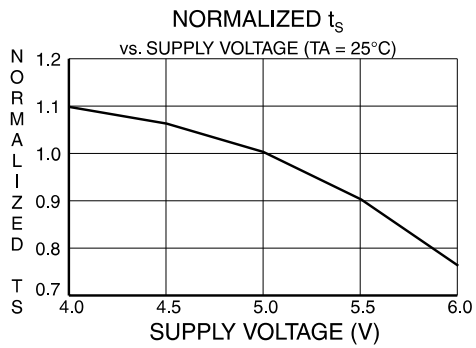
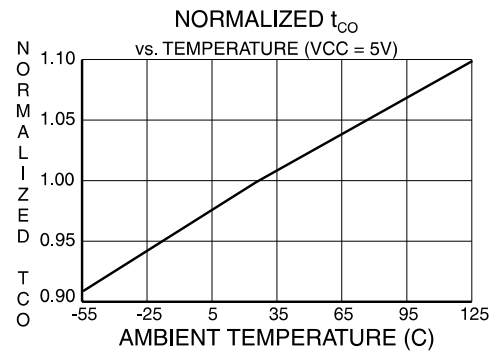
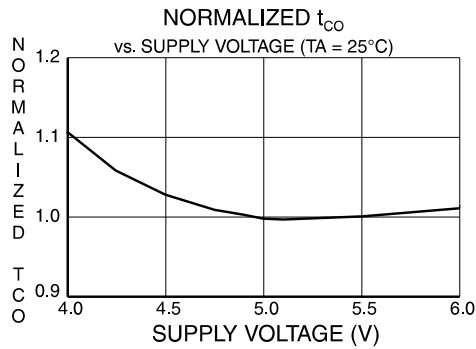
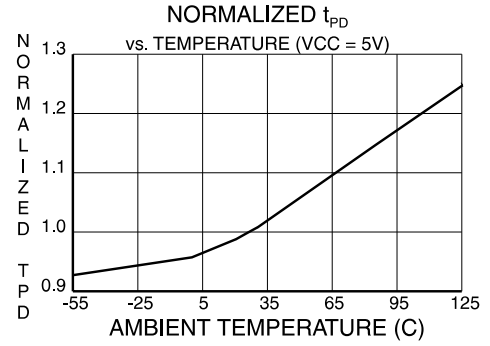
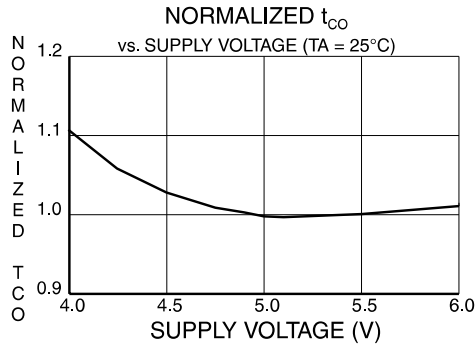
- CMOS technology provides high-speed, low-power, and high noise immunity.
- EPROM technology is the most cost-effective method for producing PLDs – surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

SUPPLY CURRENT vs. INPUT FREQUENCY  
ATV750B (TA = 25°C, VCC = 5V)



SUPPLY CURRENT vs. INPUT FREQUENCY  
ATV750BL (TA = 25°C, VCC = 5V)





## Ordering Information

$t_{PD}$ (ns)	$t_{COS}$ (ns)	Ext. $f_{MAXS}$ (MHz)	Ordering Code	Package	Operation Range
7.5	6.5	95	ATV750B-7JC <sup>(1)</sup> ATV750B-7PC <sup>(1)</sup>	28J 24P3	Commercial (0°C to 70°C)
10	7	74	ATV750B-10JC <sup>(1)</sup> ATV750B-10PC <sup>(1)</sup> ATV750B-10SC <sup>(1)</sup>	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-10JI <sup>(1)</sup> ATV750B-10PI <sup>(1)</sup> ATV750B-10SI <sup>(1)</sup>	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750B-10DM/883 <sup>(2)</sup> ATV750B-10LM/883 <sup>(2)</sup>	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	10	58	ATV750B-15JC <sup>(1)</sup> ATV750B-15PC <sup>(1)</sup> ATV750B-15SC <sup>(1)</sup>	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-15JI <sup>(1)</sup> ATV750B-15PI <sup>(1)</sup> ATV750B-15SI <sup>(1)</sup>	28J 24P3 24S	Industrial (-40°C to 85°C)
			ATV750B-15DM/883 <sup>(2)</sup> ATV750B-15LM/883 <sup>(2)</sup>	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	41	ATV750B-25JC <sup>(1)</sup> ATV750B-25PC <sup>(1)</sup> ATV750B-25SC <sup>(1)</sup>	28J 24P3 24S	Commercial (0°C to 70°C)
			ATV750B-25JI <sup>(1)</sup> ATV750B-25PI <sup>(1)</sup> ATV750B-25SI <sup>(1)</sup>	28J 24P3 24S	Industrial (-40°C to 85°C)
10	7	74	5962-88726 08 LA <sup>(2)</sup> 5962-88726 08 3X <sup>(2)</sup>	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	9	58	5962-88726 09 LA <sup>(2)</sup> 5962-88726 09 3X <sup>(2)</sup>	24DW3 28LW	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Notes: 1. Obsolete, please use ATF750C versions.

2. Continue to be available, but please do not use for new designs. For new designs recommend multiple ATF22V10s.



## Ordering Information (Continued)

$t_{PD}$ (ns)	$t_{COS}$ (ns)	Ext. $f_{MAXS}$ (MHz)	Ordering Code	Package	Operation Range
15	9	92	ATV750BL-15JC <sup>(1)</sup>	28J	Commercial (0°C to 70°C)
			ATV750BL-15PC <sup>(1)</sup>	24P3	
			ATV750BL-15SC <sup>(1)</sup>	24S	
			ATV750BL-15JI <sup>(1)</sup>	28J	Industrial (-40°C to 85°C)
			ATV750BL-15PI <sup>(1)</sup>	24P3	
			ATV750BL-15SI <sup>(1)</sup>	24S	
			ATV750BL-15DM/883 <sup>(2)</sup>	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			ATV750BL-15LM/883 <sup>(2)</sup>	28LW	
25	15	37	ATV750BL-25JC <sup>(1)</sup>	28J	Commercial (0°C to 70°C)
			ATV750BL-25PC <sup>(1)</sup>	24P3	
			ATV750BL-25SC <sup>(1)</sup>	24S	
			ATV750BL-25JI19	28J	Industrial (-40°C to 85°C)
			ATV750BL-25PI <sup>(1)</sup>	24P3	
			ATV750BL-25SI <sup>(1)</sup>	24S	
15	9	92	5962-88726 11 LX <sup>(2)</sup>	24DW3	Military/883C (-55°C to 125°C) Class B, Fully Compliant
			5962-88726 11 3X <sup>(2)</sup>	28LW	

- Notes: 1. Obsolete, please use ATF750C versions.  
2. Continue to be available, but please do not use for new designs. For new designs recommend multiple ATF22V10s.

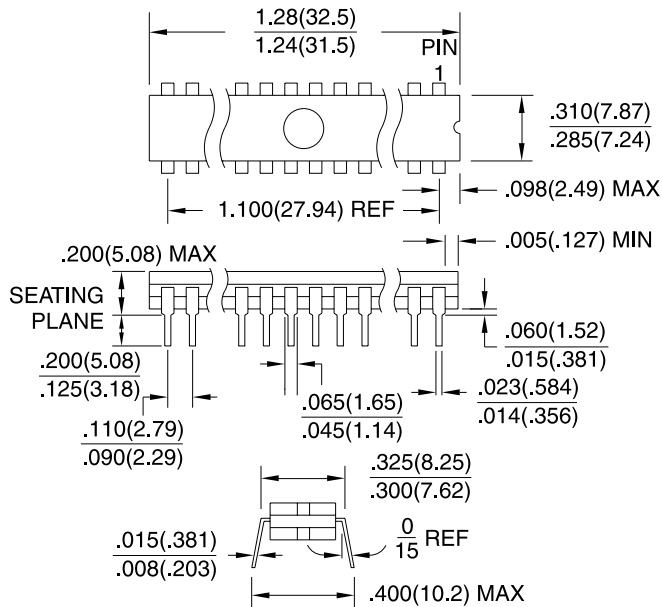
## Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

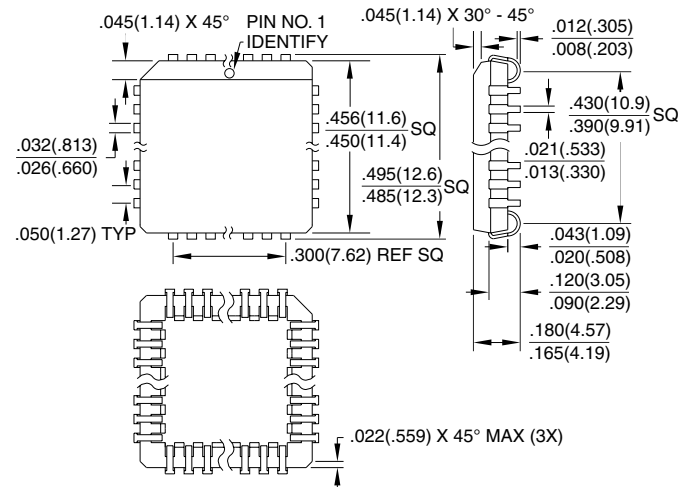
Package Type	
<b>24DW3</b>	24-lead, 0.300" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
<b>28J</b>	28-lead, Plastic J-leaded Chip Carrier OTP (PLCC)
<b>28LW</b>	28-pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
<b>24P3</b>	24-lead, 0.300" Wide, Plastic Dual Inline Package OTP (PDIP)
<b>24S</b>	24-lead, 0.300" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

## Packaging Information

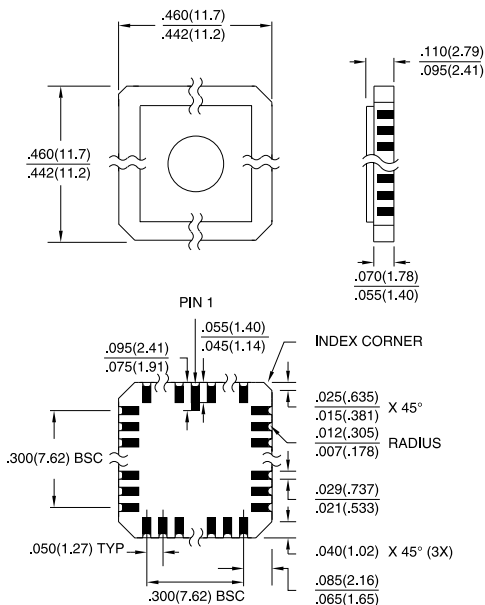
**24DW3**, 24-lead, 0.300" Wide, WIndowed, Ceramic Dual Inline Package (Cerdip)  
Dimensions in Inches and (Millimeters)  
MIL-STD-1835 D-9 CONFIG A



**28J**, 28-lead, Plastic J-leaded Chip Carrier (PLCC)  
Dimensions in Inches and (Millimeters)  
JEDEC STANDARD MS-018 AB

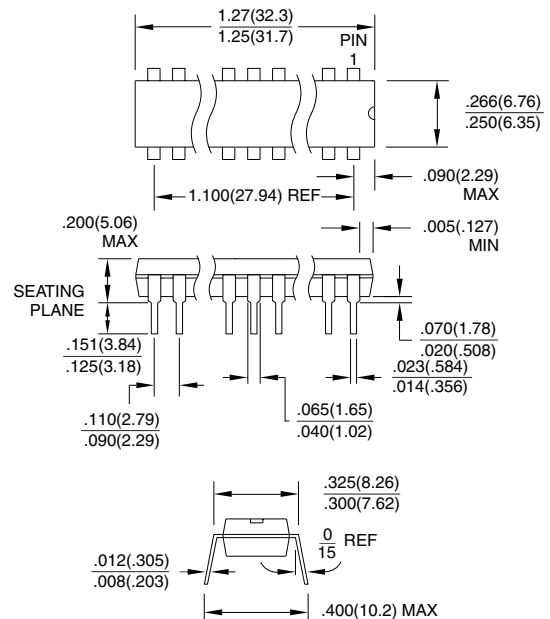


**28LW**, 28-pad, Windowed, Ceramic Leadless Chip Carrier (LCC)  
Dimensions in Inches and (Millimeters)\*  
MIL-STD-1835 C-4



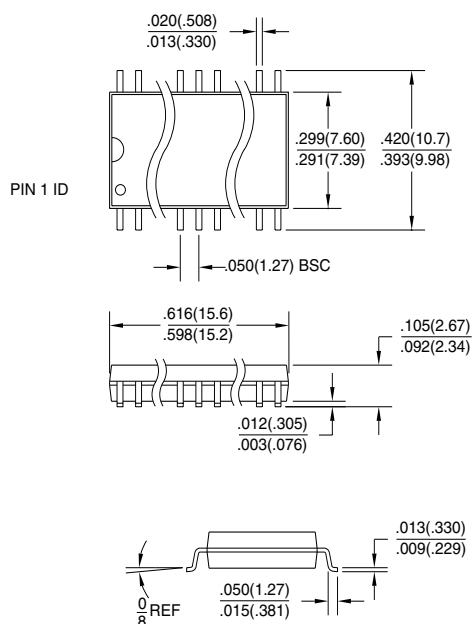
\*Controlling dimension: millimeters

**24P3**, 24-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)  
Dimensions in Inches and (Millimeters)  
JEDEC STANDARD MS-001 AF



## Packaging Information

**24S**, 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)  
Dimensions in Inches and (Millimeters)





## **Atmel Headquarters**

### ***Corporate Headquarters***

2325 Orchard Parkway  
San Jose, CA 95131  
TEL (408) 441-0311  
FAX (408) 487-2600

### ***Europe***

Atmel SarL  
Route des Arsenaux 41  
Casa Postale 80  
CH-1705 Fribourg  
Switzerland  
TEL (41) 26-426-5555  
FAX (41) 26-426-5500

### ***Asia***

Atmel Asia, Ltd.  
Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimhatsui  
East Kowloon  
Hong Kong  
TEL (852) 2721-9778  
FAX (852) 2722-1369

### ***Japan***

Atmel Japan K.K.  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
TEL (81) 3-3523-3551  
FAX (81) 3-3523-7581

## **Atmel Product Operations**

### ***Atmel Colorado Springs***

1150 E. Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906  
TEL (719) 576-3300  
FAX (719) 540-1759

### ***Atmel Grenoble***

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
TEL (33) 4-7658-3000  
FAX (33) 4-7658-3480

### ***Atmel Heilbronn***

Theresienstrasse 2  
POB 3535  
D-74025 Heilbronn, Germany  
TEL (49) 71 31 67 25 94  
FAX (49) 71 31 67 24 23

### ***Atmel Nantes***

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
TEL (33) 0 2 40 18 18 18  
FAX (33) 0 2 40 18 19 60

### ***Atmel Rousset***

Zone Industrielle  
13106 Rousset Cedex, France  
TEL (33) 4-4253-6000  
FAX (33) 4-4253-6001

### ***Atmel Smart Card ICs***

Scottish Enterprise Technology Park  
East Kilbride, Scotland G75 0QR  
TEL (44) 1355-357-000  
FAX (44) 1355-242-743

---

### ***e-mail***

[literature@atmel.com](mailto:literature@atmel.com)

### ***Web Site***

<http://www.atmel.com>

### ***BBS***

1-(408) 436-4309

## **© Atmel Corporation 2001.**

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's web site. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

ATMEL® is the registered trademark of Atmel.

Other terms and product names may be the trademarks of others.



Printed on recycled paper.