XMOS - XLF210-512-TQ128-I20 Datasheet



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Details

Product Status	Obsolete
Core Processor	XCore
Core Size	32-Bit 10-Core
Speed	2000MIPS
Connectivity	-
Peripherals	-
Number of I/O	88
Program Memory Size	2MB (2M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-TQFP Exposed Pad
Supplier Device Package	128-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xlf210-512-tq128-i20

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be used as *open collector* outputs, where signals are driven low if a zero is output, but left high impedance if a one is output. This option is set on a per-port basis.

Data is transferred between the pins and core using a FIFO that comprises a SERDES and transfer register, providing options for serialization and buffered data.

Each port has a 16-bit counter that can be used to control the time at which data is transferred between the port value and transfer register. The counter values can be obtained at any time to find out when data was obtained, or used to delay I/O until some time in the future. The port counter value is automatically saved as a timestamp, that can be used to provide precise control of response times.

The ports and xCONNECT links are multiplexed onto the physical pins. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

6.4 Clock blocks

xCORE devices include a set of programmable clocks called clock blocks that can be used to govern the rate at which ports execute. Each xCORE tile has six clock blocks: the first clock block provides the tile reference clock and runs at a default frequency of 100MHz; the remaining clock blocks can be set to run at different frequencies.

A clock block can use a 1-bit port as its clock source allowing external application clocks to be used to drive the input and output interfaces. xCORE-200 clock blocks optionally divide the clock input from a 1-bit port.

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In many cases I/O signals are accompanied by strobing signals. The xCORE ports can input and interpret strobe (known as readyIn and readyOut) signals generated by external sources, and ports can generate strobe signals to accompany output data.

On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

6.5 Channels and Channel Ends

Logical cores communicate using point-to-point connections, formed between two channel ends. A channel-end is a resource on an xCORE tile, that is allocated by the program. Each channel-end has a unique system-wide identifier that comprises a unique number and their tile identifier. Data is transmitted to a channel-end by an output-instruction; and the other side executes an input-instruction. Data can be passed synchronously or asynchronously between the channel ends.

6.6 xCONNECT Switch and Links

XMOS devices provide a scalable architecture, where multiple xCORE devices can be connected together to form one system. Each xCORE device has an xCONNECT interconnect that provides a communication infrastructure for all tasks that run on the various xCORE tiles on the system.

The interconnect relies on a collection of switches and XMOS links. Each xCORE device has an on-chip switch that can set up circuits or route data. The switches are connected by xConnect Links. An XMOS link provides a physical connection between two switches. The switch has a routing algorithm that supports many different topologies, including lines, meshes, trees, and hypercubes.

The links operate in either 2 wires per direction or 5 wires per direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

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- Program consisting of $s \times 4$ bytes.
- ▶ A 32-bit CRC, or the value 0x0D15AB1E to indicate that no CRC check should be performed.

The program size and CRC are stored least significant byte first. The program is loaded into the lowest memory address of RAM, and the program is started from that address. The CRC is calculated over the byte stream represented by the program size and the program itself. The polynomial used is 0xEDB88320 (IEEE 802.3); the CRC register is initialized with 0xFFFFFFFF and the residue is inverted to produce the CRC.

8.1 Security register

The security register enables security features on the xCORE tile. The features shown in Figure 10 provide a strong level of protection and are sufficient for providing strong IP security.

Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a "secure island" with other tiles free for non-secure user application code.
Secure Boot	5	The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (<i>see</i> §8).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables updates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG interface to this OTP.
	2115	General purpose software accessable security register available to end-users.
	3122	General purpose user programmable JTAG UserID code extension.

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Figure 10: Security register features

9 Memory

9.1 OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in four sectors each containing 512 rows of 32 bits which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

The OTP memory is programmed using three special I/O ports: the OTP address port is a 16-bit port with resource ID 0x100200, the OTP data is written via a 32-bit port with resource ID 0x200100, and the OTP control is on a 16-bit port with ID 0x100300. Programming is performed through libotp and xburn.

9.2 SRAM

Each xCORE Tile integrates a single 256KBSRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

10 ITAG

The JTAG module can be used for loading programs, boundary scan testing, incircuit source-level debugging and programming the OTP memory.



ITAG chain

The JTAG chain structure is illustrated in Figure 11. It comprises a single 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. It has a 4-bit IR and 32-bit DR. It also provides access to a chip TAP that in turn can access the xCORE Tile for loading code and debugging.



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The TRST_N pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the TRST_N pin can be tied to ground to hold the JTAG module in reset.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 12.

Figure 12 IDCODE return value

1.7.	Bit	31											De	evice	e Ide	ntifi	catio	n Re	egist	er											В	it0
12:		Ver	sion								Pa	rt N	umb	er									I	Man	ufac	ture	r Ide	ntity	,			1
DE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1
ue		()	0		0 0				6	5		6			3				3	3											

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 13. The OTP User ID field is read from bits [22:31] of the security register on xCORE Tile 0, *see* §9.1 (all zero on unprogrammed devices).

Figure 13 USERCODE return value

	Bit	Bit31 Usercode Register									В	it0																				
		OTP User ID					Unused Silicon Revision																									
-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0 0)	2			8 0			()			()																

11 Board Integration

The device has the following power supply pins:

- ▶ VDD pins for the xCORE Tile
- VDDIO pins for the I/O lines. Separate I/O supplies are provided for the left, top, and right side of the package; different I/O voltages may be supplied on those. The signal description (Section 4) specifies which I/O is powered from which power-supply
- PLL_AVDD pins for the PLL
- OTP_VCC pins for the OTP

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0V to its final value within 10 ms to ensure correct startup.

The VDDIO and OTP_VCC supply must ramp to its final value before VDD reaches 0.4 V.

The PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7Ω resistor and 100 nF multi-layer ceramic capacitor) is recommended on this pin.

The following ground pins are provided:

- PLL_AGND for PLL_AVDD
- GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 100nF 0402 for each supply pin). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §8). RST_N and must be asserted low during and after power up for 100 ns.

11.1 Land patterns and solder stencils

The package is a 128 pin Thin Quad Flat Package (TQFP) with exposed ground paddle/heat slug on a 0.4mm pitch.

The land patterns and solder stencils will depend on the PCB manufacturing process. We recommend you design them with using the IPC specifications *"Generic Requirements for Surface Mount Design and Land Pattern Standards"* IPC-7351B. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints. The mechanical drawings in Section 13 specify the dimensions and tolerances.

11.2 Ground and Thermal Vias

Vias under the heat slug into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. Typical designs could use 16 vias in a 4 \times 4 grid, equally spaced across the heat slug.

11.3 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour pressure of moisture. Example damage can include bond wire damage, die lifting, internal or external package cracks and/or delamination.

All XMOS devices are Moisture Sensitivity Level (MSL) 3 - devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from *Joint*

IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices J-STD-020 Revision D.





12.3 ESD Stress Voltage

Figure 17 ESD stress voltage

17:	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
SS	HBM	Human body model	-2.00		2.00	KV	
ge	CDM	Charged Device Model	-500		500	V	

12.4 Reset Timing

I.0	Symbol	Parameters	MIN	ТҮР	MAX	UNITS	Notes	
Figure 18:	T(RST)	Reset pulse width	5			μs		
Reset timing	T(INIT)	Initialization time			150	μs	А	
A Characteristic television attention after DCT Nikas and high								

A Shows the time taken to start booting after RST_N has gone high.

12.5 Power Consumption

	Symbol	Parameter	MIN	ТҮР	MAX	UNITS	Notes
	I(DDCQ)	Quiescent VDD current		45		mA	A, B, C
Figure 19:	PD	Tile power dissipation		325		µW/MIPS	A, D, E, F
xCORE Tile	IDD	Active VDD current		570	700	mA	A, G
currents	I(ADDPLL)	PLL_AVDD current		5	7	mA	Н

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages with no switching activity.

- C Includes PLL current.
- D Assumes typical tile and I/O voltages with nominal switching activity.
- E Assumes 1 MHz = 1 MIPS.
- F PD(TYP) value is the usage power consumption under typical operating conditions.
- G Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.
- H PLL_AVDD = 1.0 V



The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.



Package Information 13



SYMBOL	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
D	16	3.00 BS	SC
D1	14	1.00 BS	SC
e	0	.40 BS	C
E	16	3.00 BS	SC
E1	14	1.00 BS	SC
θ	0*	3.5°	7°
61	0*	-	-
9 2	11•	12*	13*
63	11*	12*	13*
с	0.09	-	0.20
c1	0.09	-	0.16
L	0.45	0.60	0.75
Ľ	1	.00 RE	F
R1	0.08	-	-
R2	0.08	-	0.20

REF	TOLERANCES OF FORM AND POSITION					
aaa	0.20					
bbb	0.20					
ccc	0.08					
ddd	0.07					

LF Ref#	Symbol	Min	Nom	Max
1-17-00011	D2	4.60	4.70	4.80
1-11-09011	E2	4.60	4.70	4.80

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13.1 Part Marking



14 Ordering Information

Figure 25:	Product Code	Marking	Qualification	Speed Grade
Orderable	XLF210-512-TQ128-C20	L11092C20	Commercial	1000 MIPS
part numbers	XLF210-512-TQ128-I20	L11092I20	Industrial	1000 MIPS

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Bits	Perm	Init	Description
31:11	RO	-	Reserved
10	DRW		Address space indentifier
9	DRW		Determines the issue mode (DI bit) upon Kernel Entry after Exception or Interrupt.
8	RO		Determines the issue mode (DI bit).
7	DRW		When 1 the thread is in fast mode and will continually issue.
6	DRW		When 1 the thread is paused waiting for events, a lock or another resource.
5	RO	-	Reserved
4	DRW		1 when in kernel mode.
3	DRW		1 when in an interrupt handler.
2	DRW		1 when in an event enabling sequence.
1	DRW		When 1 interrupts are enabled for the thread.
0	DRW		When 1 events are enabled for the thread.

0x10: Debug SSR

B.13 Debug SPC: 0x11

This register contains the value of the SPC register when the debugger was called.

0x11:	Bits	Perm	Init	Description
Debug SPC	31:0	DRW		Value.

B.14 Debug SSP: 0x12

This register contains the value of the SSP register when the debugger was called.

0x12: Debug SSP	Bits	Perm	Init	Description
	31:0	DRW		Value.

B.15 DGETREG operand 1: 0x13

The resource ID of the logical core whose state is to be read.

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B.22 Instruction breakpoint control: 0x40 .. 0x43

This register controls which logical cores may take an instruction breakpoint, and under which condition.

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
15:2	RO	-	Reserved
1	DRW	0	When 0 break when PC == IBREAK_ADDR. When 1 = break when PC != IBREAK_ADDR.
0	DRW	0	When 1 the instruction breakpoint is enabled.

0x40 .. 0x43: Instruction breakpoint control

B.23 Data watchpoint address 1: 0x50 .. 0x53

This set of registers contains the first address for the four data watchpoints.

0x50 .. 0x53: Data watchpoint address 1

Data point	Bits	Perm	Init	Description
ess 1	31:0	DRW		Value.

B.24 Data watchpoint address 2: 0x60 .. 0x63

This set of registers contains the second address for the four data watchpoints.

0x60 .. 0x63: Data watchpoint address 2

Data 1point	Bits	Perm	Init	Description
ress 2	31:0	DRW		Value.

B.25 Data breakpoint control register: 0x70 .. 0x73

This set of registers controls each of the four data watchpoints.

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	Bits	Perm	Init	Description
	31:24	RO	-	Reserved
	23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
0x9C 0x9F:	15:2	RO	-	Reserved
breakpoint control	1	DRW	0	When 0 break when condition A is met. When $1 = break$ when condition B is met.
register	0	DRW	0	When 1 the instruction breakpoint is enabled.

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D Node Configuration

The digital node control registers can be accessed using configuration reads and writes (use write_node_config_reg(device, ...) and read_node_config_reg(device, \rightarrow ...) for reads and writes).

Number	Perm	Description
0x00	RO	Device identification
0x01	RO	System switch description
0x04	RW	Switch configuration
0x05	RW	Switch node identifier
0x06	RW	PLL settings
0x07	RW	System switch clock divider
0x08	RW	Reference clock
0x09	R	System JTAG device ID register
0x0A	R	System USERCODE register
0x0C	RW	Directions 0-7
0x0D	RW	Directions 8-15
0x10	RW	Reserved
0x11	RW	Reserved.
0x1F	RO	Debug source
0x20 0x28	RW	Link status, direction, and network
0x40 0x47	RO	PLink status and network
0x80 0x88	RW	Link configuration and initialization
0xA0 0xA7	RW	Static link configuration

Figure 29: Summary

D.1 Device identification: 0x00

This register contains version and revision identifiers and the mode-pins as sampled at boot-time.

	Bits	Perm	Init	Description
0x00: Device tification	31:24	RO	-	Reserved
	23:16	RO		Sampled values of BootCtl pins on Power On Reset.
	15:8	RO		SSwitch revision.
	7:0	RO		SSwitch version.

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D.2 System switch description: 0x01

This register specifies the number of processors and links that are connected to this switch.

0x01 System switch description

	Bits	Perm	Init	Description
•	31:24	RO	-	Reserved
:	23:16	RO		Number of SLinks on the SSwitch.
	15:8	RO		Number of processors on the SSwitch.
•	7:0	RO		Number of processors on the device.

D.3 Switch configuration: 0x04

This register enables the setting of two security modes (that disable updates to the PLL or any other registers) and the header-mode.

Bits	Perm	Init	Description
31	RW	0	0 = SSCTL registers have write access. $1 = SSCTL$ registers can not be written to.
30:9	RO	-	Reserved
8	RW	0	0 = PLL_CTL_REG has write access. 1 = PLL_CTL_REG can not be written to.
7:1	RO	-	Reserved
0	RW	0	0 = 2-byte headers, $1 = 1$ -byte headers (reset as 0).

0x04: Switch configuration

D.4 Switch node identifier: 0x05

This register contains the node identifier.

0x05
Switch node
identifier

v05·	Bits	Perm	Init	Description
node	31:16	RO	-	Reserved
tifier	15:0	RW	0	The unique ID of this node.

D.5 PLL settings: 0x06

An on-chip PLL multiplies the input clock up to a higher frequency clock, used to clock the I/O, processor, and switch, see Oscillator. Note: a write to this register will cause the tile to be reset.

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D.8 System JTAG device ID register: 0x09

0x09: System JTAG device ID register

	Bits	Perm	Init	Description
•	31:28	RO		
	27:12	RO		
)	11:1	RO		
	0	RO		

D.9 System USERCODE register: 0x0A

0x0A System USERCODE register

:	Bits	Perm	Init	Description
	31:18	RO		JTAG USERCODE value programmed into OTP SR
	17:0	RO		metal fixable ID code

D.10 Directions 0-7: 0x0C

This register contains eight directions, for packets with a mismatch in bits 7..0 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

Bits	Perm	Init	Description
31:28	RW	0	The direction for packets whose dimension is 7.
27:24	RW	0	The direction for packets whose dimension is 6.
23:20	RW	0	The direction for packets whose dimension is 5.
19:16	RW	0	The direction for packets whose dimension is 4.
15:12	RW	0	The direction for packets whose dimension is 3.
11:8	RW	0	The direction for packets whose dimension is 2.
7:4	RW	0	The direction for packets whose dimension is 1.
3:0	RW	0	The direction for packets whose dimension is 0.

0x0C: Directions 0-7

D.11 Directions 8-15: 0x0D

This register contains eight directions, for packets with a mismatch in bits 15..8 of the node-identifier. The direction in which a packet will be routed is goverened by the most significant mismatching bit.

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Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RW		Reserved.
3:2	RO	-	Reserved
1	RW		If set, XCore1 is the source of last GlobalDebug event.
0	RW		If set, XCore0 is the source of last GlobalDebug event.

0x1F: Debug source

D.15 Link status, direction, and network: 0x20 .. 0x28

These registers contain status information for low level debugging (read-only), the network number that each link belongs to, and the direction that each link is part of. The registers control links 0..7.

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		Identify the SRC_TARGET type 0 - SLink, 1 - PLink, 2 - SSCTL, 3 - Undefine.
23:16	RO		When the link is in use, this is the destination link number to which all packets are sent.
15:12	RO	-	Reserved
11:8	RW	0	The direction that this link operates in.
7:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, reset as 0.
3	RO	-	Reserved
2	RO		1 when the current packet is considered junk and will be thrown away.
1	RO		1 when the dest side of the link is in use.
0	RO		1 when the source side of the link is in use.

0x20 .. 0x28: Link status, direction, and network

D.16 PLink status and network: 0x40 .. 0x47

These registers contain status information and the network number that each processor-link belongs to.

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Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		Identify the SRC_TARGET type 0 - SLink, 1 - PLink, 2 - SSCTL, 3 - Undefine.
23:16	RO		When the link is in use, this is the destination link number to which all packets are sent.
15:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, reset as 0.
3	RO	-	Reserved
2	RO		1 when the current packet is considered junk and will be thrown away.
1	RO		1 when the dest side of the link is in use.
0	RO		1 when the source side of the link is in use.

0x40 .. 0x47: PLink status and network

D.17 Link configuration and initialization: 0x80 .. 0x88

These registers contain configuration and debugging information specific to external links. The link speed and width can be set, the link can be initialized, and the link status can be monitored. The registers control links 0..7.

	Bits	Perm	Init	Description
	31	RW		Write to this bit with '1' will enable the XLink, writing '0' will disable it. This bit controls the muxing of ports with overlapping xlinks.
	30	RW	0	0: operate in 2 wire mode; 1: operate in 5 wire mode
	29:28	RO	-	Reserved
	27	RO		Rx buffer overflow or illegal token encoding received.
	26	RO	0	This end of the xlink has issued credit to allow the remote end to transmit
	25	RO	0	This end of the xlink has credit to allow it to transmit.
	24	WO		Clear this end of the xlink's credit and issue a HELLO token.
	23	WO		Reset the receiver. The next symbol that is detected will be the first symbol in a token.
	22	RO	-	Reserved
י. ג ו	21:11	RW	0	Specify min. number of idle system clocks between two contin- uous symbols witin a transmit token -1.
1	10:0	RW	0	Specify min. number of idle system clocks between two contin- uous transmit tokens -1.

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0x80 .. 0x88: Link configuration and initialization

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E JTAG, xSCOPE and Debugging

If you intend to design a board that can be used with the XMOS toolchain and xTAG debugger, you will need an xSYS header on your board. Figure 30 shows a decision diagram which explains what type of xSYS connectivity you need. The three subsections below explain the options in detail.



E.1 No xSYS header

The use of an xSYS header is optional, and may not be required for volume production designs. However, the XMOS toolchain expects the xSYS header; if you do not have an xSYS header then you must provide your own method for writing to flash/OTP and for debugging.

E.2 JTAG-only xSYS header

The xSYS header connects to an xTAG debugger, which has a 20-pin 0.1" female IDC header. The design will hence need a male IDC header. We advise to use a boxed header to guard against incorrect plug-ins. If you use a 90 degree angled header, make sure that pins 2, 4, 6, ..., 20 are along the edge of the PCB.

Connect pins 4, 8, 12, 16, 20 of the xSYS header to ground, and then connect:

 \mathbf{X} M()S

- ▶ TDI to pin 5 of the xSYS header
- TMS to pin 7 of the xSYS header
- TCK to pin 9 of the xSYS header
- TDO to pin 13 of the xSYS header

The RST_N net should be open-drain, active-low, and have a pull-up to VDDIO.

E.3 Full xSYS header

For a full xSYS header you will need to connect the pins as discussed in Section E.2, and then connect a 2-wire xCONNECT Link to the xSYS header. The links can be found in the Signal description table (Section 4): they are labelled XL0, XL1, etc in the function column. The 2-wire link comprises two inputs and outputs, labelled ${}^{1}_{out}$, ${}^{0}_{out}$, ${}^{0}_{in}$, and ${}^{1}_{in}$. For example, if you choose to use XL0 for xSCOPE I/O, you need to connect up XL0 ${}^{1}_{out}$, XL0 ${}^{0}_{out}$, XL0 ${}^{1}_{in}$ as follows:

- XL0¹_{out} (X0D43) to pin 6 of the xSYS header with a 33R series resistor close to the device.
- XL0⁰_{out} (X0D42) to pin 10 of the xSYS header with a 33R series resistor close to the device.
- > XLO_{in}^{0} (X0D41) to pin 14 of the xSYS header.
- > XLO_{in}^{1} (X0D40) to pin 18 of the xSYS header.