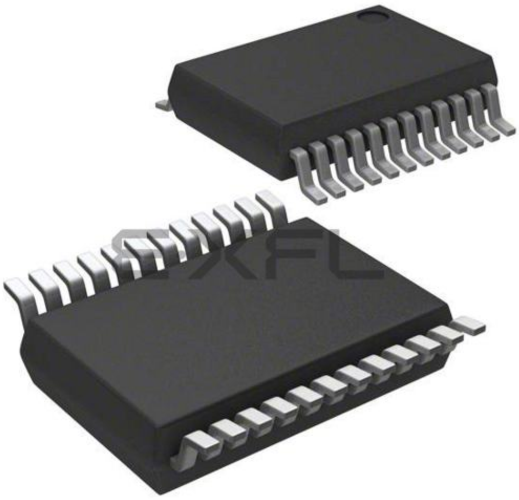
E·XFL

Silicon Labs - C8051F801-GUR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, Temp Sensor, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f801-gur

SFR Definition 21.2. RSTSRC: Reset Source 128
SFR Definition 22.1. CLKSEL: Clock Select 130
SFR Definition 22.2. OSCICL: Internal H-F Oscillator Calibration 131
SFR Definition 22.3. OSCICN: Internal H-F Oscillator Control 132
SFR Definition 22.4. OSCXCN: External Oscillator Control 134
SFR Definition 23.1. XBR0: Port I/O Crossbar Register 0 148
SFR Definition 23.2. XBR1: Port I/O Crossbar Register 1 149
SFR Definition 23.3. P0MASK: Port 0 Mask Register 151
SFR Definition 23.4. P0MAT: Port 0 Match Register 151
SFR Definition 23.5. P1MASK: Port 1 Mask Register 152
SFR Definition 23.6. P1MAT: Port 1 Match Register 152
SFR Definition 23.7. P0: Port 0 153
SFR Definition 23.8. P0MDIN: Port 0 Input Mode 154
SFR Definition 23.9. P0MDOUT: Port 0 Output Mode 154
SFR Definition 23.10. P0SKIP: Port 0 Skip 155
SFR Definition 23.11. P1: Port 1 155
SFR Definition 23.12. P1MDIN: Port 1 Input Mode 156
SFR Definition 23.13. P1MDOUT: Port 1 Output Mode 156
SFR Definition 23.14. P1SKIP: Port 1 Skip 157
SFR Definition 23.15. P2: Port 2 157
SFR Definition 23.16. P2MDOUT: Port 2 Output Mode 158
SFR Definition 24.1. CRC0CN: CRC0 Control 163
SFR Definition 24.2. CRC0IN: CRC Data Input 164
SFR Definition 24.3. CRC0DATA: CRC Data Output 164
SFR Definition 24.4. CRC0AUTO: CRC Automatic Control 165
SFR Definition 24.5. CRC0CNT: CRC Automatic Flash Sector Count 165
SFR Definition 24.6. CRC0FLIP: CRC Bit Flip 166
SFR Definition 25.1. SPI0CFG: SPI0 Configuration 174
SFR Definition 25.2. SPI0CN: SPI0 Control 175
SFR Definition 25.3. SPI0CKR: SPI0 Clock Rate 176
SFR Definition 25.4. SPI0DAT: SPI0 Data 176
SFR Definition 26.1. SMB0CF: SMBus Clock/Configuration 186
SFR Definition 26.2. SMB0CN: SMBus Control 188
SFR Definition 26.3. SMB0ADR: SMBus Slave Address 191
SFR Definition 26.4. SMB0ADM: SMBus Slave Address Mask 191
SFR Definition 26.5. SMB0DAT: SMBus Data 192
SFR Definition 27.1. SCON0: Serial Port 0 Control 206
SFR Definition 27.2. SBUF0: Serial (UART0) Port Data Buffer 207
SFR Definition 28.1. CKCON: Clock Control 210
SFR Definition 28.2. TCON: Timer Control 215
SFR Definition 28.3. TMOD: Timer Mode 216
SFR Definition 28.4. TL0: Timer 0 Low Byte 217
SFR Definition 28.5. TL1: Timer 1 Low Byte 217
SFR Definition 28.6. TH0: Timer 0 High Byte 218
SFR Definition 28.7. TH1: Timer 1 High Byte 218

Table 2.1. Product Selection Guide

Part Number	Digital Port I/Os	Capacitive Sense Channels	Flash Memory (kB)	RAM (Bytes)	10-bit 500 ksps ADC	ADC Channels	Temperature Sensor	Package (RoHS)
C8051F800-GU	17	16	16	512	✓	16	✓	QSOP-24
C8051F801-GU	17	8	16	512	✓	16	✓	QSOP-24
C8051F802-GU	17	—	16	512	✓	16	✓	QSOP-24
C8051F800-GM	17	16	16	512	✓	16	✓	QFN-20
C8051F801-GM	17	8	16	512	✓	16	✓	QFN-20
C8051F802-GM	17	—	16	512	✓	16	✓	QFN-20
C8051F803-GS	13	12	16	512	✓	12	✓	SOIC-16
C8051F804-GS	13	8	16	512	✓	12	✓	SOIC-16
C8051F805-GS	13	—	16	512	✓	12	✓	SOIC-16
C8051F806-GU	17	16	16	512	—	—	—	QSOP-24
C8051F807-GU	17	8	16	512	—	—	—	QSOP-24
C8051F808-GU	17	—	16	512	—	—	—	QSOP-24
C8051F806-GM	17	16	16	512	—	—	—	QFN-20
C8051F807-GM	17	8	16	512	—	—	—	QFN-20
C8051F808-GM	17	—	16	512	—	—	—	QFN-20
C8051F809-GS	13	12	16	512	—	—	—	SOIC-16
C8051F810-GS	13	8	16	512	—	—	—	SOIC-16
C8051F811-GS	13	—	16	512	—	—	—	SOIC-16
C8051F812-GU	17	16	8	512	✓	16	✓	QSOP-24
C8051F813-GU	17	8	8	512	✓	16	✓	QSOP-24
C8051F814-GU	17	—	8	512	✓	16	✓	QSOP-24
C8051F812-GM	17	16	8	512	✓	16	✓	QFN-20
C8051F813-GM	17	8	8	512	✓	16	✓	QFN-20
C8051F814-GM	17	—	8	512	✓	16	✓	QFN-20
C8051F815-GS	13	12	8	512	✓	12	✓	SOIC-16
C8051F816-GS	13	8	8	512	✓	12	✓	SOIC-16
C8051F817-GS	13	—	8	512	✓	12	✓	SOIC-16
C8051F818-GU	17	16	8	512	—	—	—	QSOP-24
C8051F819-GU	17	8	8	512	—	—	—	QSOP-24
C8051F820-GU	17	—	8	512	—	—	—	QSOP-24
C8051F818-GM	17	16	8	512	—	—	—	QFN-20
C8051F819-GM	17	8	8	512	—	—	—	QFN-20
C8051F820-GM	17	—	8	512	—	—	—	QFN-20

4. QFN-20 Package Specifications

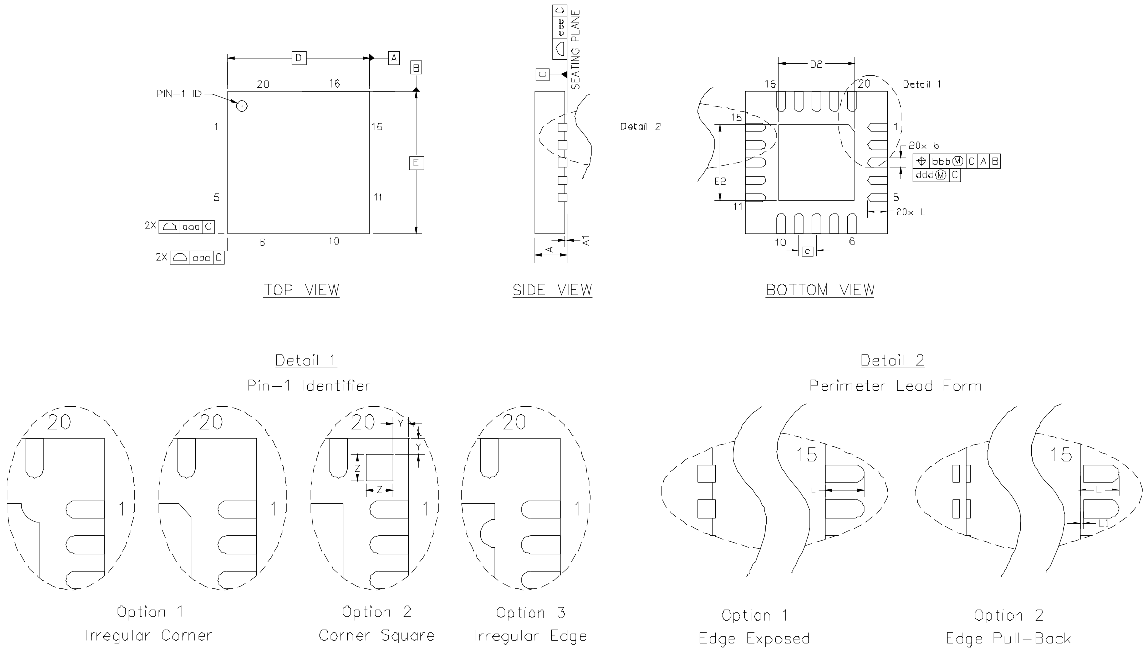


Figure 4.1. QFN-20 Package Drawing

Table 4.1. QFN-20 Package Dimensions

Dimension	Min	Typ	Max	Dimension	Min	Typ	Max
A	0.80	0.90	1.00	L	0.45	0.55	0.65
A1	0.00	0.02	0.05	L1	0.00	—	0.15
b	0.18	0.25	0.30	aaa	—	—	0.15
D	4.00 BSC.			bbb	—	—	0.10
D2	2.00	2.15	2.25	ddd	—	—	0.05
e	0.50 BSC.			eee	—	—	0.08
E	4.00 BSC.			Z	—	0.43	—
E2	2.00	2.15	2.25	Y	—	0.18	—

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VGGD except for custom features D2, E2, Z, Y, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.3.2. Tracking Modes

The AD0TM bit in register ADC0CN enables "delayed conversions", and will delay the actual conversion start by three SAR clock cycles, during which time the ADC will continue to track the input. If AD0TM is left at logic 0, a conversion will begin immediately, without the extra tracking time. For internal start-of-conversion sources, the ADC will track anytime it is not performing a conversion. When the CNVSTR signal is used to initiate conversions, ADC0 will track either when AD0TM is logic 1, or when AD0TM is logic 0 and CNVSTR is held low. See Figure 8.2 for track and convert timing details. Delayed conversion mode is useful when AMUX settings are frequently changed, due to the settling time requirements described in Section “8.3.3. Settling Time Requirements” on page 49.

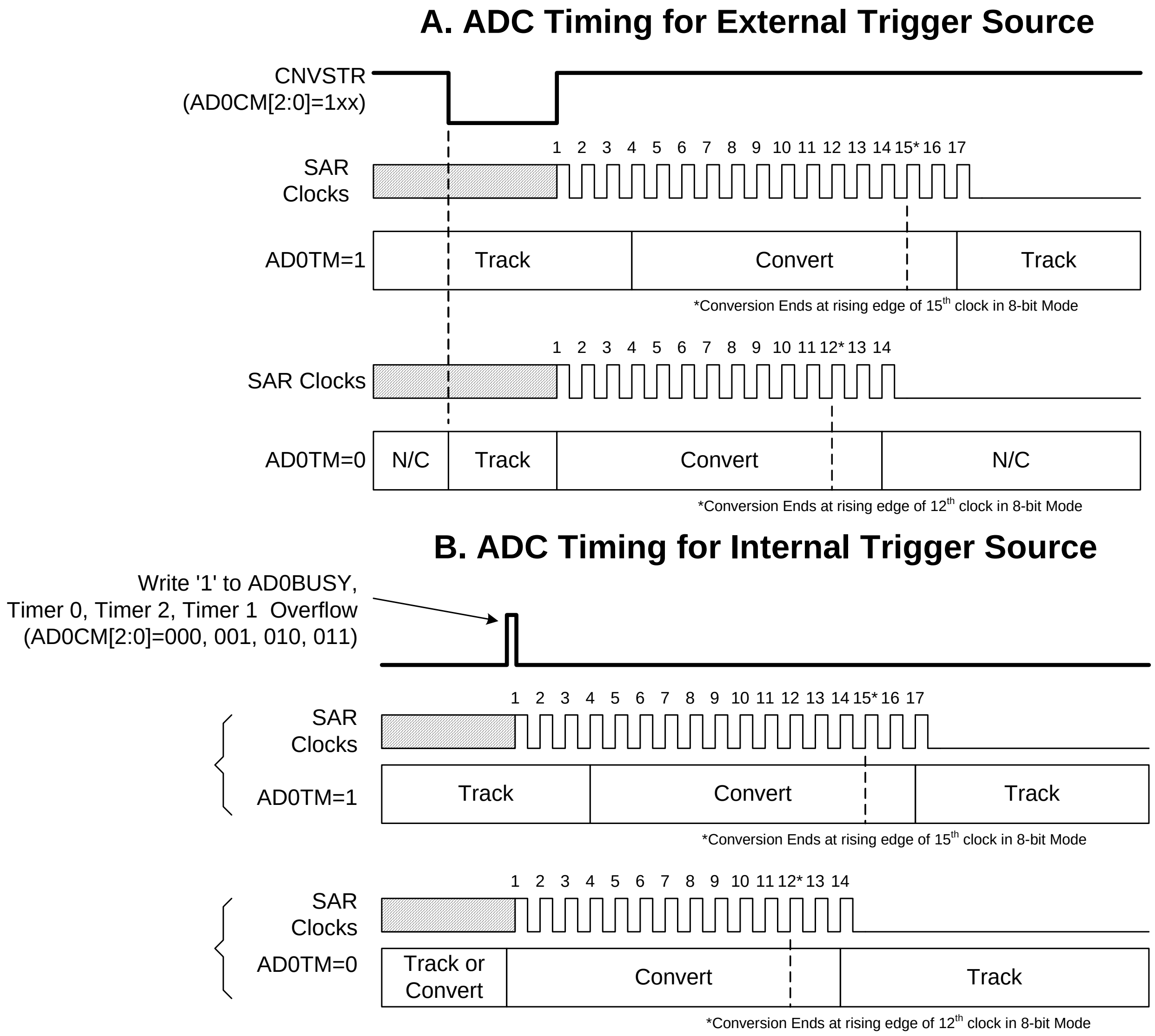

A. ADC Timing for External Trigger Source
CNVSTR
(AD0CM[2:0]=1xx)
SAR
Clocks
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15* 16 17
AD0TM=1
Track
Convert
Track
*Conversion Ends at rising edge of 15th clock in 8-bit Mode
SAR Clocks
1 2 3 4 5 6 7 8 9 10 11 12* 13 14
AD0TM=0
N/C
Track
Convert
N/C
*Conversion Ends at rising edge of 12th clock in 8-bit Mode
B. ADC Timing for Internal Trigger Source
Write '1' to AD0BUSY,
Timer 0, Timer 2, Timer 1 Overflow
(AD0CM[2:0]=000, 001, 010, 011)
SAR
Clocks
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15* 16 17
AD0TM=1
Track
Convert
Track
*Conversion Ends at rising edge of 15th clock in 8-bit Mode
SAR
Clocks
1 2 3 4 5 6 7 8 9 10 11 12* 13 14
AD0TM=0
Track or
Convert
Convert
Track
*Conversion Ends at rising edge of 12th clock in 8-bit Mode

Figure 8.2. 10-Bit ADC Track and Conversion Example Timing

8.3.3. Settling Time Requirements

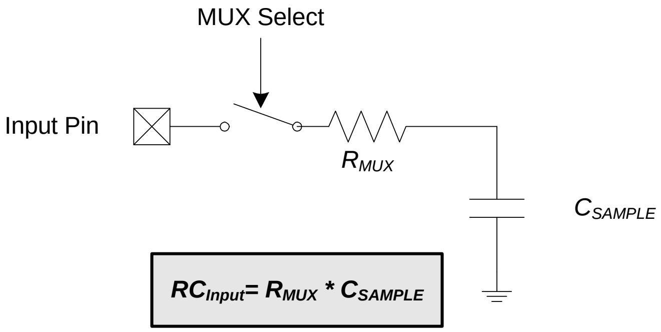
A minimum tracking time is required before each conversion to ensure that an accurate conversion is performed. This tracking time is determined by any series impedance, including the AMUX0 resistance, the the ADC0 sampling capacitance, and the accuracy required for the conversion. In delayed tracking mode, three SAR clocks are used for tracking at the start of every conversion. For many applications, these three SAR clocks will meet the minimum tracking time requirements.

Figure 8.3 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation 8.1. See Table 7.9 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL}C_{SAMPLE}$$

Equation 8.1. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (10).



Note: See electrical specification tables for R_{MUX} and C_{SAMPLE} parameters.

Figure 8.3. ADC0 Equivalent Input Circuits

13. Capacitive Sense (CS0)

The Capacitive Sense subsystem included on the C8051F800/1/3/4/6/7/9, C8051F810/2/3/5/6/8/9, C8051F821/2/4/5/7/8, C8051F830/1/3/4 uses a capacitance-to-digital circuit to determine the capacitance on a port pin. The module can take measurements from different port pins using the module’s analog multiplexer. The multiplexer supports up to 16 channels. See SFR Definition 13.9. “CS0MX: Capacitive Sense Mux Channel Select” on page 81 for channel availability for specific part numbers. The module is enabled only when the CS0EN bit (CS0CN) is set to 1. Otherwise the module is in a low-power shutdown state. The module can be configured to take measurements on one port pin or a group of port pins, using auto-scan. An accumulator can be configured to accumulate multiple conversions on an input channel. Interrupts can be generated when CS0 completes a conversion or when the measured value crosses a threshold defined in CS0THH:L.

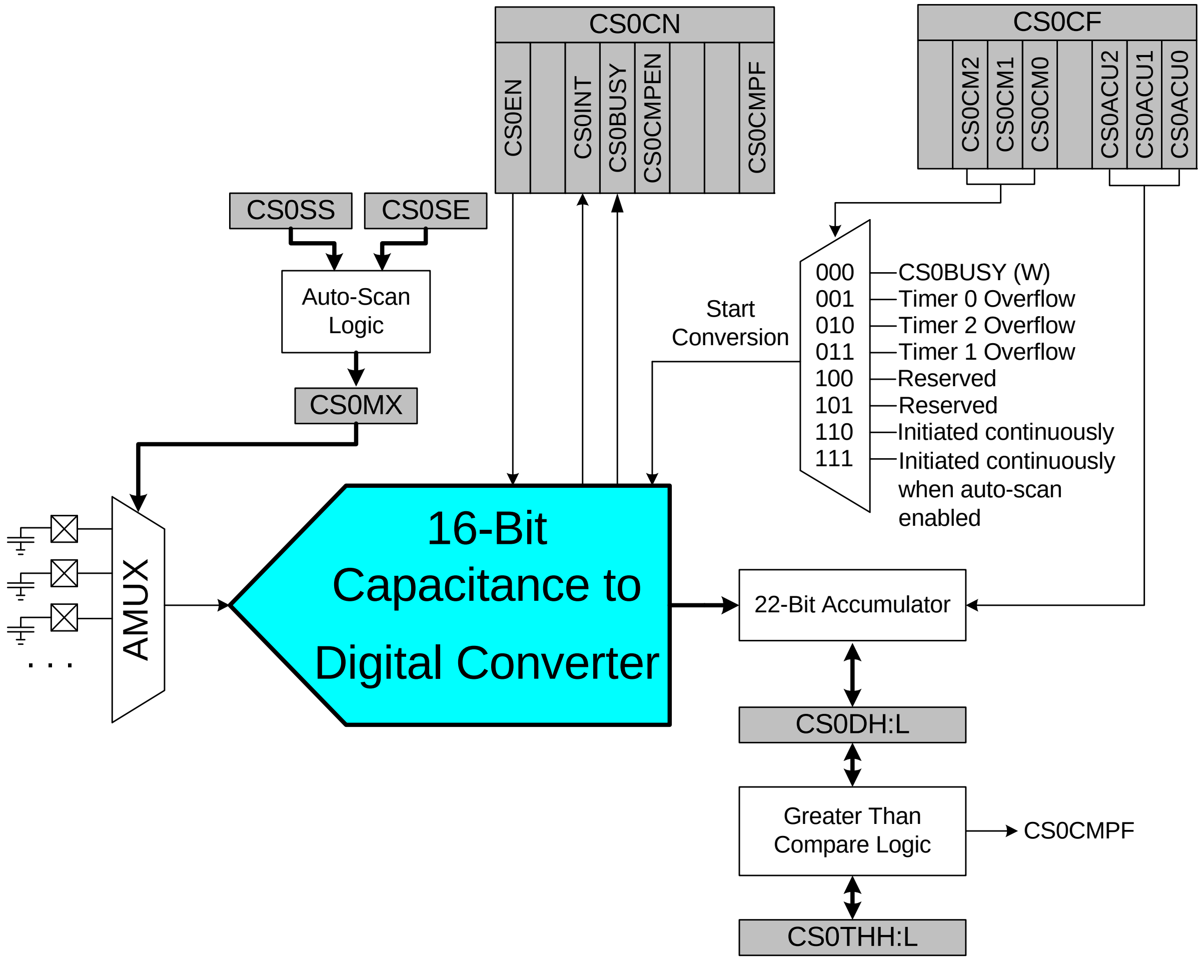


Figure 13.1. CS0 Block Diagram

SFR Definition 13.2. CS0CF: Capacitive Sense Configuration

Bit	7	6	5	4	3	2	1	0
Name		CS0CM[2:0]				CS0ACU[2:0]		
Type	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9E

Bit	Name	Description
7	Unused	Read = 0b; Write = Don't care
6:4	CS0CM[2:0]	**CS0 Start of Conversion Mode Select.** 000: Conversion initiated on every write of 1 to CS0BUSY. 001: Conversion initiated on overflow of Timer 0. 010: Conversion initiated on overflow of Timer 2. 011: Conversion initiated on overflow of Timer 1. 100: Reserved. 101: Reserved. 110: Conversion initiated continuously after writing 1 to CS0BUSY. 111: Auto-scan enabled, conversions initiated continuously after writing 1 to CS0BUSY.
3	Unused	Read = 0b; Write = Don't care
2:0	CS0ACU[2:0]	**CS0 Accumulator Mode Select.** 000: Accumulate 1 sample. 001: Accumulate 4 samples. 010: Accumulate 8 samples. 011: Accumulate 16 samples 100: Accumulate 32 samples. 101: Accumulate 64 samples. 11x: Reserved.

13.6. Capacitive Sense Multiplexer

The input multiplexer can be controlled through two methods. The CS0MX register can be written to through firmware, or the register can be configured automatically using the modules auto-scan functionality (see “13.3. Automatic Scanning”).

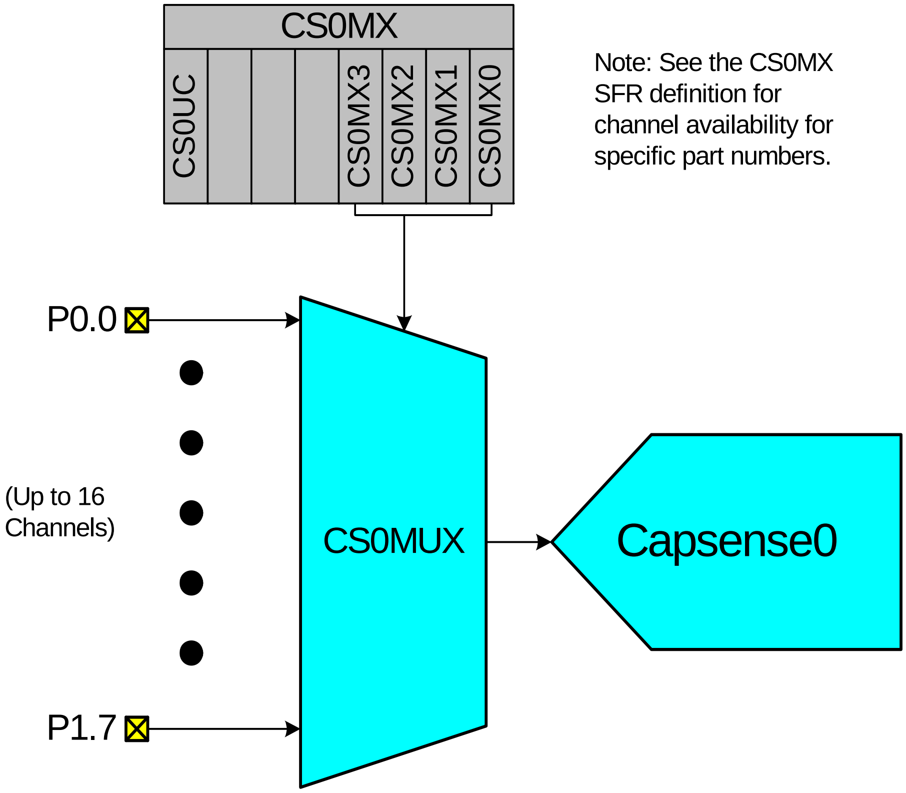

CS0MX
CS0UC
CS0MX3
CS0MX2
CS0MX1
CS0MX0
Note: See the CS0MX SFR definition for channel availability for specific part numbers.
P0.0
(Up to 16 Channels)
P1.7
CS0MUX
Capsense0

Figure 13.3. CS0 Multiplexer Block Diagram

15. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory organization of the C8051F80x-83x device family is shown in Figure 15.1

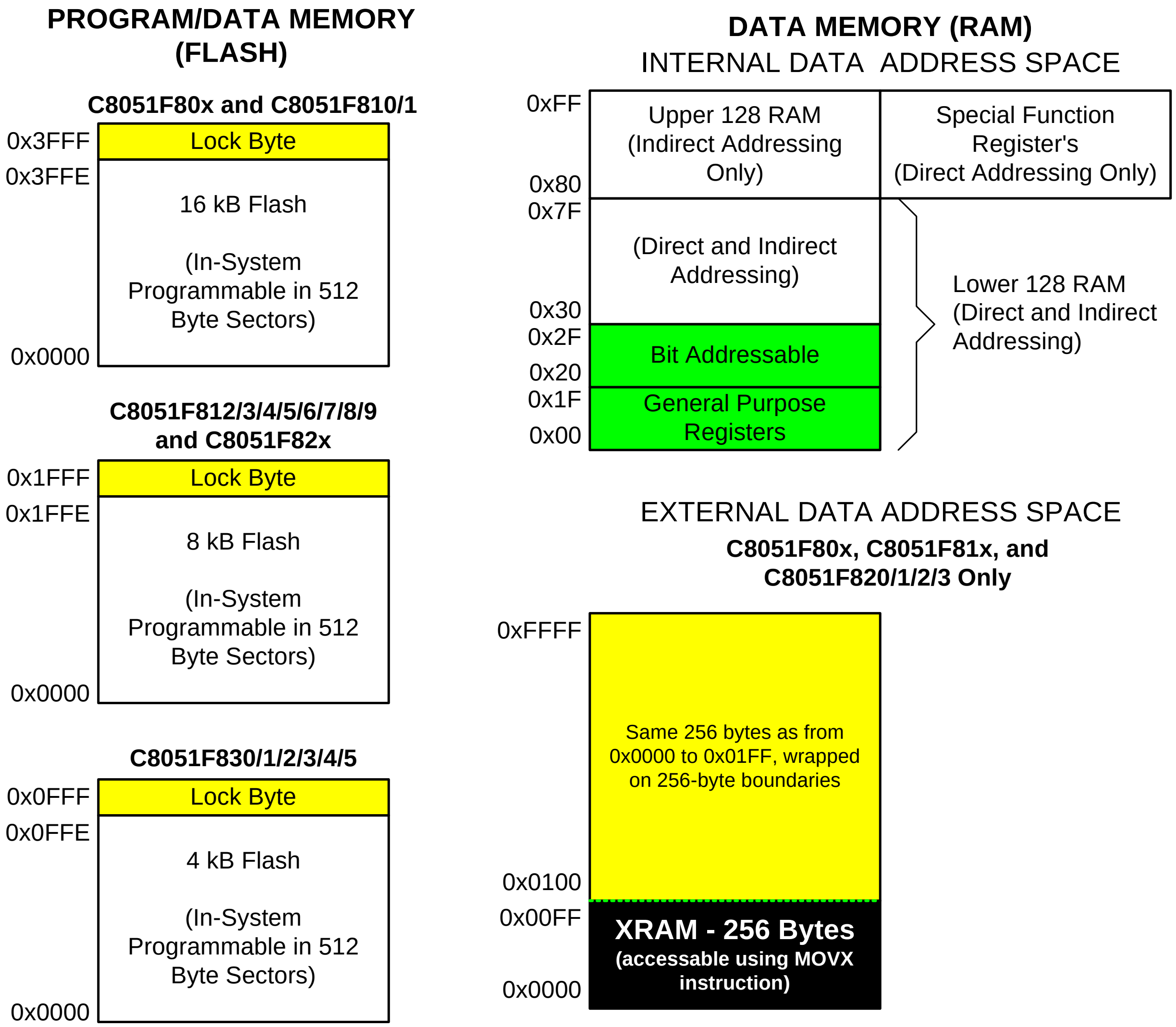

PROGRAM/DATA MEMORY (FLASH)
C8051F80x and C8051F810/1
0x3FFF
Lock Byte
0x3FFE
16 kB Flash
(In-System Programmable in 512 Byte Sectors)
0x0000
C8051F812/3/4/5/6/7/8/9 and C8051F82x
0x1FFF
Lock Byte
0x1FFE
8 kB Flash
(In-System Programmable in 512 Byte Sectors)
0x0000
C8051F830/1/2/3/4/5
0x0FFF
Lock Byte
0x0FFE
4 kB Flash
(In-System Programmable in 512 Byte Sectors)
0x0000
DATA MEMORY (RAM)
INTERNAL DATA ADDRESS SPACE
0xFF
Upper 128 RAM (Indirect Addressing Only)
Special Function Register's (Direct Addressing Only)
0x80
0x7F
(Direct and Indirect Addressing)
0x30
0x2F
Bit Addressable
0x20
0x1F
General Purpose Registers
0x00
Lower 128 RAM (Direct and Indirect Addressing)
EXTERNAL DATA ADDRESS SPACE
C8051F80x, C8051F81x, and C8051F820/1/2/3 Only
0xFFFF
Same 256 bytes as from 0x0000 to 0x01FF, wrapped on 256-byte boundaries
0x0100
0x00FF
XRAM - 256 Bytes
(accessable using MOVX instruction)
0x0000

Figure 15.1. C8051F80x-83x Memory Map

SFR Definition 18.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	ECP0	EADC0	EPCA0	EWADC0	EMAT	ESMB0
Type	W	W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE6

Bit	Name	Function
7	Reserved	Must write 0.
6	Reserved	**Reserved.** Must write 0.
5	ECP0	**Enable Comparator0 (CP0) Interrupt.** This bit sets the masking of the CP0 rising edge or falling edge interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the CP0RIF and CP0FIF flags.
4	EADC0	**Enable ADC0 Conversion Complete Interrupt.** This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the AD0INT flag.
3	EPCA0	**Enable Programmable Counter Array (PCA0) Interrupt.** This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
2	EWADC0	**Enable Window Comparison ADC0 interrupt.** This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).
1	EMAT	**Enable Port Match Interrupts.** This bit sets the masking of the Port Match event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.
0	ESMB0	**Enable SMBus (SMB0) Interrupt.** This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

The following guidelines are recommended for any system that contains routines which write or erase Flash from code.

19.4.1. VDD Maintenance and the VDD Monitor

1. If the system power supply is subject to voltage or current "spikes," add sufficient transient protection devices to the power supply to ensure that the supply voltages listed in the Absolute Maximum Ratings table are not exceeded.
2. Make certain that the minimum VDD rise time specification of 1 ms is met. If the system cannot meet this rise time specification, then add an external VDD brownout circuit to the $\overline{\text{RST}}$ pin of the device that holds the device in reset until VDD reaches the minimum device operating voltage and re-asserts $\overline{\text{RST}}$ if VDD drops below the minimum device operating voltage.
3. Keep the on-chip VDD Monitor enabled and enable the VDD Monitor as a reset source as early in code as possible. This should be the first set of instructions executed after the Reset Vector. For C-based systems, this will involve modifying the startup code added by the C compiler. See your compiler documentation for more details. Make certain that there are no delays in software between enabling the VDD Monitor and enabling the VDD Monitor as a reset source. Code examples showing this can be found in “AN201: Writing to Flash from Firmware," available from the Silicon Laboratories website.

Note: On C8051F80x-83x devices, both the VDD Monitor and the VDD Monitor reset source must be enabled to write or erase Flash without generating a Flash Error Device Reset.

On C8051F80x-83x devices, both the VDD Monitor and the VDD Monitor reset source are enabled by hardware after a power-on reset.

4. As an added precaution, explicitly enable the VDD Monitor and enable the VDD Monitor as a reset source inside the functions that write and erase Flash memory. The VDD Monitor enable instructions should be placed just after the instruction to set PSWE to a 1, but before the Flash write or erase operation instruction.
5. Make certain that all writes to the RSTSRC (Reset Sources) register use direct assignment operators and explicitly DO NOT use the bit-wise operators (such as AND or OR). For example, "RSTSRC = 0x02" is correct, but "RSTSRC |= 0x02" is incorrect.
6. Make certain that all writes to the RSTSRC register explicitly set the PORSF bit to a 1. Areas to check are initialization code which enables other reset sources, such as the Missing Clock Detector or Comparator, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.

19.4.2. PSWE Maintenance

1. Reduce the number of places in code where the PSWE bit (b0 in PSCTL) is set to a 1. There should be exactly one routine in code that sets PSWE to a 1 to write Flash bytes and one routine in code that sets both PSWE and PSEE both to a 1 to erase Flash pages.
2. Minimize the number of variable accesses while PSWE is set to a 1. Handle pointer address updates and loop maintenance outside the "PSWE = 1;... PSWE = 0;" area. Code examples showing this can be found in “AN201: Writing to Flash from Firmware," available from the Silicon Laboratories website.
3. Disable interrupts prior to setting PSWE to a 1 and leave them disabled until after PSWE has been reset to 0. Any interrupts posted during the Flash write or erase operation will be serviced in priority order after the Flash operation has been completed and interrupts have been re-enabled by software.
4. Make certain that the Flash write and erase pointer variables are not located in XRAM. See your compiler documentation for instructions regarding how to explicitly locate variables in different memory areas.
5. Add address bounds checking to the routines that write or erase Flash memory to ensure that a routine called with an illegal address does not result in modification of the Flash.

23.3. Priority Crossbar Decoder

The Priority Crossbar Decoder assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which is always at pins 4 and 5). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Because of the nature of the Priority Crossbar Decoder, not all peripherals can be located on all port pins. Figure 23.4 maps peripherals to the potential port pins on which the peripheral I/O can appear.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to P0.0 if VREF is used, P0.1 if AGND is used, P0.3 and/or P0.2 if the external oscillator circuit is enabled, P0.6 if the ADC is configured to use the external conversion start signal (CNVSTR), and any selected ADC, Comparator, or Capacitive Sense inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin.

Registers XBR0, XBR1, and XBR2 are used to assign the digital I/O resources to the physical I/O Port pins. Note that when the SMBus is selected, the Crossbar assigns both pins associated with the SMBus (SDA and SCL); when a UART is selected, the Crossbar assigns both pins associated with the UART (TX and RX). UART0 pin assignments are fixed for bootloading purposes: UART TX0 is always assigned to P0.4; UART RX0 is always assigned to P0.5. Standard Port I/Os appear contiguously after the prioritized functions have been assigned.

Important Note: The SPI can be operated in either 3-wire or 4-wire modes, depending on the state of the NSSMD1–NSSMD0 bits in register SPI0CN. According to the SPI mode, the NSS signal may or may not be routed to a Port pin.

SFR Definition 24.2. CRC0IN: CRC Data Input

Bit	7	6	5	4	3	2	1	0
Name	CRC0IN[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xDD

Bit	Name	Function
7:0	CRC0IN[7:0]	**CRC0 Data Input.** Each write to CRC0IN results in the written data being computed into the existing CRC result according to the CRC algorithm described in Section 24.1

SFR Definition 24.3. CRC0DATA: CRC Data Output

Bit	7	6	5	4	3	2	1	0
Name	CRC0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xDE

Bit	Name	Function
7:0	CRC0DAT[7:0]	**CRC0 Data Output.** Each read or write performed on CRC0DAT targets the CRC result bits pointed to by the CRC0 Result Pointer (CRC0PNT bits in CRC0CN).

SFR Definition 24.4. CRC0AUTO: CRC Automatic Control

Bit	7	6	5	4	3	2	1	0
Name	AUTOEN	CRCCPT	Reserved	CRC0ST[4:0]				
Type	R/W							
Reset	0	1	0	0	0	0	0	0

SFR Address = 0xD2

Bit	Name	Function
7	AUTOEN	**Automatic CRC Calculation Enable.** When AUTOEN is set to 1, any write to CRC0CN will initiate an automatic CRC starting at Flash sector CRC0ST and continuing for CRC0CNT sectors.
6	CRCCPT	**Automatic CRC Calculation Complete.** Set to 0 when a CRC calculation is in progress. Code execution is stopped during a CRC calculation, therefore reads from firmware will always return 1.
5	Reserved	Must write 0.
4:0	CRC0ST[4:0]	**Automatic CRC Calculation Starting Flash Sector.** These bits specify the Flash sector to start the automatic CRC calculation. The starting address of the first Flash sector included in the automatic CRC calculation is CRC0ST x 512.

SFR Definition 24.5. CRC0CNT: CRC Automatic Flash Sector Count

Bit	7	6	5	4	3	2	1	0
Name			CRC0CNT[5:0]					
Type	R	R	R/W					
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xD3

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don’t Care.
5:0	CRC0CNT[5:0]	**Automatic CRC Calculation Flash Sector Count.** These bits specify the number of Flash sectors to include when performing an automatic CRC calculation. The base address of the last flash sector included in the automatic CRC calculation is equal to (CRC0ST + CRC0CNT) x 512.

26.5.2. Read Sequence (Master)

During a read sequence, an SMBus master reads data from a slave device. The master in this transfer will be a transmitter during the address byte, and a receiver during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 1 (READ). Serial data is then received from the slave on SDA while the SMBus outputs the serial clock. The slave transmits one or more bytes of serial data.

If hardware ACK generation is disabled, the ACKRQ is set to 1 and an interrupt is generated after each received byte. Software must write the ACK bit at that time to ACK or NACK the received byte.

With hardware ACK generation enabled, the SMBus hardware will automatically generate the ACK/NACK, and then post the interrupt. **It is important to note that the appropriate ACK or NACK value should be set up by the software prior to receiving the byte when hardware ACK generation is enabled.**

Writing a 1 to the ACK bit generates an ACK; writing a 0 generates a NACK. Software should write a 0 to the ACK bit for the last data transfer, to transmit a NACK. The interface exits Master Receiver Mode after the STO bit is set and a STOP is generated. The interface will switch to Master Transmitter Mode if SMB0DAT is written while an active Master Receiver. Figure 26.6 shows a typical master read sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur at different places in the sequence, depending on whether hardware ACK generation is enabled. The interrupt occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled.

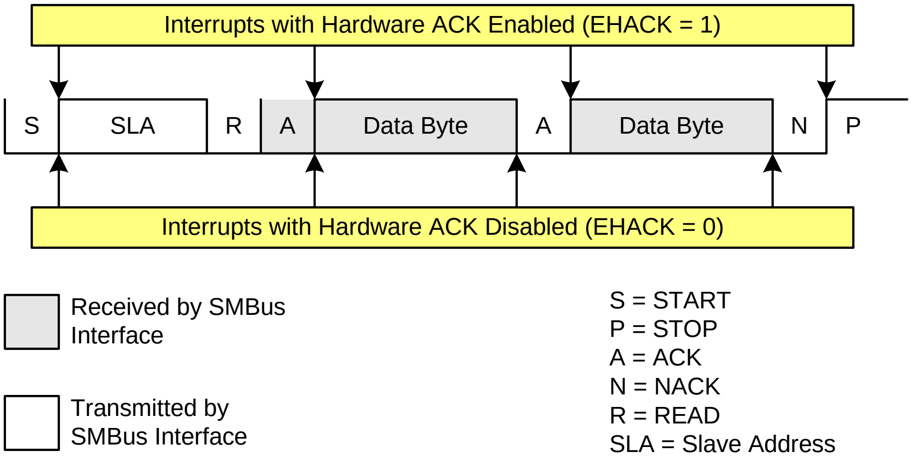

Interrupts with Hardware ACK Enabled (EHACK = 1)
S
SLA
R
A
Data Byte
A
Data Byte
N
P
Interrupts with Hardware ACK Disabled (EHACK = 0)
Received by SMBus Interface
Transmitted by SMBus Interface
S = START
P = STOP
A = ACK
N = NACK
R = READ
SLA = Slave Address

Figure 26.6. Typical Master Read Sequence

Table 26.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1) (Continued)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	—
Slave Receiver	0010	0	0	X	A slave address + R/W was received; ACK sent.	If Write, Set ACK for first data byte.	0	0	1	0000
						If Read, Load SMB0DAT with data byte	0	0	X	0100
		0	1	X	Lost arbitration as master; slave address + R/W received; ACK sent.	If Write, Set ACK for first data byte.	0	0	1	0000
						If Read, Load SMB0DAT with data byte	0	0	X	0100
						Reschedule failed transfer	1	0	X	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	—
		0	1	X	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0	—
	0000	0	0	X	A slave byte was received.	Set ACK for next data byte; Read SMB0DAT.	0	0	1	0000
						Set NACK for next data byte; Read SMB0DAT.	0	0	0	0000
Bus Error Condition	0010	0	1	X	Lost arbitration while attempting a repeated START.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0001	0	1	X	Lost arbitration due to a detected STOP.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110
	0000	0	1	X	Lost arbitration while transmitting a data byte as master.	Abort failed transfer.	0	0	X	—
						Reschedule failed transfer.	1	0	X	1110

27.1. Enhanced Baud Rate Generation

The UART0 baud rate is generated by Timer 1 in 8-bit auto-reload mode. The TX clock is generated by TL1; the RX clock is generated by a copy of TL1 (shown as RX Timer in Figure 27.2), which is not user-accessible. Both TX and RX Timer overflows are divided by two to generate the TX and RX baud rates. The RX Timer runs when Timer 1 is enabled, and uses the same reload value (TH1). However, an RX Timer reload is forced when a START condition is detected on the RX pin. This allows a receive to begin any time a START is detected, independent of the TX Timer state.

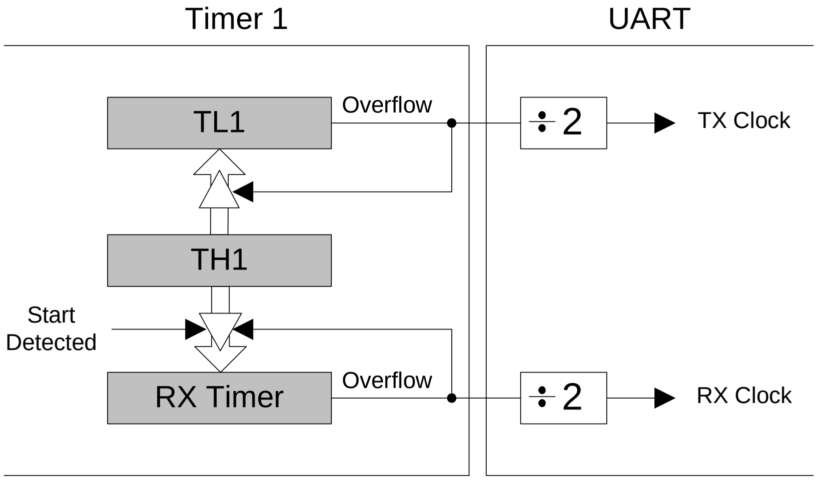


Figure 27.2. UART0 Baud Rate Logic

Timer 1 should be configured for Mode 2, 8-bit auto-reload (see Section “28.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload” on page 212). The Timer 1 reload value should be set so that overflows will occur at two times the desired UART baud rate frequency. Note that Timer 1 may be clocked by one of six sources: SYSCLK, SYSCLK/4, SYSCLK/12, SYSCLK/48, the external oscillator clock/8, or an external input T1. For any given Timer 1 clock source, the UART0 baud rate is determined by Equation 27.1-A and Equation 27.1-B.

A) $$\text{UartBaudRate} = \frac{1}{2} \times \text{T1\_Overflow\_Rate}$$

B) $$\text{T1\_Overflow\_Rate} = \frac{\text{T1}_{\text{CLK}}}{256 - \text{TH1}}$$

Equation 27.1. UART0 Baud Rate

Where $T1_{CLK}$ is the frequency of the clock supplied to Timer 1, and *T1H* is the high byte of Timer 1 (reload value). Timer 1 clock frequency is selected as described in Section “28. Timers” on page 209. A quick reference for typical baud rates and system clock frequencies is given in Table 27.1 through Table 27.2. The internal oscillator may still generate the system clock when the external oscillator is driving Timer 1.

27.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown in Figure 27.3.

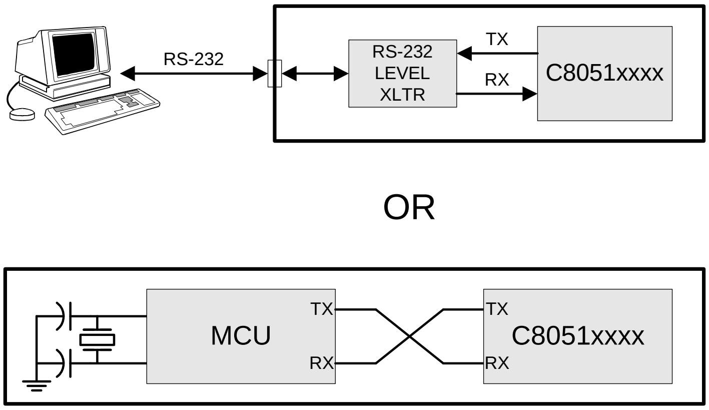


Figure 27.3. UART Interconnect Diagram

27.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 is set.

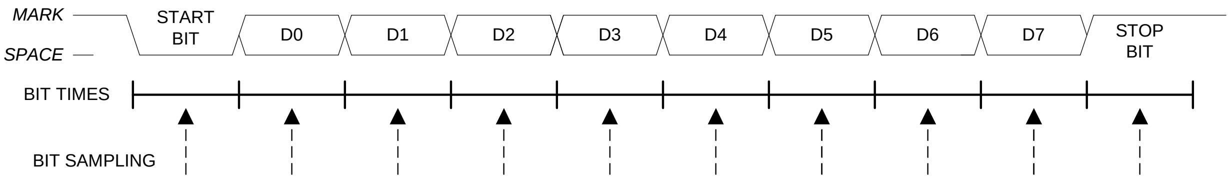


Figure 27.4. 8-Bit UART Timing Diagram

SFR Definition 28.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8C

Bit	Name	Function
7:0	TH0[7:0]	**Timer 0 High Byte.** The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 28.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8D

Bit	Name	Function
7:0	TH1[7:0]	**Timer 1 High Byte.** The TH1 register is the high byte of the 16-bit Timer 1.