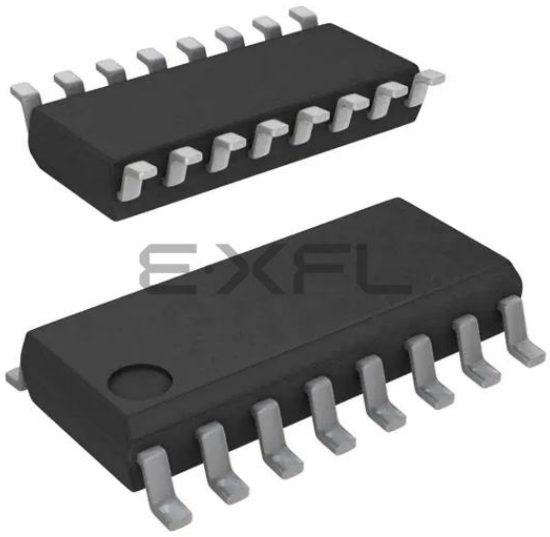

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f805-gsr

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F80x-83x

Name	Pin QSOP-24	Pin QFN-20	Pin SOIC-16	Type	Description
GND	5	2	4		Ground. This ground connection is required. The center pad may optionally be connected to ground as well on the QFN-20 packages.
V_{DD}	6	3	5		Power Supply Voltage.
$\overline{RST}$/	7	4	6	D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 10 µs.
C2CK				D I/O	Clock signal for the C2 Debug Interface.
P2.0/	8	5	7	D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
C2D				D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
P0.0/	4	1	3	D I/O or A In	Port 0.0.
VREF				A In	External VREF input.
P0.1	3	20	2	D I/O or A In	Port 0.1.
P0.2/	2	19	1	D I/O or A In	Port 0.2.
XTAL1				A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/	23	18	16	D I/O or A In	Port 0.3.
XTAL2				A I/O or D In	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	22	17	15	D I/O or A In	Port 0.4.

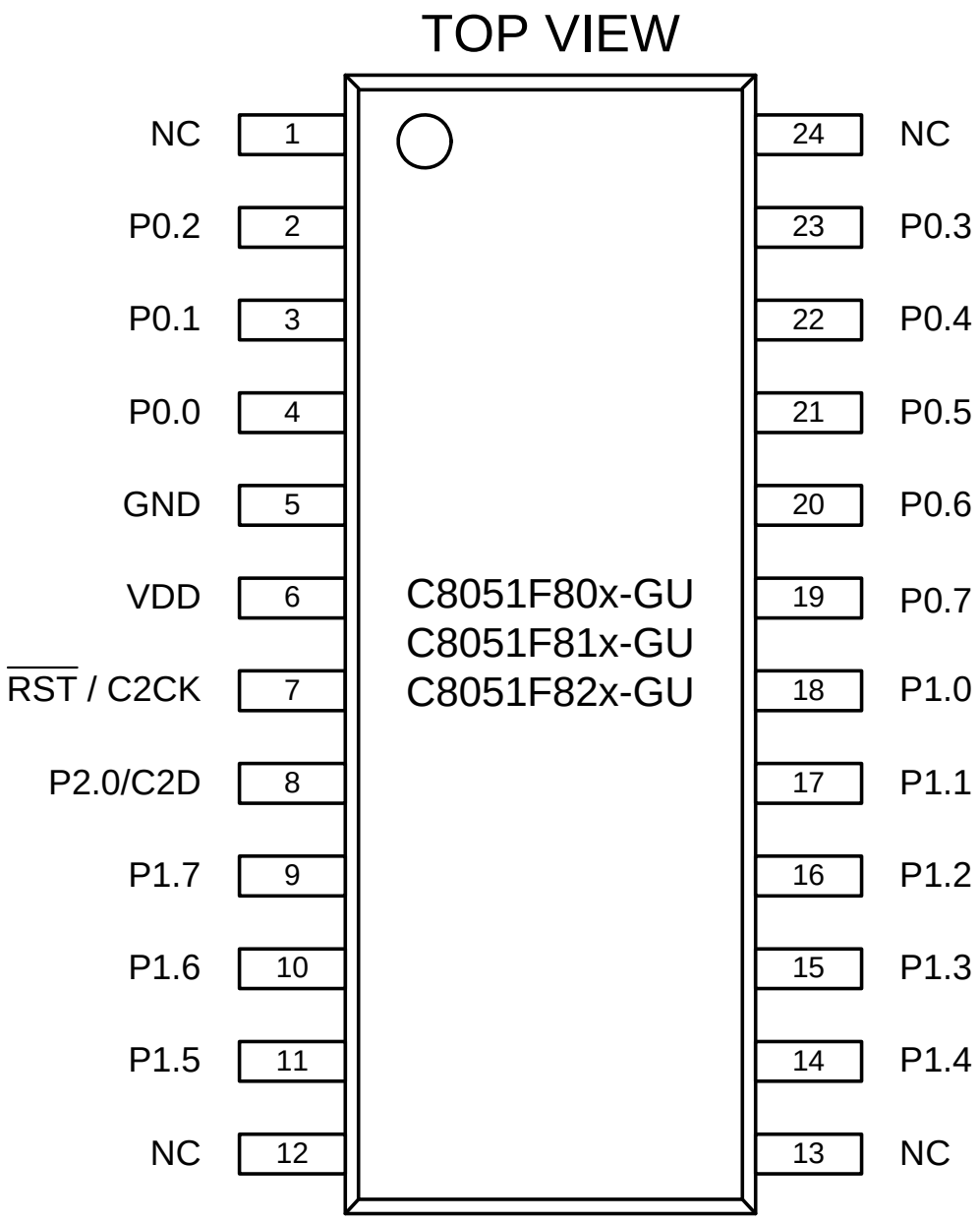

Figure 3.2. QSOP-24 Pinout Diagram (Top View)

8.4. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 8.5. ADC0GTH: ADC0 Greater-Than Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTH[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC4

Bit	Name	Function
7:0	ADC0GTH[7:0]	**ADC0 Greater-Than Data Word High-Order Bits.**

SFR Definition 8.6. ADC0GTL: ADC0 Greater-Than Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC3

Bit	Name	Function
7:0	ADC0GTL[7:0]	**ADC0 Greater-Than Data Word Low-Order Bits.**

SFR Definition 8.9. ADC0MX: AMUX0 Channel Select

Bit	7	6	5	4	3	2	1	0
Name				AMX0P[3:0]				
Type	R	R	R	R/W				
Reset	0	0	0	1	1	1	1	1

SFR Address = 0xBB

Bit	Name	Function		
7:5	Unused	Read = 000b; Write = Don't Care.		
4:0	AMX0P[4:0]	**AMUX0 Positive Input Selection.**		
			20-Pin and 24-Pin Devices	**16-Pin Devices**
		00000:	P0.0	P0.0
		00001:	P0.1	P0.1
		00010:	P0.2	P0.2
		00011:	P0.3	P0.3
		00100:	P0.4	P0.4
		00101:	P0.5	P0.5
		00110:	P0.6	P0.6
		00111:	P0.7	P0.7
		01000	P1.0	P1.0
		01001	P1.1	P1.1
		01010	P1.2	P1.2
		01011	P1.3	P1.3
		01100	P1.4	Reserved.
		01101	P1.5	Reserved.
		01110	P1.6	Reserved.
		01111	P1.7	Reserved.
		10000:	Temp Sensor	Temp Sensor
		10001:	VREG Output	VREG Output
		10010:	VDD	VDD
		10011:	GND	GND
		10100 – 11111:	no input selected	

9. Temperature Sensor

An on-chip temperature sensor is included on the C8051F800/1/2/3/4/5, C8051F812/3/4/5/6/7, C8051F824/5/6, and C8051F830/1/2 which can be directly accessed via the ADC multiplexer in single-ended configuration. To use the ADC to measure the temperature sensor, the ADC mux channel should be configured to connect to the temperature sensor. The temperature sensor transfer function is shown in Figure 9.1. The output voltage (V_{TEMP}) is the positive ADC input when the ADC multiplexer is set correctly.

The TEMPE bit in register REF0CN enables/disables the temperature sensor, as described in SFR Definition 10.1. While disabled, the temperature sensor defaults to a high impedance state and any ADC measurements performed on the sensor will result in meaningless data. Refer to Table 7.11 for the slope and offset parameters of the temperature sensor.

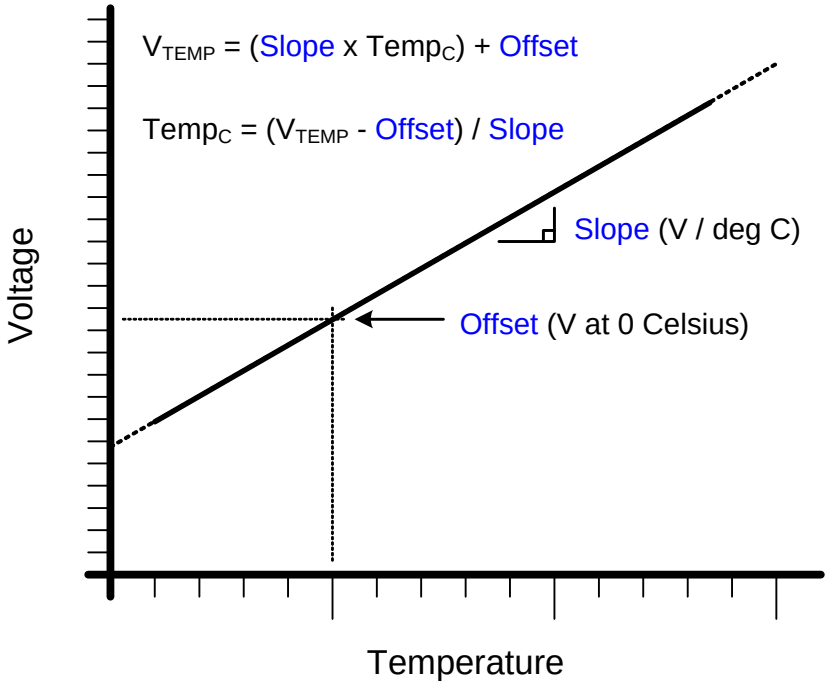

Figure 9.1. Temperature Sensor Transfer Function

9.1. Calibration

The uncalibrated temperature sensor output is extremely linear and suitable for relative temperature measurements (see Table 5.1 for linearity specifications). For absolute temperature measurements, offset and/or gain calibration is recommended. Typically a 1-point (offset) calibration includes the following steps:

1. Control/measure the ambient temperature (this temperature must be known).
2. Power the device, and delay for a few seconds to allow for self-heating.
3. Perform an ADC conversion with the temperature sensor selected as the ADC's input.
4. Calculate the offset characteristics, and store this value in non-volatile memory for use with subsequent temperature sensor measurements.

Figure 5.3 shows the typical temperature sensor error assuming a 1-point calibration at 0 °C.

Parameters that affect ADC measurement, in particular the voltage reference value, will also affect temperature measurement.

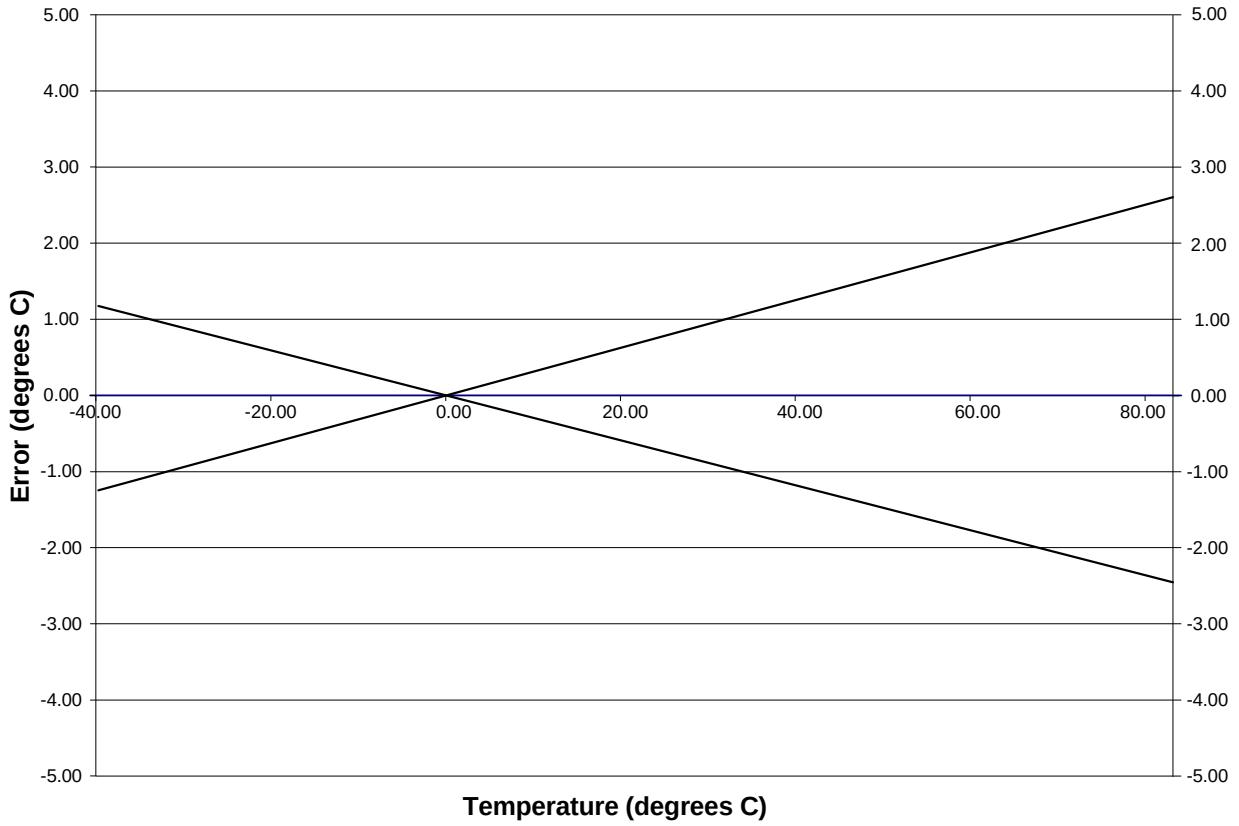

Figure 9.2. Temperature Sensor Error with 1-Point Calibration at 0 °C

SFR Definition 12.3. CPT0MX: Comparator0 MUX Selection

Bit	7	6	5	4	3	2	1	0
Name	CMX0N[3:0]				CMX0P[3:0]			
Type	R/W				R/W			
Reset	1	1	1	1	1	1	1	1

SFR Address = 0x9F

Bit	Name	Function		
7:4	CMX0N[3:0]	**Comparator0 Negative Input MUX Selection.**		
			20-Pin and 24-Pin Devices	**16-Pin Devices**
		0000	P0.1	P0.1
		0001	P0.3	P0.3
		0010	P0.5	P0.5
		0011	P0.7	P0.7
		0100	P1.1	P1.1
		0101	P1.3	P1.3
		0110	P1.5	Reserved.
		0111	P1.7	Reserved.
		1000	VREG Output.	VREG Output.
		1001–1111	No input selected.	No input selected.
3:0	CMX0P[3:0]	**Comparator0 Positive Input MUX Selection.**		
			20-Pin and 24-Pin Devices	**16-Pin Devices**
		0000	P0.0	P0.0
		0001	P0.2	P0.2
		0010	P0.4	P0.4
		0011	P0.6	P0.6
		0100	P1.0	P1.0
		0101	P1.2	P1.2
		0110	P1.4	Reserved.
		0111	P1.6	Reserved.
		1000	VREG Output.	VREG Output.
		1001–1111	No input selected.	No input selected.

13.1. Configuring Port Pins as Capacitive Sense Inputs

In order for a port pin to be measured by CS0, that port pin must be configured as an analog input (see “23. Port Input/Output”). Configuring the input multiplexer to a port pin not configured as an analog input will cause the capacitive sense comparator to output incorrect measurements.

13.2. Capacitive Sense Start-Of-Conversion Sources

A capacitive sense conversion can be initiated in one of seven ways, depending on the programmed state of the CS0 start of conversion bits (CS0CF6:4). Conversions may be initiated by one of the following:

1. Writing a 1 to the CS0BUSY bit of register CS0CN
2. Timer 0 overflow
3. Timer 2 overflow
4. Timer 1 overflow
5. Convert continuously
6. Convert continuously with auto-scan enabled

Conversions can be configured to be initiated continuously through one of two methods. CS0 can be configured to convert at a single channel continuously or it can be configured to convert continuously with auto-scan enabled. When configured to convert continuously, conversions will begin after the CS0BUSY bit in CS0CF has been set.

An interrupt will be generated if CS0 conversion complete interrupts are enabled by setting the ECSCPT bit (EIE2.0).

Note: CS0 conversion complete interrupt behavior depends on the settings of the CS0 accumulator. If CS0 is configured to accumulate multiple conversions on an input channel, a CS0 conversion complete interrupt will be generated only after the last conversion completes.

13.3. Automatic Scanning

CS0 can be configured to automatically scan a sequence of contiguous CS0 input channels by configuring and enabling auto-scan. Using auto-scan with the CS0 comparator interrupt enabled allows a system to detect a change in measured capacitance without requiring any additional dedicated MCU resources.

Auto-scan is enabled by setting the CS0 start-of-conversion bits (CS0CF6:4) to 111b. After enabling auto-scan, the starting and ending channels should be set to appropriate values in CS0SS and CS0SE, respectively. Writing to CS0SS when auto-scan is enabled will cause the value written to CS0SS to be copied into CS0MX. After being enabled, writing a 1 to CS0BUSY will start auto-scan conversions. When auto-scan completes the number of conversions defined in the CS0 accumulator bits (CS0CF1:0) (see “13.5. CS0 Conversion Accumulator”), auto-scan configures CS0MX to the next highest port pin configured as an analog input and begins a conversion on that channel. This scan sequence continues until CS0MX reaches the ending input channel value defined in CS0SE. After one or more conversions have been taken at this channel, auto-scan configures CS0MX back to the starting input channel. For an example system configured to use auto-scan, please see Figure “13.2 Auto-Scan Example” on page 73.

Note: Auto-scan attempts one conversion on a CS0MX channel regardless of whether that channel’s port pin has been configured as an analog input.

If auto-scan is enabled when the device enters suspend mode, auto-scan will remain enabled and running. This feature allows the device to wake from suspend through CS0 greater-than comparator event on any configured capacitive sense input included in the auto-scan sequence of inputs.

SFR Definition 16.2. DERIVID: Derivative Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	DERIVID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xAD

Bit	Name	Description
7:0	DERIVID[7:0]	**Derivative Identification Byte.** Shows the C8051F80x-83x derivative being used. 0xD0: C8051F800; 0xD1: C8051F801; 0xD2: C8051F802; 0xD3: C8051F803 0xD4: C8051F804; 0xD5: C8051F805; 0xD6: C8051F806; 0xD7: C8051F807 0xD8: C8051F808; 0xD9: C8051F809; 0xDA: C8051F810; 0xDB: C8051F811 0xDC: C8051F812; 0xDD: C8051F813; 0xDE: C8051F814; 0xDF: C8051F815 0xE0: C8051F816; 0xE1: C8051F817; 0xE2: C8051F818; 0xE3: C8051F819 0xE4: C8051F820; 0xE5: C8051F821; 0xE6: C8051F822; 0xE7: C8051F823 0xE8: C8051F824; 0xE9: C8051F825; 0xEA: C8051F826; 0xEB: C8051F827 0xEC: C8051F828; 0xED: C8051F829; 0xEE: C8051F830; 0xEF: C8051F831 0xF0: C8051F832; 0xF1: C8051F833; 0xF2: C8051F834; 0xF3: C8051F835

SFR Definition 16.3. REVID: Hardware Revision Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R	R	R	R	R	R	R	R
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xB6

Bit	Name	Description
7:0	REVID[7:0]	**Hardware Revision Identification Byte.** Shows the C8051F80x-83x hardware revision being used. For example, 0x00 = Revision A.

SFR Definition 18.6. EIP2: Extended Interrupt Priority 2

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PSCGRT	PSCCPT
Type	R	R	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF4

Bit	Name	Function
7:2	Reserved	
1	PSCGRT	**Capacitive Sense Greater Than Comparator Priority Control.** This bit sets the priority of the Capacitive Sense Greater Than Comparator interrupt. 0: CS0 Greater Than Comparator interrupt set to low priority level. 1: CS0 Greater Than Comparator set to high priority level.
0	PSCCPT	**Capacitive Sense Conversion Complete Priority Control.** This bit sets the priority of the Capacitive Sense Conversion Complete interrupt. 0: CS0 Conversion Complete set to low priority level. 1: CS0 Conversion Complete set to high priority level.

21. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source. Program execution begins at location 0x0000.

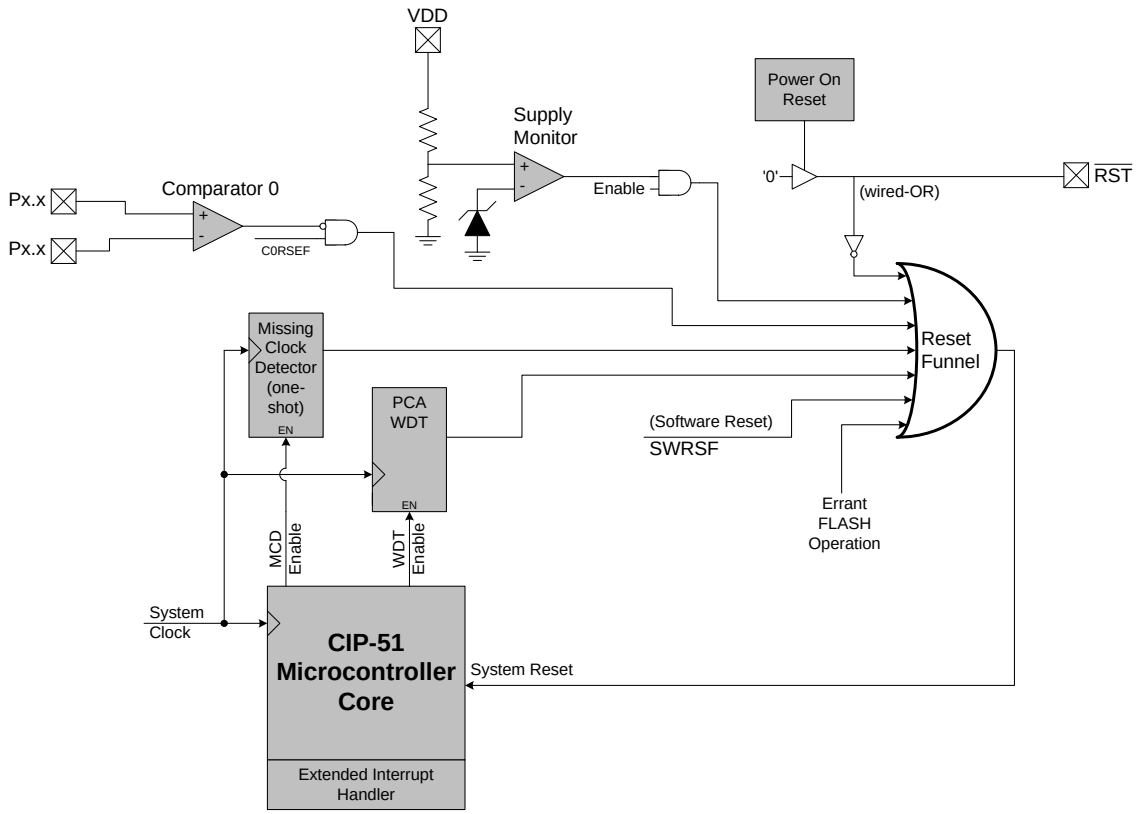

Figure 21.1. Reset Sources

SFR Definition 21.2. RSTSRC: Reset Source

Bit	7	6	5	4	3	2	1	0
Name		FERROR	C0RSEF	SWRSF	WDTRSF	MCDRSF	PORSF	PINRSF
Type	R	R	R/W	R/W	R	R/W	R/W	R
Reset	0	Varies	Varies	Varies	Varies	Varies	Varies	Varies

SFR Address = 0xEF

Bit	Name	Description	Write	Read
7	Unused	**Unused.**	Don't care.	0
6	FERROR	**Flash Error Reset Flag.**	N/A	Set to 1 if Flash read/write/erase error caused the last reset.
5	C0RSEF	**Comparator0 Reset Enable and Flag.**	Writing a 1 enables Comparator0 as a reset source (active-low).	Set to 1 if Comparator0 caused the last reset.
4	SWRSF	**Software Reset Force and Flag.**	Writing a 1 forces a system reset.	Set to 1 if last reset was caused by a write to SWRSF.
3	WDTRSF	**Watchdog Timer Reset Flag.**	N/A	Set to 1 if Watchdog Timer overflow caused the last reset.
2	MCDRSF	**Missing Clock Detector Enable and Flag.**	Writing a 1 enables the Missing Clock Detector. The MCD triggers a reset if a missing clock condition is detected.	Set to 1 if Missing Clock Detector timeout caused the last reset.
1	PORSF	**Power-On / V_{DD} Monitor Reset Flag, and V_{DD} monitor Reset Enable.**	Writing a 1 enables the V_{DD} monitor as a reset source. **Writing 1 to this bit before the V_{DD} monitor is enabled and stabilized may cause a system reset.**	Set to 1 anytime a power-on or V_{DD} monitor reset occurs. **When set to 1 all other RSTSRC flags are indeterminate.**
0	PINRSF	**HW Pin Reset Flag.**	N/A	Set to 1 if $\overline{\text{RST}}$ pin caused the last reset.

Note: Do not use read-modify-write operations on this register

23.4. Port I/O Initialization

Port I/O initialization consists of the following steps:

1. Select the input mode (analog or digital) for all Port pins, using the Port Input Mode register (PnMDIN). **If the pin is in analog mode, a '1' must also be written to the corresponding Port Latch (Pn)**.
2. Select the output mode (open-drain or push-pull) for all Port pins, using the Port Output Mode register (PnMDOUT).
3. Select any pins to be skipped by the I/O Crossbar using the Port Skip registers (PnSKIP).
4. Assign Port pins to desired peripherals (XBR0, XBR1).
5. Enable the Crossbar (XBARE = 1).

All Port pins must be configured as either analog or digital inputs. When a pin is configured as an analog input, its weak pullup, digital driver, and digital receiver are disabled. This process saves power and reduces noise on the analog input. Pins configured as digital inputs may still be used by analog peripherals; however this practice is not recommended.

Additionally, all analog input pins should be configured to be skipped by the Crossbar (accomplished by setting the associated bits in PnSKIP). Port input mode is set in the PnMDIN register, where a 1 indicates a digital input, and a 0 indicates an analog input. All port pins in analog mode must have a '1' set in the corresponding Port Latch register. All pins default to digital inputs on reset. See SFR Definition 23.8 and SFR Definition 23.12 for the PnMDIN register details.

The output driver characteristics of the I/O pins are defined using the Port Output Mode registers (PnMDOUT). Each Port Output driver can be configured as either open drain or push-pull. This selection is required even for the digital resources selected in the XBRn registers, and is not automatic. The only exception to this is the SMBus (SDA, SCL) pins, which are configured as open-drain regardless of the PnMDOUT settings. When the WEAKPUD bit in XBR1 is 0, a weak pullup is enabled for all Port I/O configured as open-drain. WEAKPUD does not affect the push-pull Port I/O. Furthermore, the weak pullup is turned off on an output that is driving a 0 to avoid unnecessary power dissipation.

Registers XBR0 and XBR1 must be loaded with the appropriate values to select the digital I/O functions required by the design. Setting the XBARE bit in XBR1 to 1 enables the Crossbar. Until the Crossbar is enabled, the external pins remain as standard Port I/O (in input mode), regardless of the XBRn Register settings. For given XBRn Register settings, one can determine the I/O pin-out using the Priority Decode Table; as an alternative, the Configuration Wizard utility will determine the Port I/O pin-assignments based on the XBRn Register settings.

The Crossbar must be enabled to use Port pins as standard Port I/O in output mode. Port output drivers are disabled while the Crossbar is disabled.

SFR Definition 23.3. P0MASK: Port 0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFE

Bit	Name	Function
7:0	P0MASK[7:0]	**Port 0 Mask Value.** Selects P0 pins to be compared to the corresponding bits in P0MAT. 0: P0.n pin logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin logic value is compared to P0MAT.n.

SFR Definition 23.4. P0MAT: Port 0 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P0MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xFD

Bit	Name	Function
7:0	P0MAT[7:0]	**Port 0 Match Value.** Match comparison value used on Port 0 for bits in P0MASK which are set to 1. 0: P0.n pin logic value is compared with logic LOW. 1: P0.n pin logic value is compared with logic HIGH.

is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 25.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 25.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 25.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.

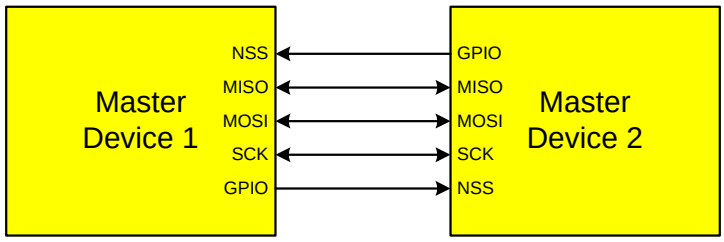

Figure 25.2. Multiple-Master Mode Connection Diagram

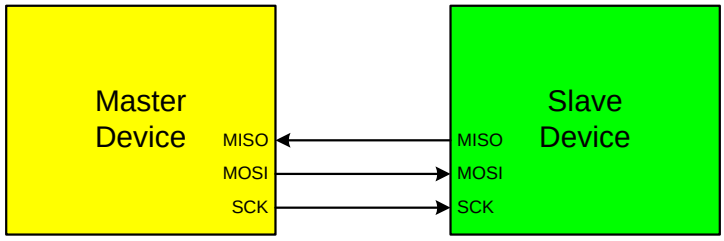

Figure 25.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

SFR Definition 28.9. TMR2RLL: Timer 2 Reload Register Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCA

Bit	Name	Function
7:0	TMR2RLL[7:0]	**Timer 2 Reload Register Low Byte.** TMR2RLL holds the low byte of the reload value for Timer 2.

SFR Definition 28.10. TMR2RLH: Timer 2 Reload Register High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR2RLH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCB

Bit	Name	Function
7:0	TMR2RLH[7:0]	**Timer 2 Reload Register High Byte.** TMR2RLH holds the high byte of the reload value for Timer 2.

C2 Register Definition 30.2. DEVICEID: C2 Device ID

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID[7:0]							
Type	R/W							
Reset	1	1	1	0	0	0	0	1

C2 Address: 0x00

Bit	Name	Function
7:0	DEVICEID[7:0]	**Device ID.** This read-only register returns the 8-bit device ID: 0x23 (C8051F80x-83x).

C2 Register Definition 30.3. REVID: C2 Revision ID

Bit	7	6	5	4	3	2	1	0
Name	REVID[7:0]							
Type	R/W							
Reset	Varies	Varies	Varies	Varies	Varies	Varies	Varies	Varies

C2 Address: 0x01

Bit	Name	Function
7:0	REVID[7:0]	**Revision ID.** This read-only register returns the 8-bit revision ID. For example: 0x00 = Revision A.