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Details

Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f818-gu

C8051F80x-83x

Table 2.1. Product Selection Guide

Part Number	Digital Port I/Os	Capacitive Sense Channels	Flash Memory (kB)	RAM (Bytes)	10-bit 500 ksps ADC	ADC Channels	Temperature Sensor	Package (RoHS)
C8051F800-GU	17	16	16	512	✓	16	✓	QSOP-24
C8051F801-GU	17	8	16	512	✓	16	✓	QSOP-24
C8051F802-GU	17	—	16	512	✓	16	✓	QSOP-24
C8051F800-GM	17	16	16	512	✓	16	✓	QFN-20
C8051F801-GM	17	8	16	512	✓	16	✓	QFN-20
C8051F802-GM	17	—	16	512	✓	16	✓	QFN-20
C8051F803-GS	13	12	16	512	✓	12	✓	SOIC-16
C8051F804-GS	13	8	16	512	✓	12	✓	SOIC-16
C8051F805-GS	13	—	16	512	✓	12	✓	SOIC-16
C8051F806-GU	17	16	16	512	—	—	—	QSOP-24
C8051F807-GU	17	8	16	512	—	—	—	QSOP-24
C8051F808-GU	17	—	16	512	—	—	—	QSOP-24
C8051F806-GM	17	16	16	512	—	—	—	QFN-20
C8051F807-GM	17	8	16	512	—	—	—	QFN-20
C8051F808-GM	17	—	16	512	—	—	—	QFN-20
C8051F809-GS	13	12	16	512	—	—	—	SOIC-16
C8051F810-GS	13	8	16	512	—	—	—	SOIC-16
C8051F811-GS	13	—	16	512	—	—	—	SOIC-16
C8051F812-GU	17	16	8	512	✓	16	✓	QSOP-24
C8051F813-GU	17	8	8	512	✓	16	✓	QSOP-24
C8051F814-GU	17	—	8	512	✓	16	✓	QSOP-24
C8051F812-GM	17	16	8	512	✓	16	✓	QFN-20
C8051F813-GM	17	8	8	512	✓	16	✓	QFN-20
C8051F814-GM	17	—	8	512	✓	16	✓	QFN-20
C8051F815-GS	13	12	8	512	✓	12	✓	SOIC-16
C8051F816-GS	13	8	8	512	✓	12	✓	SOIC-16
C8051F817-GS	13	—	8	512	✓	12	✓	SOIC-16
C8051F818-GU	17	16	8	512	—	—	—	QSOP-24
C8051F819-GU	17	8	8	512	—	—	—	QSOP-24
C8051F820-GU	17	—	8	512	—	—	—	QSOP-24
C8051F818-GM	17	16	8	512	—	—	—	QFN-20
C8051F819-GM	17	8	8	512	—	—	—	QFN-20
C8051F820-GM	17	—	8	512	—	—	—	QFN-20

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Table 3.1. Pin Definitions for the C8051F80x-83x (Continued)

Name	Pin QSOP-24	Pin QFN-20	Pin SOIC-16	Type	Description
P0.5	21	16	14	D I/O or A In	Port 0.5.
P0.6/ CNVSTR	20	15	13	D I/O or A In D In	Port 0.6. ADC0 External Convert Start or IDA0 Update Source Input.
P0.7	19	14	12	D I/O or A In	Port 0.7.
P1.0	18	13	11	D I/O or A In	Port 1.0.
P1.1	17	12	10	D I/O or A In	Port 1.1.
P1.2	16	11	9	D I/O or A In	Port 1.2.
P1.3	15	10	8	D I/O or A In	Port 1.3.
P1.4	14	9		D I/O or A In	Port 1.4.
P1.5	11	8		D I/O or A In	Port 1.5.
P1.6	10	7		D I/O or A In	Port 1.6.
P1.7	9	6		D I/O or A In	Port 1.7.
NC	1, 12, 13, 24				No Connection.

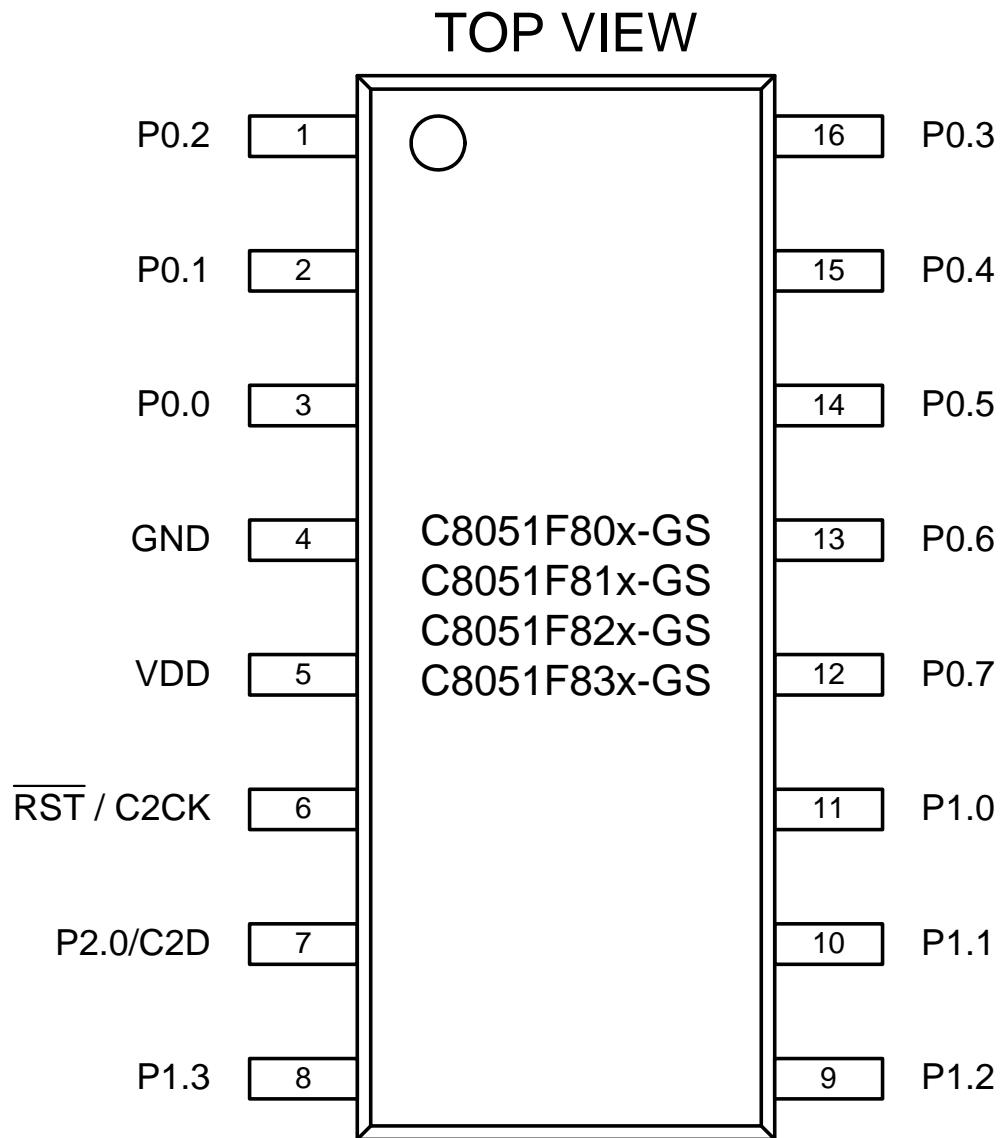


Figure 3.3. SOIC-16 Pinout Diagram (Top View)

Table 7.9. ADC0 Electrical Characteristics

$V_{DD} = 3.0\text{ V}$, $V_{REF} = 2.40\text{ V}$ (REFSL=0), -40 to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution		10			bits
Integral Nonlinearity		—	± 0.5	± 1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	± 0.5	± 1	LSB
Offset Error		−2	0	2	LSB
Full Scale Error		−2	0	2	LSB
Offset Temperature Coefficient		—	45	—	ppm/ $^{\circ}\text{C}$
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, 200 ksps)					
Signal-to-Noise Plus Distortion		54	60	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	75	—	dB
Spurious-Free Dynamic Range		—	−90	—	dB
Conversion Rate					
SAR Conversion Clock		—	—	8.33	MHz
Conversion Time in SAR Clocks	10-bit Mode	13	—	—	clocks
	8-bit Mode	11	—	—	clocks
Track/Hold Acquisition Time	$V_{DD} \geq 2.0\text{ V}$	300	—	—	ns
	$V_{DD} < 2.0\text{ V}$	2.0	—	—	μs
Throughput Rate		—	—	500	ksps
Analog Inputs					
ADC Input Voltage Range		0	—	V_{REF}	V
Sampling Capacitance	1x Gain	—	5	—	pF
	0.5x Gain	—	3	—	pF
Input Multiplexer Impedance		—	5	—	k Ω
Power Specifications					
Power Supply Current	Operating Mode, 500 ksps	—	630	1000	μA
Power Supply Rejection		—	−70	—	dB

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8.4. Programmable Window Detector

The ADC Programmable Window Detector continuously compares the ADC0 output registers to user-programmed limits, and notifies the system when a desired condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in register ADC0CN) can also be used in polled mode. The ADC0 Greater-Than (ADC0GTH, ADC0GTL) and Less-Than (ADC0LTH, ADC0LTL) registers hold the comparison values. The window detector flag can be programmed to indicate when measured data is inside or outside of the user-programmed limits, depending on the contents of the ADC0 Less-Than and ADC0 Greater-Than registers.

SFR Definition 8.5. ADC0GTH: ADC0 Greater-Than Data High Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTH[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC4

Bit	Name	Function
7:0	ADC0GTH[7:0]	ADC0 Greater-Than Data Word High-Order Bits.

SFR Definition 8.6. ADC0GTL: ADC0 Greater-Than Data Low Byte

Bit	7	6	5	4	3	2	1	0
Name	ADC0GTL[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xC3

Bit	Name	Function
7:0	ADC0GTL[7:0]	ADC0 Greater-Than Data Word Low-Order Bits.

8.5. ADC0 Analog Multiplexer

ADC0 on the C8051F800/1/2/3/4/5, C8051F812/3/4/5/6/7, C8051F824/5/6, and C8051F830/1/2 uses an analog input multiplexer to select the positive input to the ADC. Any of the following may be selected as the positive input: Port 0 or Port 1 I/O pins, the on-chip temperature sensor, or the positive power supply (V_{DD}). The ADC0 input channel is selected in the ADC0MX register described in SFR Definition 8.9.

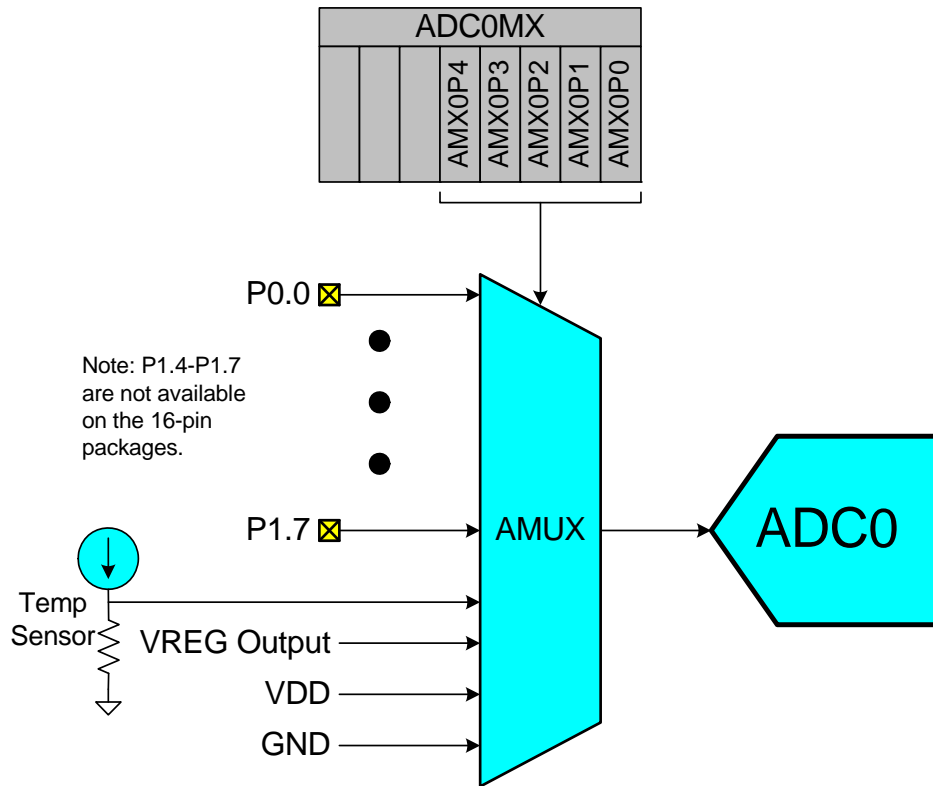


Figure 8.6. ADC0 Multiplexer Block Diagram

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set the corresponding bit in register PnMDIN to 0. To force the Crossbar to skip a Port pin, set the corresponding bit in register PnSKIP to 1. See Section “23. Port Input/Output” on page 138 for more Port I/O configuration details.

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SFR Definition 11.1. REG0CN: Voltage Regulator Control

Bit	7	6	5	4	3	2	1	0
Name	STOPCF							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC9

Bit	Name	Function
7	STOPCF	Stop Mode Configuration. This bit configures the regulator's behavior when the device enters STOP mode. 0: Regulator is still active in STOP mode. Any enabled reset source will reset the device. 1: Regulator is shut down in STOP mode. Only the $\overline{\text{RST}}$ pin or power cycle can reset the device.
6:0	Reserved	Must write to 0000000b.

14.2. CIP-51 Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should always be written to the value indicated in the SFR description. Future product versions may use these bits to implement new features in which case the reset value of the bit will be the indicated value, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the data sheet associated with their corresponding system function.

SFR Definition 14.1. DPL: Data Pointer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	DPL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x82

Bit	Name	Function
7:0	DPL[7:0]	Data Pointer Low. The DPL register is the low byte of the 16-bit DPTR.

SFR Definition 14.2. DPH: Data Pointer High Byte

Bit	7	6	5	4	3	2	1	0
Name	DPH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x83

Bit	Name	Function
7:0	DPH[7:0]	Data Pointer High. The DPH register is the high byte of the 16-bit DPTR.

Table 17.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
P1MAT	0xED	P1 Match	152
P1MDIN	0xF2	Port 1 Input Mode Configuration	156
P1MDOUT	0xA5	Port 1 Output Mode Configuration	156
P1SKIP	0xD5	Port 1 Skip	157
P2	0xA0	Port 2 Latch	157
P2MDOUT	0xA6	Port 2 Output Mode Configuration	158
PCA0CN	0xD8	PCA Control	238
PCA0CPH0	0xFC	PCA Capture 0 High	243
PCA0CPH1	0xEA	PCA Capture 1 High	243
PCA0CPH2	0xEC	PCA Capture 2 High	243
PCA0CPL0	0xFB	PCA Capture 0 Low	243
PCA0CPL1	0xE9	PCA Capture 1 Low	243
PCA0CPL2	0xEB	PCA Capture 2 Low	243
PCA0CPM0	0xDA	PCA Module 0 Mode Register	241
PCA0CPM1	0xDB	PCA Module 1 Mode Register	241
PCA0CPM2	0xDC	PCA Module 2 Mode Register	241
PCA0H	0xFA	PCA Counter High	242
PCA0L	0xF9	PCA Counter Low	242
PCA0MD	0xD9	PCA Mode	239
PCA0PWM	0xF7	PCA PWM Configuration	240
PCON	0x87	Power Control	122
PSCTL	0x8F	Program Store R/W Control	118
PSW	0xD0	Program Status Word	91
REF0CN	0xD1	Voltage Reference Control	62
REG0CN	0xC9	Voltage Regulator Control	64
REVID	0xB6	Revision ID	96
RSTSRC	0xEF	Reset Source Configuration/Status	128

21.2. Power-Fail Reset / V_{DD} Monitor

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST} , the power supply monitor will drive the \overline{RST} pin low and hold the CIP-51 in a reset state (see Figure 21.2). When V_{DD} returns to a level above V_{RST} , the CIP-51 will be released from the reset state. Even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag reads 1, the data may no longer be valid. The V_{DD} monitor is enabled and selected as a reset source after power-on resets. Its defined state (enabled/disabled) is not altered by any other reset source. For example, if the V_{DD} monitor is disabled by code and a software reset is performed, the V_{DD} monitor will still be disabled after the reset.

Important Note: If the V_{DD} monitor is being turned on from a disabled state, it should be enabled before it is selected as a reset source. Selecting the V_{DD} monitor as a reset source before it is enabled and stabilized may cause a system reset. In some applications, this reset may be undesirable. If this is not desirable in the application, a delay should be introduced between enabling the monitor and selecting it as a reset source. The procedure for enabling the V_{DD} monitor and configuring it as a reset source from a disabled state is shown below:

1. Enable the V_{DD} monitor (VDMEN bit in VDM0CN = 1).
2. If necessary, wait for the V_{DD} monitor to stabilize.
3. Select the V_{DD} monitor as a reset source (PORSF bit in RSTSRC = 1).

See Figure 21.2 for V_{DD} monitor timing; note that the power-on-reset delay is not incurred after a V_{DD} monitor reset. See Section “7. Electrical Characteristics” on page 39 for complete electrical characteristics of the V_{DD} monitor.

24.3. Preparing for a CRC Calculation

To prepare CRC0 for a CRC calculation, software should select the desired polynomial and set the initial value of the result. Two polynomials are available: 0x1021 (16-bit) and 0x04C11DB7 (32-bit). The CRC0 result may be initialized to one of two values: 0x00000000 or 0xFFFFFFFF. The following steps can be used to initialize CRC0.

1. Select a polynomial (Set CRC0SEL to 0 for 32-bit or 1 for 16-bit).
2. Select the initial result value (Set CRC0VAL to 0 for 0x00000000 or 1 for 0xFFFFFFFF).
3. Set the result to its initial value (Write 1 to CRC0INIT).

24.4. Performing a CRC Calculation

Once CRC0 is initialized, the input data stream is sequentially written to CRC0IN, one byte at a time. The CRC0 result is automatically updated after each byte is written. The CRC engine may also be configured to automatically perform a CRC on one or more Flash sectors. The following steps can be used to automatically perform a CRC on Flash memory.

1. Prepare CRC0 for a CRC calculation as shown above.
2. Write the index of the starting page to CRC0AUTO.
3. Set the AUTOEN bit in CRC0AUTO.
4. Write the number of Flash sectors to perform in the CRC calculation to CRC0CNT.

Note: Each Flash sector is 512 bytes.

5. Write any value to CRC0CN (or OR its contents with 0x00) to initiate the CRC calculation. The CPU will not execute code any additional code until the CRC operation completes.
6. Clear the AUTOEN bit in CRC0AUTO.
7. Read the CRC result using the procedure below.

24.5. Accessing the CRC0 Result

The internal CRC0 result is 32-bits (CRC0SEL = 0b) or 16-bits (CRC0SEL = 1b). The CRC0PNT bits select the byte that is targeted by read and write operations on CRC0DAT and increment after each read or write. The calculation result will remain in the internal CR0 result register until it is set, overwritten, or additional data is written to CRC0IN.

SFR Definition 24.1. CRC0CN: CRC0 Control

Bit	7	6	5	4	3	2	1	0
Name				CRC0SEL	CRC0INIT	CRC0VAL	CRC0PNT[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xCE

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care.
4	CRC0SEL	CRC0 Polynomial Select Bit. This bit selects the CRC0 polynomial and result length (32-bit or 16-bit). 0: CRC0 uses the 32-bit polynomial 0x04C11DB7 for calculating the CRC result. 1: CRC0 uses the 16-bit polynomial 0x1021 for calculating the CRC result.
3	CRC0INIT	CRC0 Result Initialization Bit. Writing a 1 to this bit initializes the entire CRC result based on CRC0VAL.
2	CRC0VAL	CRC0 Set Value Initialization Bit. This bit selects the set value of the CRC result. 0: CRC result is set to 0x00000000 on write of 1 to CRC0INIT. 1: CRC result is set to 0xFFFFFFFF on write of 1 to CRC0INIT.
1:0	CRC0PNT[1:0]	CRC0 Result Pointer. Specifies the byte of the CRC result to be read/written on the next access to CRC0DAT. The value of these bits will auto-increment upon each read or write. For CRC0SEL = 0: 00: CRC0DAT accesses bits 7–0 of the 32-bit CRC result. 01: CRC0DAT accesses bits 15–8 of the 32-bit CRC result. 10: CRC0DAT accesses bits 23–16 of the 32-bit CRC result. 11: CRC0DAT accesses bits 31–24 of the 32-bit CRC result. For CRC0SEL = 1: 00: CRC0DAT accesses bits 7–0 of the 16-bit CRC result. 01: CRC0DAT accesses bits 15–8 of the 16-bit CRC result. 10: CRC0DAT accesses bits 7–0 of the 16-bit CRC result. 11: CRC0DAT accesses bits 15–8 of the 16-bit CRC result.

25.4. SPI0 Interrupt Sources

When SPI0 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

All of the following bits must be cleared by software.

- The SPI Interrupt Flag, SPIF (SPI0CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI0 modes.
- The Write Collision Flag, WCOL (SPI0CN.6) is set to logic 1 if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written. This flag can occur in all SPI0 modes.
- The Mode Fault Flag MODF (SPI0CN.5) is set to logic 1 when SPI0 is configured as a master, and for multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI0CN are set to logic 0 to disable SPI0 and allow another master device to access the bus.
- The Receive Overrun Flag RXOVRN (SPI0CN.4) is set to logic 1 when configured as a slave, and a transfer is completed and the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.

25.5. Serial Clock Phase and Polarity

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 25.5. For slave mode, the clock and data relationships are shown in Figure 25.6 and Figure 25.7. Note that CKPHA should be set to 0 on both the master and slave SPI when communicating between two Silicon Labs C8051 devices.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 25.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

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SFR Definition 28.1. CKCON: Clock Control

Bit	7	6	5	4	3	2	1	0
Name			T2MH	T2ML	T1M	T0M	SCA[1:0]	
Type	R	R	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8E

Bit	Name	Function
7:6	Unused	Read = 0b; Write = Don't care
5	T2MH	Timer 2 High Byte Clock Select. Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only). 0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 high byte uses the system clock.
4	T2ML	Timer 2 Low Byte Clock Select. Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer. 0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 low byte uses the system clock.
3	T1	Timer 1 Clock Select. Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1. 0: Timer 1 uses the clock defined by the prescale bits SCA[1:0]. 1: Timer 1 uses the system clock.
2	T0	Timer 0 Clock Select. Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1. 0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0]. 1: Counter/Timer 0 uses the system clock.
1:0	SCA[1:0]	Timer 0/1 Prescale Bits. These bits control the Timer 0/1 Clock Prescaler: 00: System clock divided by 12 01: System clock divided by 4 10: System clock divided by 48 11: External clock divided by 8 (synchronized with the system clock)

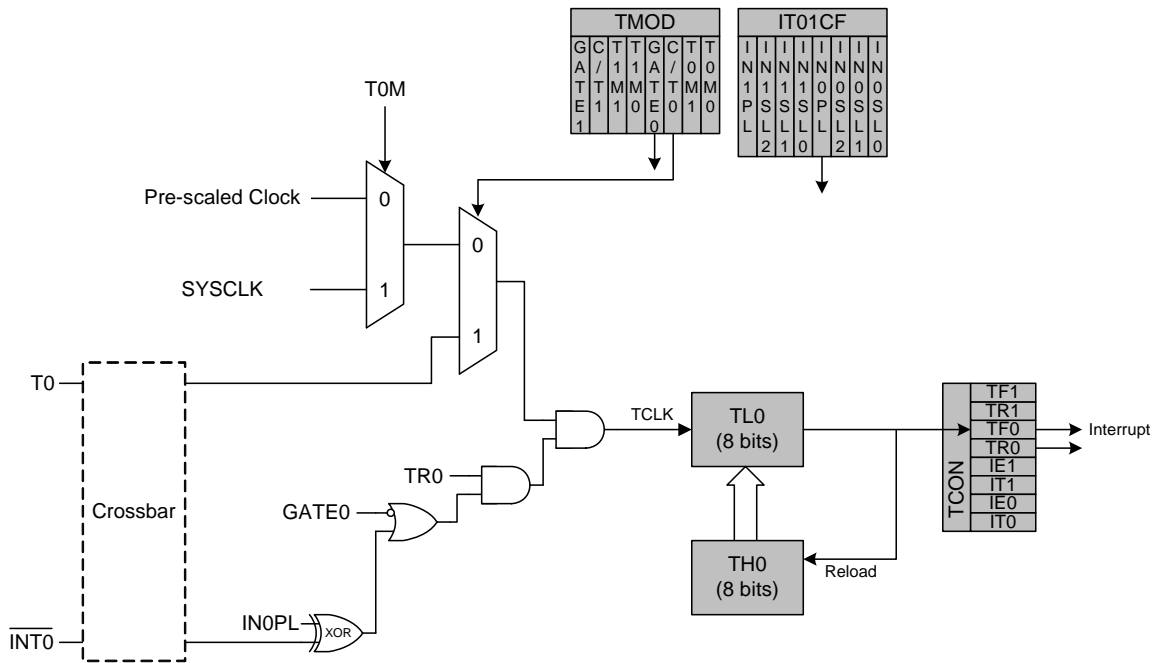


Figure 28.2. T0 Mode 2 Block Diagram

28.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock or prescaled clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3. When Timer 0 is operating in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used to generate baud rates or overflow conditions for other peripherals. While Timer 0 is operating in Mode 3, Timer 1 run control is handled through its mode settings. To run Timer 1 while Timer 0 is in Mode 3, set the Timer 1 Mode as 0, 1, or 2. To disable Timer 1, configure it for Mode 3.

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SFR Definition 28.3. TMOD: Timer Mode

Bit	7	6	5	4	3	2	1	0
Name	GATE1	C/T1	T1M[1:0]		GATE0	C/T0	T0M[1:0]	
Type	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x89

Bit	Name	Function
7	GATE1	Timer 1 Gate Control. 0: Timer 1 enabled when TR1 = 1 irrespective of $\overline{\text{INT1}}$ logic level. 1: Timer 1 enabled only when TR1 = 1 AND $\overline{\text{INT1}}$ is active as defined by bit IN1PL in register IT01CF (see SFR Definition 18.7).
6	C/T1	Counter/Timer 1 Select. 0: Timer: Timer 1 incremented by clock defined by T1M bit in register CKCON. 1: Counter: Timer 1 incremented by high-to-low transitions on external pin (T1).
5:4	T1M[1:0]	Timer 1 Mode Select. These bits select the Timer 1 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Timer 1 Inactive
3	GATE0	Timer 0 Gate Control. 0: Timer 0 enabled when TR0 = 1 irrespective of $\overline{\text{INT0}}$ logic level. 1: Timer 0 enabled only when TR0 = 1 AND $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 18.7).
2	C/T0	Counter/Timer 0 Select. 0: Timer: Timer 0 incremented by clock defined by T0M bit in register CKCON. 1: Counter: Timer 0 incremented by high-to-low transitions on external pin (T0).
1:0	T0M[1:0]	Timer 0 Mode Select. These bits select the Timer 0 operation mode. 00: Mode 0, 13-bit Counter/Timer 01: Mode 1, 16-bit Counter/Timer 10: Mode 2, 8-bit Counter/Timer with Auto-Reload 11: Mode 3, Two 8-bit Counter/Timers

28.2.3. Comparator 0 Capture Mode

The capture mode in Timer 2 allows Comparator 0 rising edges to be captured with the timer clocking from the system clock or the system clock divided by 12. Timer 2 capture mode is enabled by setting TF2CEN to 1 and T2SPLIT to 0.

When capture mode is enabled, a capture event will be generated on every Comparator 0 rising edge. When the capture event occurs, the contents of Timer 2 (TMR2H:TMR2L) are loaded into the Timer 2 reload registers (TMR2RLH:TMR2RLL) and the TF2H flag is set (triggering an interrupt if Timer 2 interrupts are enabled). By recording the difference between two successive timer capture values, the Comparator 0 period can be determined with respect to the Timer 2 clock. The Timer 2 clock should be much faster than the capture clock to achieve an accurate reading.

This mode allows software to determine the time between consecutive Comparator 0 rising edges, which can be used for detecting changes in the capacitance of a capacitive switch, or measuring the frequency of a low-level analog signal.

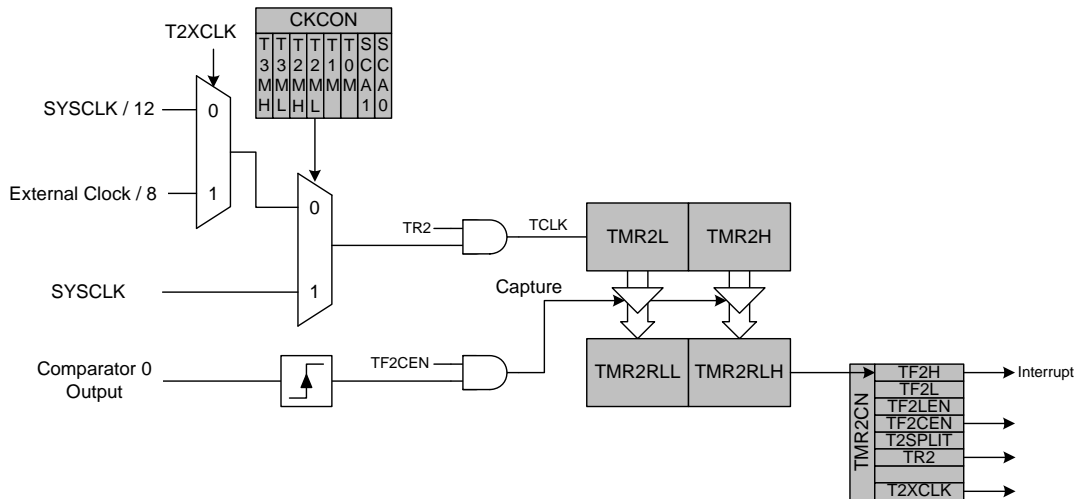


Figure 28.6. Timer 2 Capture Mode Block Diagram

29.3.5.1. 8-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 8-bit PWM mode is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 29.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. This synchronous update feature allows software to asynchronously write a new PWM high time, which will then take effect on the following PWM period.

Setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to 000b enables 8-Bit Pulse Width Modulator mode. If the MATn bit is set to 1, the CCFn flag for the module will be set each time an 8-bit comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 256 PCA clock cycles. The duty cycle for 8-Bit PWM Mode is given in Equation 29.2.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(256 - \text{PCA0CPHn})}{256}$$

Equation 29.2. 8-Bit PWM Duty Cycle

Using Equation 29.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

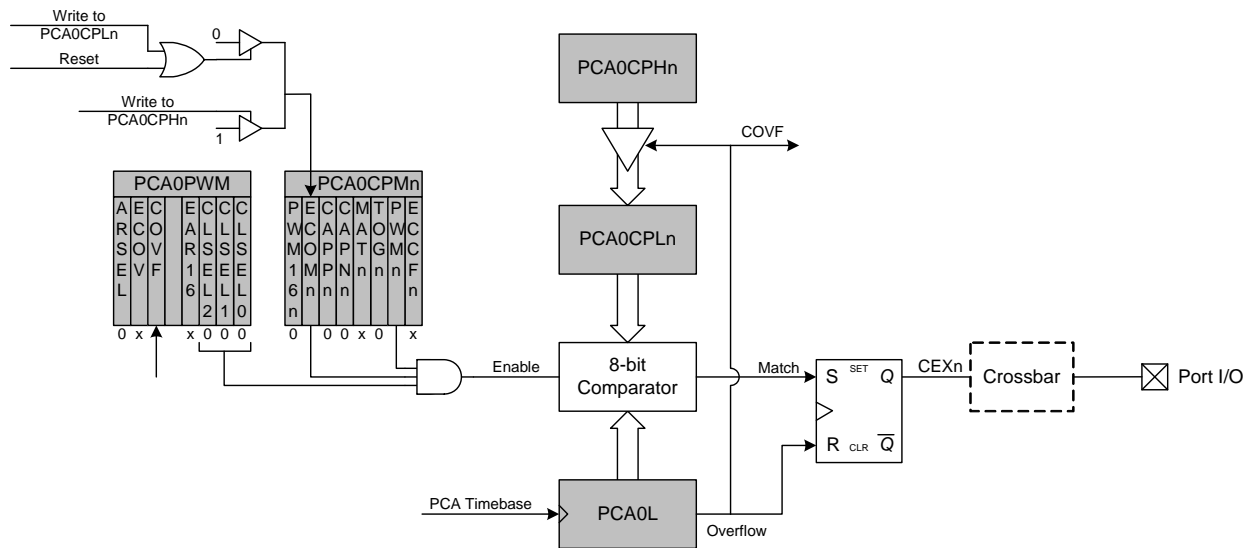


Figure 29.8. PCA 8-Bit PWM Mode Diagram

C8051F80x-83x

SFR Definition 29.5. PCA0L: PCA0 Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF9

Bit	Name	Function
7:0	PCA0[7:0]	PCA Counter/Timer Low Byte. The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.
Note: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents of the PCA0L register, the Watchdog Timer must first be disabled.		

SFR Definition 29.6. PCA0H: PCA0 Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFA

Bit	Name	Function
7:0	PCA0[15:8]	PCA Counter/Timer High Byte. The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 29.1).
Note: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the contents of the PCA0H register, the Watchdog Timer must first be disabled.		