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Applications of "Embedded - Microcontrollers"

Details

Product Status	Last Time Buy
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Cap Sense, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.154", 3.90mm Width)
Supplier Device Package	24-QSOP
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f818-gur

C8051F80x-83x

26.4.4. Data Register	192
26.5. SMBus Transfer Modes.....	193
26.5.1. Write Sequence (Master)	193
26.5.2. Read Sequence (Master)	194
26.5.3. Write Sequence (Slave)	195
26.5.4. Read Sequence (Slave)	196
26.6. SMBus Status Decoding.....	196
27. UART0.....	201
27.1. Enhanced Baud Rate Generation.....	202
27.2. Operational Modes	203
27.2.1. 8-Bit UART	203
27.2.2. 9-Bit UART	204
27.3. Multiprocessor Communications	205
28. Timers	209
28.1. Timer 0 and Timer 1	211
28.1.1. Mode 0: 13-bit Counter/Timer	211
28.1.2. Mode 1: 16-bit Counter/Timer	212
28.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload.....	212
28.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only).....	213
28.2. Timer 2	219
28.2.1. 16-bit Timer with Auto-Reload.....	219
28.2.2. 8-bit Timers with Auto-Reload.....	220
29. Programmable Counter Array.....	225
29.1. PCA Counter/Timer	226
29.2. PCA0 Interrupt Sources.....	227
29.3. Capture/Compare Modules	228
29.3.1. Edge-Triggered Capture Mode	229
29.3.2. Software Timer (Compare) Mode.....	230
29.3.3. High-Speed Output Mode	231
29.3.4. Frequency Output Mode	232
29.3.5. 8-bit through 15-bit Pulse Width Modulator Modes	232
29.3.5.1. 8-bit Pulse Width Modulator Mode.....	233
29.3.5.2. 9-bit through 15-bit Pulse Width Modulator Mode	234
29.3.6. 16-Bit Pulse Width Modulator Mode.....	235
29.4. Watchdog Timer Mode	236
29.4.1. Watchdog Timer Operation	236
29.4.2. Watchdog Timer Usage	237
29.5. Register Descriptions for PCA0.....	237
30. C2 Interface	244
30.1. C2 Interface Registers.....	244
30.2. C2CK Pin Sharing	247
Document Change List.....	248
Contact Information.....	250

C8051F80x-83x

Table 18.1. Interrupt Summary	104
19. Flash Memory	
Table 19.1. Flash Security Summary	115
20. Power Management Modes	
21. Reset Sources	
22. Oscillators and Clock Selection	
23. Port Input/Output	
Table 23.1. Port I/O Assignment for Analog Functions	141
Table 23.2. Port I/O Assignment for Digital Functions	142
Table 23.3. Port I/O Assignment for External Digital Event Capture Functions	142
24. Cyclic Redundancy Check Unit (CRC0)	
Table 24.1. Example 16-bit CRC Outputs	160
Table 24.2. Example 32-bit CRC Outputs	161
25. Enhanced Serial Peripheral Interface (SPI0)	
Table 25.1. SPI Slave Timing Parameters	179
26. SMBus	
Table 26.1. SMBus Clock Source Selection	184
Table 26.2. Minimum SDA Setup and Hold Times	185
Table 26.3. Sources for Hardware Changes to SMB0CN	189
Table 26.4. Hardware Address Recognition Examples (EHACK = 1)	190
Table 26.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)	197
Table 26.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1)	199
27. UART0	
Table 27.1. Timer Settings for Standard Baud Rates Using The Internal 24.5 MHz Oscillator	208
Table 27.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator	208
28. Timers	
29. Programmable Counter Array	
Table 29.1. PCA Timebase Input Options	226
Table 29.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Mod- ules ^{1,2,3,4,5,6}	228
Table 29.3. Watchdog Timer Timeout Intervals1	237
30. C2 Interface	

C8051F80x-83x

SFR Definition 21.2. RSTSRC: Reset Source	128
SFR Definition 22.1. CLKSEL: Clock Select	130
SFR Definition 22.2. OSCICL: Internal H-F Oscillator Calibration	131
SFR Definition 22.3. OSCICN: Internal H-F Oscillator Control	132
SFR Definition 22.4. OSCXCN: External Oscillator Control	134
SFR Definition 23.1. XBR0: Port I/O Crossbar Register 0	148
SFR Definition 23.2. XBR1: Port I/O Crossbar Register 1	149
SFR Definition 23.3. P0MASK: Port 0 Mask Register	151
SFR Definition 23.4. P0MAT: Port 0 Match Register	151
SFR Definition 23.5. P1MASK: Port 1 Mask Register	152
SFR Definition 23.6. P1MAT: Port 1 Match Register	152
SFR Definition 23.7. P0: Port 0	153
SFR Definition 23.8. P0MDIN: Port 0 Input Mode	154
SFR Definition 23.9. P0MDOUT: Port 0 Output Mode	154
SFR Definition 23.10. P0SKIP: Port 0 Skip	155
SFR Definition 23.11. P1: Port 1	155
SFR Definition 23.12. P1MDIN: Port 1 Input Mode	156
SFR Definition 23.13. P1MDOUT: Port 1 Output Mode	156
SFR Definition 23.14. P1SKIP: Port 1 Skip	157
SFR Definition 23.15. P2: Port 2	157
SFR Definition 23.16. P2MDOUT: Port 2 Output Mode	158
SFR Definition 24.1. CRC0CN: CRC0 Control	163
SFR Definition 24.2. CRC0IN: CRC Data Input	164
SFR Definition 24.3. CRC0DATA: CRC Data Output	164
SFR Definition 24.4. CRC0AUTO: CRC Automatic Control	165
SFR Definition 24.5. CRC0CNT: CRC Automatic Flash Sector Count	165
SFR Definition 24.6. CRC0FLIP: CRC Bit Flip	166
SFR Definition 25.1. SPI0CFG: SPI0 Configuration	174
SFR Definition 25.2. SPI0CN: SPI0 Control	175
SFR Definition 25.3. SPI0CKR: SPI0 Clock Rate	176
SFR Definition 25.4. SPI0DAT: SPI0 Data	176
SFR Definition 26.1. SMB0CF: SMBus Clock/Configuration	186
SFR Definition 26.2. SMB0CN: SMBus Control	188
SFR Definition 26.3. SMB0ADR: SMBus Slave Address	191
SFR Definition 26.4. SMB0ADM: SMBus Slave Address Mask	191
SFR Definition 26.5. SMB0DAT: SMBus Data	192
SFR Definition 27.1. SCON0: Serial Port 0 Control	206
SFR Definition 27.2. SBUF0: Serial (UART0) Port Data Buffer	207
SFR Definition 28.1. CKCON: Clock Control	210
SFR Definition 28.2. TCON: Timer Control	215
SFR Definition 28.3. TMOD: Timer Mode	216
SFR Definition 28.4. TL0: Timer 0 Low Byte	217
SFR Definition 28.5. TL1: Timer 1 Low Byte	217
SFR Definition 28.6. TH0: Timer 0 High Byte	218
SFR Definition 28.7. TH1: Timer 1 High Byte	218

SFR Definition 28.8. TMR2CN: Timer 2 Control	222
SFR Definition 28.9. TMR2RLL: Timer 2 Reload Register Low Byte	223
SFR Definition 28.10. TMR2RLH: Timer 2 Reload Register High Byte	223
SFR Definition 28.11. TMR2L: Timer 2 Low Byte	224
SFR Definition 28.12. TMR2H Timer 2 High Byte	224
SFR Definition 29.1. PCA0CN: PCA0 Control	238
SFR Definition 29.2. PCA0MD: PCA0 Mode	239
SFR Definition 29.3. PCA0PWM: PCA0 PWM Configuration	240
SFR Definition 29.4. PCA0CPMn: PCA0 Capture/Compare Mode	241
SFR Definition 29.5. PCA0L: PCA0 Counter/Timer Low Byte	242
SFR Definition 29.6. PCA0H: PCA0 Counter/Timer High Byte	242
SFR Definition 29.7. PCA0CPLn: PCA0 Capture Module Low Byte	243
SFR Definition 29.8. PCA0CPHn: PCA0 Capture Module High Byte	243
C2 Register Definition 30.1. C2ADD: C2 Address	244
C2 Register Definition 30.3. REVID: C2 Revision ID	245
C2 Register Definition 30.2. DEVICEID: C2 Device ID	245
C2 Register Definition 30.4. FPCTL: C2 Flash Programming Control	246
C2 Register Definition 30.5. FPDAT: C2 Flash Programming Data	246

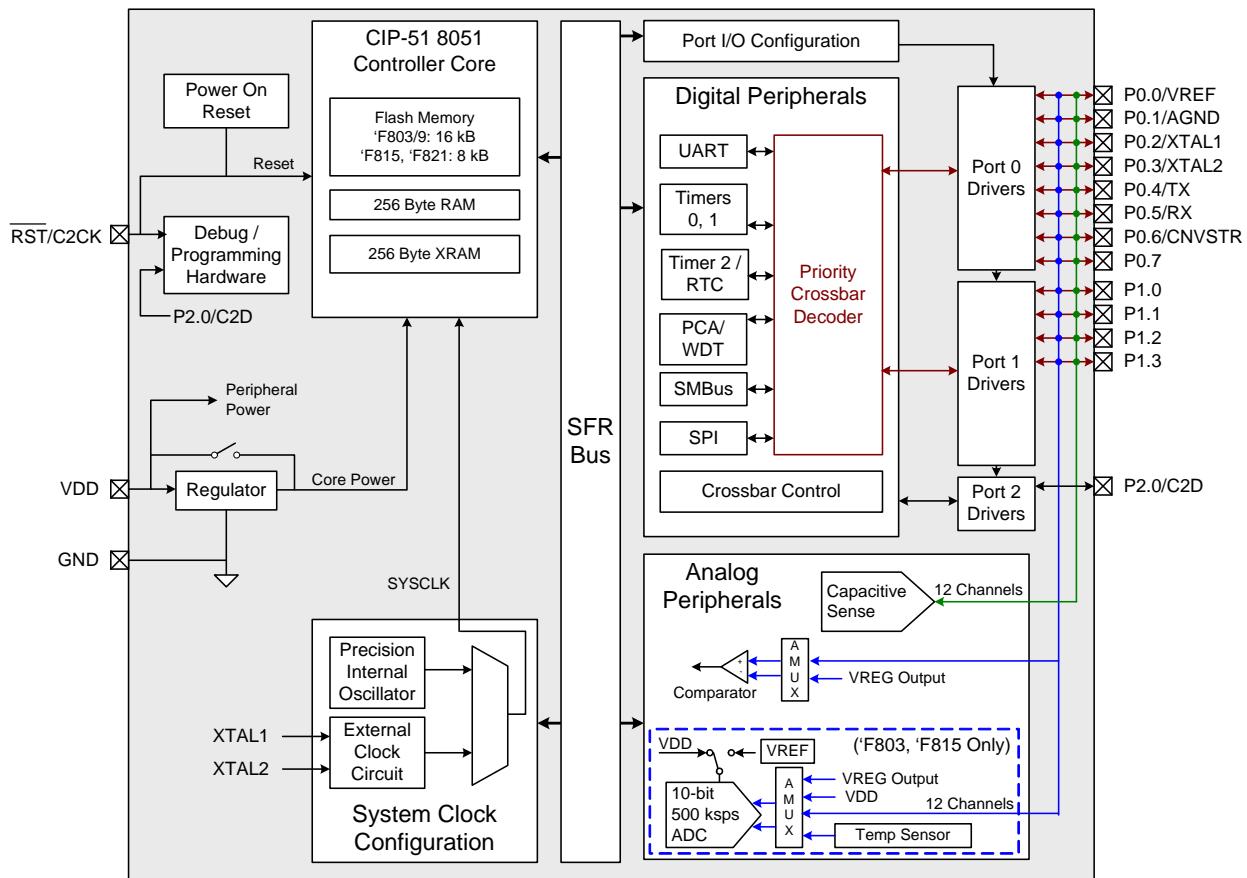


Figure 1.4. C8051F803, C8051F809, C8051F815, C8051F821 Block Diagram

3. Pin Definitions

Table 3.1. Pin Definitions for the C8051F80x-83x

Name	Pin QSOP-24	Pin QFN-20	Pin SOIC-16	Type	Description
GND	5	2	4		Ground. This ground connection is required. The center pad may optionally be connected to ground as well on the QFN-20 packages.
V _{DD}	6	3	5		Power Supply Voltage.
RST/ C2CK	7	4	6	D I/O	Device Reset. Open-drain output of internal POR or V _{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 10 µs.
				D I/O	Clock signal for the C2 Debug Interface.
P2.0/ C2D	8	5	7	D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
				D I/O	Bi-directional data signal for the C2 Debug Interface. Shared with P2.0 on 20-pin packaging and P2.4 on 24-pin packaging.
P0.0/ VREF	4	1	3	D I/O or A In	Port 0.0.
				A In	External VREF input.
P0.1	3	20	2	D I/O or A In	Port 0.1.
P0.2/ XTAL1	2	19	1	D I/O or A In	Port 0.2.
				A In	External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/ XTAL2	23	18	16	D I/O or A In	Port 0.3.
				A I/O or D In	External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	22	17	15	D I/O or A In	Port 0.4.

5. QSOP-24 Package Specifications

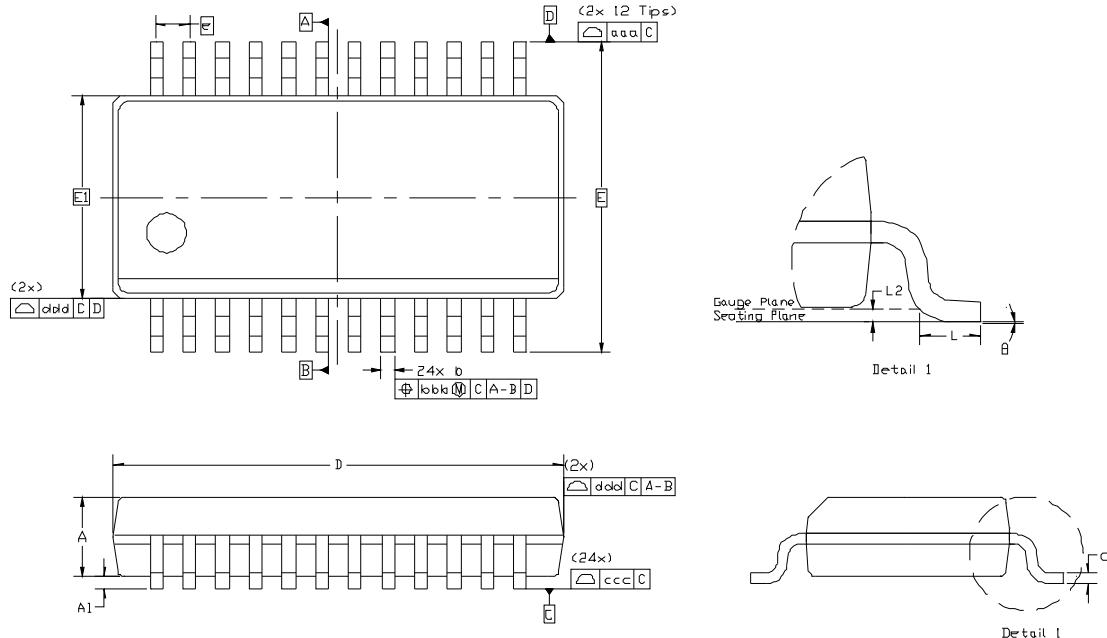


Figure 5.1. QSOP-24 Package Drawing

Table 5.1. QSOP-24 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.75	L	0.40	—	1.27
A1	0.10	—	0.25	L2		0.25 BSC	
b	0.20	—	0.30	θ	0°	—	8°
c	0.10	—	0.25	aaa		0.20	
D		8.65 BSC		bbb		0.18	
E		6.00 BSC		ccc		0.10	
E1		3.90 BSC		ddd		0.10	
e		0.635 BSC					

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

C8051F80x-83x

SFR Definition 8.2. ADC0H: ADC0 Data Word MSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBE

Bit	Name	Function
7:0	ADC0H[7:0]	ADC0 Data Word High-Order Bits. For AD0LJST = 0: Bits 7–2 will read 000000b. Bits 1–0 are the upper 2 bits of the 10-bit ADC0 Data Word. For AD0LJST = 1: Bits 7–0 are the most-significant bits of the 10-bit ADC0 Data Word. Note: In 8-bit mode AD0LJST is ignored, and ADC0H holds the 8-bit data word.

SFR Definition 8.3. ADC0L: ADC0 Data Word LSB

Bit	7	6	5	4	3	2	1	0
Name	ADC0L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xBD

Bit	Name	Function
7:0	ADC0L[7:0]	ADC0 Data Word Low-Order Bits. For AD0LJST = 0: Bits 7–0 are the lower 8 bits of the 10-bit Data Word. For AD0LJST = 1: Bits 7–6 are the lower 2 bits of the 10-bit Data Word. Bits 5–0 will always read 0. Note: In 8-bit mode AD0LJST is ignored, and ADC0L will read back 0000000b.

12.1. Comparator Multiplexer

C8051F80x-83x devices include an analog input multiplexer to connect Port I/O pins to the comparator inputs. The Comparator0 inputs are selected in the CPT0MX register (SFR Definition 12.3). The CMX0P3–CMX0P0 bits select the Comparator0 positive input; the CMX0N3–CMX0N0 bits select the Comparator0 negative input. **Important Note About Comparator Inputs:** The Port pins selected as comparator inputs should be configured as analog inputs in their associated Port configuration register, and configured to be skipped by the Crossbar (for details on Port configuration, see Section “23.6. Special Function Registers for Accessing and Configuring Port I/O” on page 152).

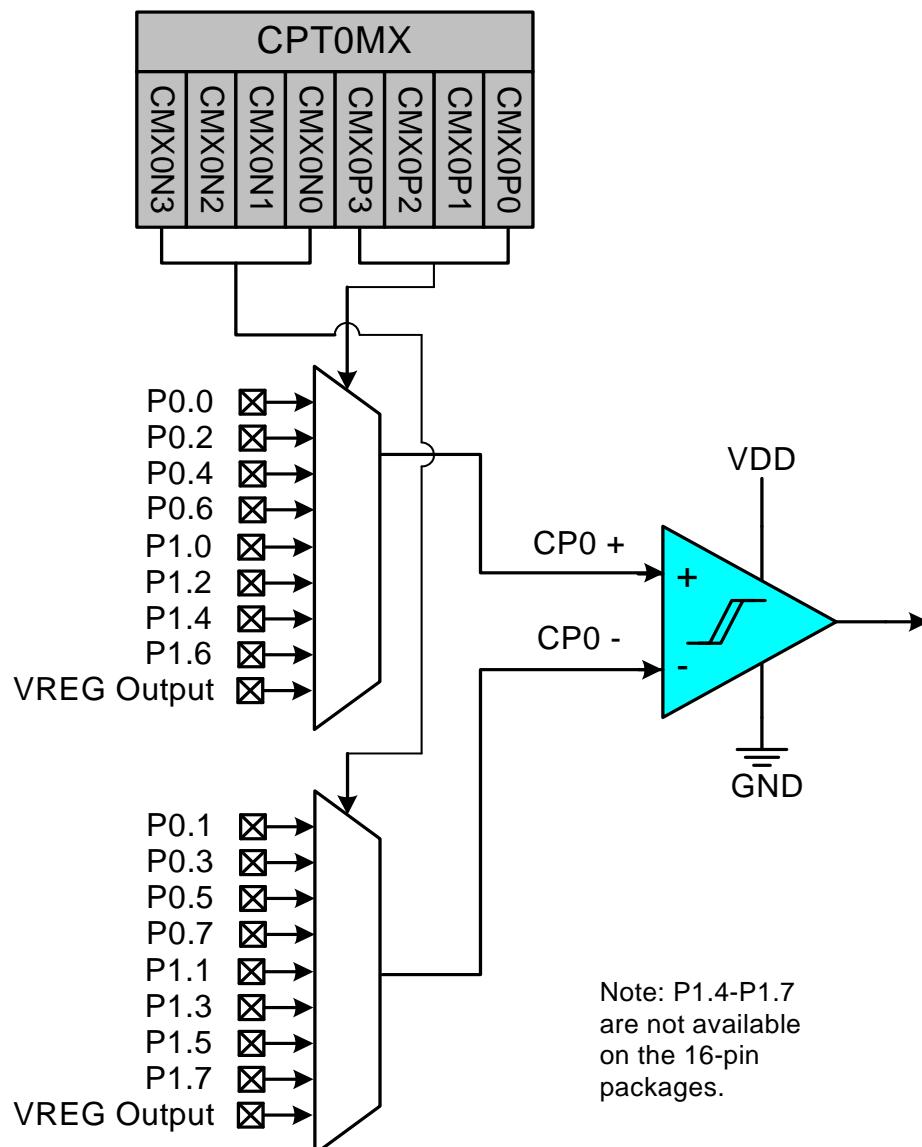
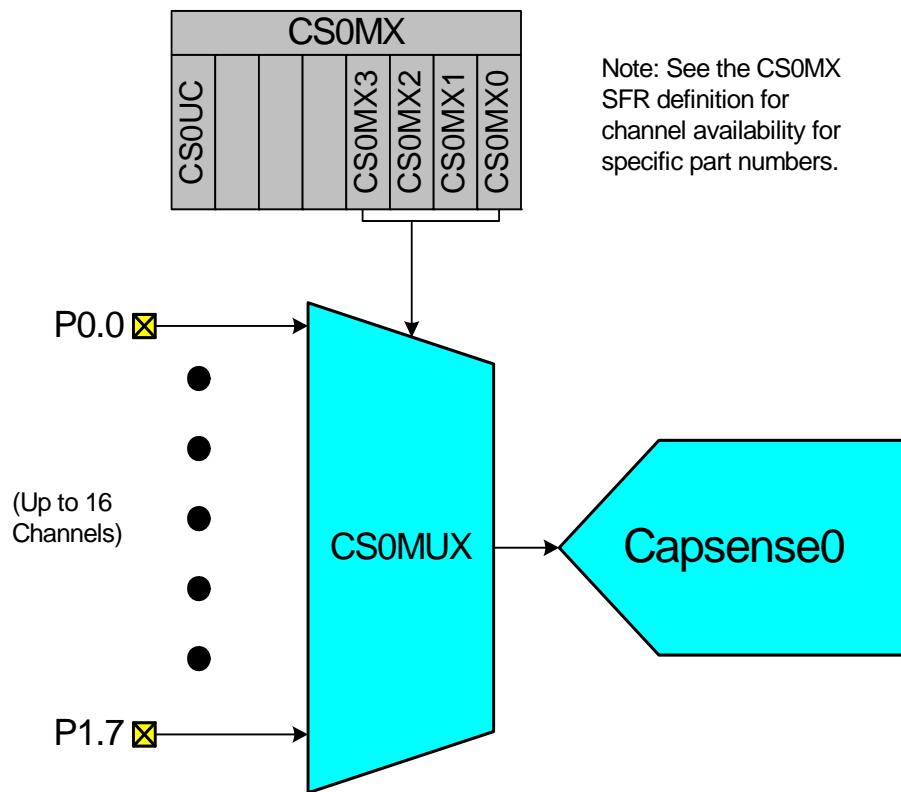


Figure 12.3. Comparator Input Multiplexer Block Diagram

13.6. Capacitive Sense Multiplexer

The input multiplexer can be controlled through two methods. The CS0MX register can be written to through firmware, or the register can be configured automatically using the modules auto-scan functionality (see “13.3. Automatic Scanning”).



C8051F80x-83x

SFR Definition 23.2. XBR1: Port I/O Crossbar Register 1

Bit	7	6	5	4	3	2	1	0
Name	WEAKPUD	XBARE	T1E	T0E	ECIE		PCA0ME[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE2

Bit	Name	Function
7	WEAKPUD	Port I/O Weak Pullup Disable. 0: Weak Pullups enabled (except for Ports whose I/O are configured for analog mode). 1: Weak Pullups disabled.
6	XBARE	Crossbar Enable. 0: Crossbar disabled. 1: Crossbar enabled.
5	T1E	T1 Enable. 0: T1 unavailable at Port pin. 1: T1 routed to Port pin.
4	T0E	T0 Enable. 0: T0 unavailable at Port pin. 1: T0 routed to Port pin.
3	ECIE	PCA0 External Counter Input Enable. 0: ECI unavailable at Port pin. 1: ECI routed to Port pin.
2	Unused	Read = 0b; Write = Don't Care.
1:0	PCA0ME[1:0]	PCA Module I/O Enable Bits. 00: All PCA I/O unavailable at Port pins. 01: CEX0 routed to Port pin. 10: CEX0, CEX1 routed to Port pins. 11: CEX0, CEX1, CEX2 routed to Port pins.

23.5. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMATCH registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMATCH registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (P0MATCH & P0MASK) or if (P1 & P1MASK) does not equal (P1MATCH & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode, such as IDLE or SUSPEND. See the Interrupts and Power Options chapters for more details on interrupt and wake-up sources.

26.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. Note that the position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

26.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 26.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the “data byte transferred” interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.

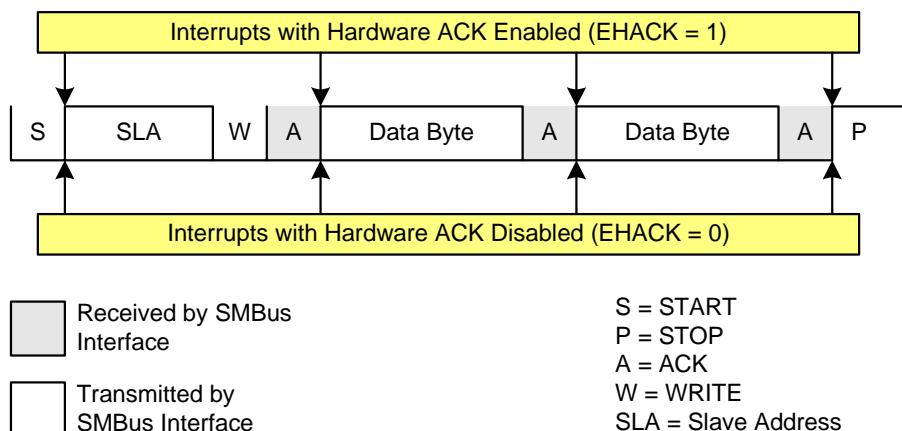


Figure 26.5. Typical Master Write Sequence

C8051F80x-83x

SFR Definition 28.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2		T2XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC8; Bit-Addressable

Bit	Name	Function
7	TF2H	Timer 2 High Byte Overflow Flag. Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	Timer 2 Low Byte Overflow Flag. Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	Timer 2 Low Byte Interrupt Enable. When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	Timer 2 Comparator Capture Enable. When set to 1, this bit enables Timer 2 Comparator Capture Mode. If TF2CEN is set, on a rising edge of the Comparator0 output the current 16-bit timer value in TMR2H:TMR2L will be copied to TMR2RH:TMR2RL. If Timer 2 interrupts are also enabled, an interrupt will be generated on this event.
3	T2SPLIT	Timer 2 Split Mode Enable. When this bit is set, Timer 2 operates as two 8-bit timers with auto-reload. 0: Timer 2 operates in 16-bit auto-reload mode. 1: Timer 2 operates as two 8-bit auto-reload timers.
2	TR2	Timer 2 Run Control. Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don't Care.
0	T2XCLK	Timer 2 External Clock Select. This bit selects the external clock source for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: System clock divided by 12. 1: External clock divided by 8 (synchronized with SYSCLK when not in suspend).

29.3.6. 16-Bit Pulse Width Modulator Mode

A PCA module may be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8-bit through 15-bit) PWM modes. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the 16-bit counter overflows, CEXn is asserted low. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register.

The duty cycle of the PWM output signal can be varied by writing to an “Auto-Reload” Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0. This synchronous update feature allows software to asynchronously write a new PWM high time, which will then take effect on the following PWM period.

For backwards-compatibility with the 16-bit PWM mode available on other devices, the PWM duty cycle can also be changed without using the “Auto-Reload” register. To output a varying duty cycle without using the “Auto-Reload” register, new value writes should be synchronized with PCA CCFn match interrupts. Match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a 16-bit comparator match (rising edge) occurs. The CF flag in PCA0CN can be used to detect the overflow (falling edge). The duty cycle for 16-Bit PWM Mode is given by Equation 29.4.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(65536 - \text{PCA0CPn})}{65536}$$

Equation 29.4. 16-Bit PWM Duty Cycle

Using Equation 29.4, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

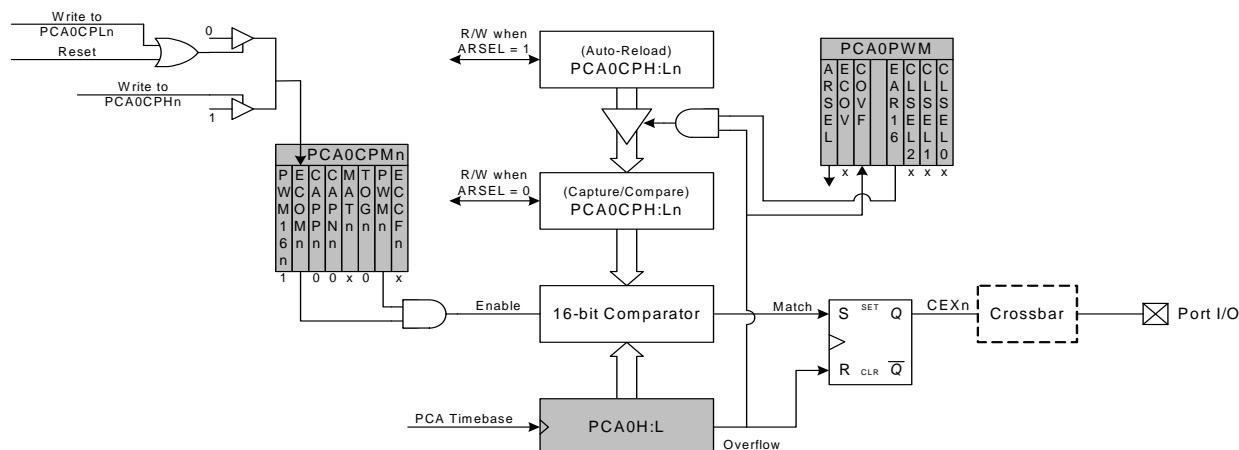


Figure 29.10. PCA 16-Bit PWM Mode

SFR Definition 29.2. PCA0MD: PCA0 Mode

Bit	7	6	5	4	3	2	1	0
Name	CIDL	WDTE	WDLCK		CPS2	CPS1	CPS0	ECF
Type	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

SFR Address = 0xD9

Bit	Name	Function
7	CIDL	PCA Counter/Timer Idle Control. Specifies PCA behavior when CPU is in idle mode. 0: PCA continues to function normally while the system controller is in Idle mode. 1: PCA operation is suspended while the system controller is in idle mode.
6	WDTE	Watchdog Timer Enable. If this bit is set, PCA Module 2 is used as the watchdog timer. 0: Watchdog Timer disabled. 1: PCA Module 2 enabled as Watchdog Timer.
5	WDLCK	Watchdog Timer Lock. This bit locks/unlocks the Watchdog Timer Enable. When WDLCK is set, the Watchdog Timer may not be disabled until the next system reset. 0: Watchdog Timer Enable unlocked. 1: Watchdog Timer Enable locked.
4	Unused	Read = 0b, Write = Don't care.
3:1	CPS[2:0]	PCA Counter/Timer Pulse Select. These bits select the timebase source for the PCA counter 000: System clock divided by 12 001: System clock divided by 4 010: Timer 0 overflow 011: High-to-low transitions on ECI (max rate = system clock divided by 4) 100: System clock 101: External clock divided by 8 (synchronized with the system clock) 11x: Reserved
0	ECF	PCA Counter/Timer Overflow Interrupt Enable. This bit sets the masking of the PCA Counter/Timer Overflow (CF) interrupt. 0: Disable the CF interrupt. 1: Enable a PCA Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.
Note: When the WDTE bit is set to 1, the other bits in the PCA0MD register cannot be modified. To change the contents of the PCA0MD register, the Watchdog Timer must first be disabled.		

C8051F80x-83x

SFR Definition 29.3. PCA0PWM: PCA0 PWM Configuration

Bit	7	6	5	4	3	2	1	0
Name	ARSEL	ECOV	COVF		EAR16	CLSEL[1:0]		
Type	R/W	R/W	R/W	R	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF7

Bit	Name	Function									
7	ARSEL	Auto-Reload Register Select. This bit selects whether to read and write the normal PCA capture/compare registers (PCA0CPn), or the Auto-Reload registers at the same SFR addresses. This function is used to define the reload value for 9-bit through 15-bit PWM mode and 16-bit PWM mode. In all other modes, the Auto-Reload registers have no function. 0: Read/Write Capture/Compare Registers at PCA0CPHn and PCA0CPLn. 1: Read/Write Auto-Reload Registers at PCA0CPHn and PCA0CPLn.									
6	ECOV	Cycle Overflow Interrupt Enable. This bit sets the masking of the Cycle Overflow Flag (COVF) interrupt. 0: COVF will not generate PCA interrupts. 1: A PCA interrupt will be generated when COVF is set.									
5	COVF	Cycle Overflow Flag. This bit indicates an overflow of the nth bit (n= 9 through 15) of the main PCA counter (PCA0). The specific bit used for this flag depends on the setting of the CLSEL bits. The bit can be set by hardware or software, but must be cleared by software. 0: No overflow has occurred since the last time this bit was cleared. 1: An overflow has occurred since the last time this bit was cleared.									
4	Unused	Read = 0b; Write = Don't care.									
3	EAR16	16-Bit PWM Auto-Reload Enable. This bit controls the Auto-Reload feature in 16-bit PWM mode, which loads the PCA0CPn capture/compare registers with the values from the Auto-Reload registers at the same SFR addresses on an overflow of the PCA counter (PCA0). This setting affects all PCA channels that are configured to use 16-bit PWM mode. 0: 16-bit PWM mode Auto-Reload is disabled. This default setting is backwards-compatible with the 16-bit PWM mode available on other devices. 1: 16-bit PWM mode Auto-Reload is enabled.									
2:0	CLSEL[2:0]	Cycle Length Select. When 16-bit PWM mode is not selected, these bits select the length of the PWM cycle, from 8 to 15 bits. This affects all channels configured for PWM which are not using 16-bit PWM mode. These bits are ignored for individual channels configured to 16-bit PWM mode. <table border="1"><tr><td>000: 8 bits.</td><td>011: 11 bits.</td><td>110: 14 bits.</td></tr><tr><td>001: 9 bits.</td><td>100: 12 bits.</td><td>111: 15 bits.</td></tr><tr><td>010: 10 bits.</td><td>101: 13 bits.</td><td></td></tr></table>	000: 8 bits.	011: 11 bits.	110: 14 bits.	001: 9 bits.	100: 12 bits.	111: 15 bits.	010: 10 bits.	101: 13 bits.	
000: 8 bits.	011: 11 bits.	110: 14 bits.									
001: 9 bits.	100: 12 bits.	111: 15 bits.									
010: 10 bits.	101: 13 bits.										

SFR Definition 29.7. PCA0CPLn: PCA0 Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPL0 = 0xFB, PCA0CPL1 = 0xE9, PCA0CPL2 = 0xEB

Bit	Name	Function
7:0	PCA0CPn[7:0]	PCA Capture Module Low Byte. The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n. This register address also allows access to the low byte of the corresponding PCA channel's auto-reload value for 9-bit through 15-bit PWM mode and 16-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.

Note: A write to this register will clear the module's ECOMn bit to a 0.

SFR Definition 29.8. PCA0CPHn: PCA0 Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPH0 = 0xFC, PCA0CPH1 = 0xEA, PCA0CPH2 = 0xEC

Bit	Name	Function
7:0	PCA0CPn[15:8]	PCA Capture Module High Byte. The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n. This register address also allows access to the high byte of the corresponding PCA channel's auto-reload value for 9-bit through 15-bit PWM mode and 16-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.

Note: A write to this register will set the module's ECOMn bit to a 1.

C2 Register Definition 30.4. FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	FPCTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0x02

Bit	Name	Function
7:0	FPCTL[7:0]	C2 Flash Programming Control Register. This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 30.5. FPDAT: C2 Flash Programming Data

Bit	7	6	5	4	3	2	1	0
Name	FPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xBF

Bit	Name	Function
7:0	FPDAT[7:0]	C2 Flash Programming Data Register. This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.
	Code	Command
	0x06	Flash Block Read
	0x07	Flash Block Write
	0x08	Flash Page Erase
	0x03	Device Erase

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 1.0

- Updated Electrical Specification Tables to reflect production characterization data.
- Added Minimum SYSCLK specification for writing or erasing Flash.
- Added caution for going into suspend with wake source active (Section 20.3)
- Corrected VDM0CN reset values to "Varies".
- Removed mention of IDAC in Pinout table.