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Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f820-gm

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Figure 5.2. QSOP-24 PCB Land Pattern

Table 5.2. QSOP-24 PCB Land Pattern Dimensions

Dimension	Min	Мах		
С	5.20	5.30		
E	0.635 BSC			
Х	0.30	0.40		
Y	1.50	1.60		

Notes: General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This land pattern design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

- **4.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 5. The stencil thickness should be 0.125 mm (5 mils).
- 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

- 7. A No-Clean, Type-3 solder paste is recommended.
- 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



Table 7.10. Power Management Electrical Characteristics

 V_{DD} = 1.8 to 3.6 V; T_A = -40 to +85 °C unless otherwise specified. Use factory-calibrated settings.

Parameter	Conditions	Min	Тур	Max	Units
Idle Mode Wake-Up Time		2		3	SYSCLKs
Suspend Mode Wake-up Time		_	500		ns

Table 7.11. Temperature Sensor Electrical Characteristics

 V_{DD} = 3.0 V, -40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Тур	Мах	Units			
Linearity	1	[_ '	1	[_]	°C			
Slope		[2.43		mV/°C			
Slope Error*	1	[±45		µV/°C			
Offset	Temp = 0 °C	['	873		mV			
Offset Error*	Temp = 0 °C	[14.5		mV			
*Note: Represents one standard dev	Note: Represents one standard deviation from the mean.							

Table 7.12. Voltage Reference Electrical Characteristics

 V_{DD} = 1.8 to 3.6 V; -40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Тур	Max	Units				
Internal High Speed Reference (REFSL[1:0] = 11)									
Output Voltage	25 °C ambient	1.55	1.65	1.75	V				
Turn-on Time		—	_	1.7	μs				
Supply Current		—	180	_	μA				
	External Reference (REF0E = 0)	•							
Input Voltage Range		0	—	V _{DD}					
Input Current	Sample Rate = 500 ksps; VREF = 3.0 V		7	_	μA				



SFR Definition 10.1. REF0CN: Voltage Reference Control

Bit	7	6	5	4	3	2	1	0
Name			REFGND	REFSL		TEMPE	BIASE	
Туре	R	R	R/W	R/W	R/W	R/W	R/W	R
Reset	0	0	0	1	0	0	0	0

SFR Address = 0xD1

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don't Care.
5	REFGND	Analog Ground Reference.
		Selects the ADC0 ground reference.
		0: The ADC0 ground reference is the GND pin.
		1: The ADC0 ground reference is the P0.1/AGND pin.
4:3	REFSL	Voltage Reference Select.
		Selects the ADC0 voltage reference.
		00: The ADC0 voltage reference is the P0.0/VREF pin.
		01: The ADC0 voltage reference is the VDD pin.
		10: The ADC0 voltage reference is the internal 1.8 V digital supply voltage.
		11: The ADC0 voltage reference is the internal 1.65 V high speed voltage reference.
2	TEMPE	Temperature Sensor Enable.
		Enables/Disables the internal temperature sensor.
		0: Temperature Sensor Disabled.
		1: Temperature Sensor Enabled.
1	BIASE	Internal Analog Bias Generator Enable Bit.
		0: Internal Bias Generator off.
		1: Internal Bias Generator on.
0	Unused	Read = 0b; Write = Don't Care.



16. In-System Device Identification

The C8051F80x-83x has SFRs that identify the device family and derivative. These SFRs can be read by firmware at runtime to determine the capabilities of the MCU that is executing code. This allows the same firmware image to run on MCUs with different memory sizes and peripherals, and dynamically changing functionality to suit the capabilities of that MCU.

In order for firmware to identify the MCU, it must read three SFRs. HWID describes the MCU's family, DERIVID describes the specific derivative within that device family, and REVID describes the hardware revision of the MCU.

SFR Definition 16.1. HWID: Hardware Identification Byte

Bit	7	6	5	4	3	2	1	0
Name	e HWID[7:0]							
Туре	R	R	R	R	R	R	R	R
Reset	0	0	1	0	0	0	1	1

SFR Address = 0xB5

Bit	Name	Description
7:0	HWID[7:0]	Hardware Identification Byte.
		Describes the MCU family. 0x23: Devices covered in this document (C8051F80x-83x)



SFR Definition 18.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	ECP0	EADC0	EPCA0	EWADC0	EMAT	ESMB0
Туре	W	W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE6

Name	Function
Reserved	Must write 0.
Reserved	Reserved.
	Must write 0.
ECP0	Enable Comparator0 (CP0) Interrupt.
	0: Disable CP0 interrupts.
	1: Enable interrupt requests generated by the CP0RIF and CP0FIF flags.
EADC0	Enable ADC0 Conversion Complete Interrupt.
	This bit sets the masking of the ADC0 Conversion Complete interrupt.
	1: Enable interrupt requests generated by the AD0INT flag.
EPCA0	Enable Programmable Counter Array (PCA0) Interrupt.
	This bit sets the masking of the PCA0 interrupts.
	1: Enable interrupt requests generated by PCA0.
EWADC0	Enable Window Comparison ADC0 interrupt.
	This bit sets the masking of ADC0 Window Comparison interrupt.
	1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).
EMAT	Enable Port Match Interrupts.
	This bit sets the masking of the Port Match event interrupt.
	1: Enable interrupt requests generated by a Port Match.
ESMB0	Enable SMBus (SMB0) Interrupt.
	This bit sets the masking of the SMB0 interrupt.
	1: Enable interrupt requests generated by SMB0.
	Reserved Reserved ECP0 EADC0 EPCA0 EWADC0



SFR Definition 18.5. EIP1: Extended Interrupt Priority 1

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	PCP0	PPCA0	PADC0	PWADC0	PMAT	PSMB0
Туре	W	W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF3

Bit	Name	Function
7:6	Reserved	Must write 0.
5	PCP0	Comparator0 (CP0) Interrupt Priority Control.
		This bit sets the priority of the CP0 rising edge or falling edge interrupt.
		0: CP0 interrupt set to low priority level.
		1: CP0 interrupt set to high priority level.
4	PPCA0	Programmable Counter Array (PCA0) Interrupt Priority Control.
		This bit sets the priority of the PCA0 interrupt.
		0: PCA0 interrupt set to low priority level.
		1: PCAU interrupt set to high priority level.
3	PADC0	ADC0 Conversion Complete Interrupt Priority Control.
		This bit sets the priority of the ADC0 Conversion Complete interrupt.
		0: ADC0 Conversion Complete interrupt set to low priority level.
	-	1: ADC0 Conversion Complete interrupt set to high priority level.
2	PWADC0	ADC0 Window Comparator Interrupt Priority Control.
		This bit sets the priority of the ADC0 Window interrupt.
		0: ADC0 Window interrupt set to low priority level.
		1: ADCU window interrupt set to high priority level.
1	PMAT	Port Match Interrupt Priority Control.
		This bit sets the priority of the Port Match Event interrupt.
		0: Port Match interrupt set to low priority level.
		1: Port Match Interrupt set to high priority level.
0	PSMB0	SMBus (SMB0) Interrupt Priority Control.
		This bit sets the priority of the SMB0 interrupt.
		U: SMBU interrupt set to low priority level.
		1: SIVIBU INTERRUPT SET to high priority level.



SFR Definition 18.7. IT01CF: INT0/INT1 Configuration

Bit	7	6	5	4	3	2	1	0	
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]			
Туре	R/W		R/W		R/W	R/W			
Reset	0	0	0	0	0	0 0		1	

SFR Address = 0xE4

Bit	Name	Function
7	IN1PL	INT1 Polarity. 0: INT1 input is active low. 1: INT1 input is active high.
6:4	IN1SL[2:0]	INT1 Port Pin Selection Bits. These bits select which Port pin is assigned to INT1. Note that this pin assignment is independent of the Crossbar; INT1 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7
3	INOPL	INTO Polarity. 0: INTO input is active low. 1: INTO input is active high.
2:0	IN0SL[2:0]	INTO Port Pin Selection Bits. These bits select which Port pin is assigned to INTO. Note that this pin assignment is independent of the Crossbar; INTO will monitor the assigned Port pin without disturb- ing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7



is set. While the SPI0 master transfers data to a slave on the MOSI line, the addressed SPI slave device simultaneously transfers the contents of its shift register to the SPI master on the MISO line in a full-duplex operation. Therefore, the SPIF flag serves as both a transmit-complete and receive-data-ready flag. The data byte received from the slave is transferred MSB-first into the master's shift register. When a byte is fully shifted into the register, it is moved to the receive buffer where it can be read by the processor by reading SPI0DAT.

When configured as a master, SPI0 can operate in one of three different modes: multi-master mode, 3-wire single-master mode, and 4-wire single-master mode. The default, multi-master mode is active when NSS-MD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In this mode, NSS is an input to the device, and is used to disable the master SPI0 when another master is accessing the bus. When NSS is pulled low in this mode, MSTEN (SPI0CN.6) and SPIEN (SPI0CN.0) are set to 0 to disable the SPI master device, and a Mode Fault is generated (MODF, SPI0CN.5 = 1). Mode Fault will generate an interrupt if enabled. SPI0 must be manually re-enabled in software under these circumstances. In multi-master systems, devices will typically default to being slave devices while they are not acting as the system master device. In multi-master mode, slave devices can be addressed individually (if needed) using general-purpose I/O pins. Figure 25.2 shows a connection diagram between two master devices in multiple-master mode.

3-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. In this mode, NSS is not used, and is not mapped to an external port pin through the crossbar. Any slave devices that must be addressed in this mode should be selected using general-purpose I/O pins. Figure 25.3 shows a connection diagram between a master device in 3-wire master mode and a slave device.

4-wire single-master mode is active when NSSMD1 (SPI0CN.3) = 1. In this mode, NSS is configured as an output pin, and can be used as a slave-select signal for a single SPI device. In this mode, the output value of NSS is controlled (in software) with the bit NSSMD0 (SPI0CN.2). Additional slave devices can be addressed using general-purpose I/O pins. Figure 25.4 shows a connection diagram for a master device in 4-wire master mode and two slave devices.



Figure 25.2. Multiple-Master Mode Connection Diagram



Figure 25.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram



SFR Definition 26.2. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER	TXMODE	STA	STO	ACKRQ	ARBLOST	ACK	SI
Туре	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC0; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER	SMBus Master/Slave Indicator. This read-only bit indicates when the SMBus is operating as a master.	0: SMBus operating in slave mode. 1: SMBus operating in master mode.	N/A
6	TXMODE	SMBus Transmit Mode Indicator. This read-only bit indicates when the SMBus is operating as a transmitter.	0: SMBus in Receiver Mode. 1: SMBus in Transmitter Mode.	N/A
5	STA	SMBus Start Flag.	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO	SMBus Stop Flag.	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pend- ing (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmit- ted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ	SMBus Acknowledge Request.	0: No Ack requested 1: ACK requested	N/A
2	ARBLOST	SMBus Arbitration Lost Indicator.	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK	SMBus Acknowledge.	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI	SMBus Interrupt Flag. This bit is set by hardware under the conditions listed in Table 15.3. SI must be cleared by software. While SI is set, SCL is held low and the SMBus is stalled.	0: No interrupt pending 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event.1: Force interrupt.



26.5. SMBus Transfer Modes

The SMBus interface may be configured to operate as master and/or slave. At any particular time, it will be operating in one of the following four modes: Master Transmitter, Master Receiver, Slave Transmitter, or Slave Receiver. The SMBus interface enters Master Mode any time a START is generated, and remains in Master Mode until it loses an arbitration or generates a STOP. An SMBus interrupt is generated at the end of all SMBus byte frames. Note that the position of the ACK interrupt when operating as a receiver depends on whether hardware ACK generation is enabled. As a receiver, the interrupt for an ACK occurs **before** the ACK with hardware ACK generation disabled, and **after** the ACK when hardware ACK generation is enabled. As a transmitter, interrupts occur **after** the ACK, regardless of whether hardware ACK generation is enabled or not.

26.5.1. Write Sequence (Master)

During a write sequence, an SMBus master writes data to a slave device. The master in this transfer will be a transmitter during the address byte, and a transmitter during all data bytes. The SMBus interface generates the START condition and transmits the first byte containing the address of the target slave and the data direction bit. In this case the data direction bit (R/W) will be logic 0 (WRITE). The master then transmits one or more bytes of serial data. After each byte is transmitted, an acknowledge bit is generated by the slave. The transfer is ended when the STO bit is set and a STOP is generated. Note that the interface will switch to Master Receiver Mode if SMB0DAT is not written following a Master Transmitter interrupt. Figure 26.5 shows a typical master write sequence. Two transmit data bytes are shown, though any number of bytes may be transmitted. Notice that all of the "data byte transferred" interrupts occur **after** the ACK cycle in this mode, regardless of whether hardware ACK generation is enabled.







 Table 26.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)

	Valu	es l	Rea	d			Val V	lues Vrit	e to	tus ected
Mode	Status Vector	Current SMbus State				Typical Response Options	STA	STO	ACK	Next Sta Vector Exp
	1110	0	0	Х	A master START was gener- ated.	Load slave address + R/W into SMB0DAT.	0	0	Х	1100
					A master data or address byte	Set STA to restart transfer.	1	0	Х	1110
tter		0	0	0	was transmitted; NACK received.	Abort transfer.	0	1	Х	—
insmit						Load next data byte into SMB0DAT.	0	0	Х	1100
Tra	1100					End transfer with STOP.	0	1	Х	—
laster	1100	0	0	1	A master data or address byte was transmitted; ACK received.	End transfer with STOP and start another transfer.	1	1	Х	—
2						Send repeated START.	1	0	Х	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT).	0	0	Х	1000
						Acknowledge received byte; Read SMB0DAT.	0	0	1	1000
						Send NACK to indicate last byte, and send STOP.	0	1	0	—
iver						Send NACK to indicate last byte, and send STOP followed by START.	1	1	0	1110
Recei	1000	1	0	x	A master data byte was	Send ACK followed by repeated START.	1	0	1	1110
Aaster						Send NACK to indicate last byte, and send repeated START.	1	0	0	1110
~						Send ACK and switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	1	1100
						Send NACK and switch to Mas- ter Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	0	1100



Table 26.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)(Continued)

	Valu	es F	Rea	d			Val V	ues Vrit	e to	tus ected
Mode	Status Vector	ACKRQ	ARBLOST	ACK	Current SMbus State	Typical Response Options	STA	STO	ACK	Next Sta Vector Exp
er.		0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	Х	0001
smitt€	0100	0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	Х	0100
e Tran		0	1	Х	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	Х	0001
Slav	0101	0	х	Х	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	Х	
						If Write, Acknowledge received address	0	0	1	0000
		1	0	Х	received; ACK requested.	If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	
	0010					If Write, Acknowledge received address	0	0	1	0000
<u>șiver</u>		1	1	х	Lost arbitration as master; slave address + R/W received;	If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
ece					ACK requested.	NACK received address.	0	0	0	_
lave R						Reschedule failed transfer; NACK received address.	1	0	0	1110
S	0001	0	0	х	A STOP was detected while addressed as a Slave Trans- mitter or Slave Receiver.	Clear STO.	0	0	Х	
		1	1	Х	Lost arbitration while attempt- ing a STOP.	No action required (transfer complete/aborted).	0	0	0	
	0000	1	0	х	A slave byte was received;	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
					Aon lequested.	NACK received byte.	0	0	0	_
on	0010	0	1	x	Lost arbitration while attempt-	Abort failed transfer.	0	0	Х	
diti	0010		'	~	ing a repeated START.	Reschedule failed transfer.	1	0	Х	1110
Cor	0001	0	1	х	Lost arbitration due to a	Abort failed transfer.	0	0	Х	_
ror					detected STOP.	Reschedule failed transfer.	1	0	Х	1110
Ш	0000	1	1	x	Lost arbitration while transmit-	Abort failed transfer.	0	0	0	
Bus	0000		1	~	ting a data byte as master.	Reschedule failed transfer.	1	0	0	1110



Table 26.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1)(Continued)

0	Valu	es F	Rea	d			Val V	lues Vrite	sto e	atus bected
€PoM	Status Vector	ACKRQ	ARBLOST	ACK	Current SMbus State	Typical Response Options	STA	STO	ACK	Next Sta Vector Exp
er.		0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	Х	0001
smitt€	0100	0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	Х	0100
e Tran		0	1	х	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	Х	0001
Slav	0101	0	х	х	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	Х	
		0	0	v	A slave address + R/W was	If Write, Set ACK for first data byte.	0	0	1	0000
		U	U	^	received; ACK sent.	If Read, Load SMB0DAT with data byte	0	0	Х	0100
	0010				Lost arbitration as master:	If Write, Set ACK for first data byte.	0	0	1	0000
iver		0	1	Х	slave address + R/W received; ACK sent.	If Read, Load SMB0DAT with data byte	0	0	Х	0100
ece						Reschedule failed transfer	1	0	Х	1110
Slave R	0001	0	0	х	A STOP was detected while addressed as a Slave Trans- mitter or Slave Receiver.	Clear STO.	0	0	Х	
		0	1	х	Lost arbitration while attempt- ing a STOP.	No action required (transfer complete/aborted).	0	0	0	
	0000	0	0	v		Set ACK for next data byte; Read SMB0DAT.	0	0	1	0000
	0000	U	0	^	A slave byle was received.	Set NACK for next data byte; Read SMB0DAT.	0	0	0	0000
ion	0010	0	1	x	Lost arbitration while attempt-	Abort failed transfer.	0	0	Х	
Jdit	0010	Ŭ			ing a repeated START.	Reschedule failed transfer.	1	0	Х	1110
So	0001	0	1	х	Lost arbitration due to a	Abort failed transfer.	0	0	Х	—
ror			Ľ		detected STOP.	Reschedule failed transfer.	1	0	Х	1110
ц	0000	0	1	x	Lost arbitration while transmit-	Abort failed transfer.	0	0	Х	
Buŝ		0			ting a data byte as master.	Reschedule failed transfer.	1	0	Х	1110



27.3. Multiprocessor Communications

9-Bit UART mode supports multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the MCE0 bit (SCON0.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic 1 (RB80 = 1) signifying an address byte has been received. In the UART interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its MCE0 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their MCE0 bits set and do not generate interrupts on the reception of the following data byte(s) addressed slave resets its MCE0 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).



Figure 27.6. UART Multi-Processor Mode Interconnect Diagram



			Fre	quency: 24.5 M	IHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select) ¹	T1M ¹	Timer 1 Reload Value (hex)				
	230400	-0.32%	106	SYSCLK	XX ²	1	0xCB				
E	115200	-0.32%	212	SYSCLK	XX	1	0x96				
ror Sc	57600	0.15%	426	SYSCLK	XX	1	0x2B				
Υ Ψ	28800	-0.32%	848	SYSCLK/4	01	0	0x96				
ц я	14400	0.15%	1704	SYSCLK/12	00	0	0xB9				
YS	9600	-0.32%	2544	SYSCLK/12	00	0	0x96				
– v	2400	-0.32%	10176	SYSCLK/48	10	0	0x96				
	1200	0.15%	20448	SYSCLK/48	10	0	0x2B				
Notes: 1. 2.	 Notes: 1. SCA1–SCA0 and T1M bit definitions can be found in Section 28.1. 2. X = Don't care. 										

Table 27.1. Timer Settings for Standard Baud RatesUsing The Internal 24.5 MHz Oscillator

Table 27.2. Timer Settings for Standard Baud RatesUsing an External 22.1184 MHz Oscillator

			Frequ	uency: 22.1184	MHz		
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select) ¹	T1M ¹	Timer 1 Reload Value (hex)
	230400	0.00%	96	SYSCLK	XXZ	1	0xD0
εĸ	115200	0.00%	192	SYSCLK	XX	1	0xA0
ror Dsc	57600	0.00%	384	SYSCLK	XX	1	0x40
K f al C	28800	0.00%	768	SYSCLK / 12	00	0	0xE0
CL	14400	0.00%	1536	SYSCLK / 12	00	0	0xC0
ΥS xte	9600	0.00%	2304	SYSCLK / 12	00	0	0xA0
ŚШ	2400	0.00%	9216	SYSCLK / 48	10	0	0xA0
	1200	0.00%	18432	SYSCLK / 48	10	0	0x40
۲. ۲	230400	0.00%	96	EXTCLK / 8	11	0	0xFA
ror Sc	115200	0.00%	192	EXTCLK / 8	11	0	0xF4
K f I O	57600	0.00%	384	EXTCLK / 8	11	0	0xE8
CL rna	28800	0.00%	768	EXTCLK / 8	11	0	0xD0
ΥS	14400	0.00%	1536	EXTCLK / 8	11	0	0xA0
s =	9600	0.00%	2304	EXTCLK / 8	11	0	0x70
Mateau		-					

Notes:

1. SCA1–SCA0 and T1M bit definitions can be found in Section 28.1.

2. X = Don't care.



SFR Definition 28.2. TCON: Timer Control

Bit	7	6	5	4	3	2	1	0
Name	e TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Rese	t 0	0	0	0	0	0	0	0
SFR Address = 0x88: Bit-Addressable								
Bit	Name	Function						
7	TF1	Timer 1 Overflow Flag.						
		Set to 1 by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.						
6	TR1	TR1Timer 1 Run Control.Timer 1 is enabled by setting this bit to 1.						
5	TF0	Timer 0 Overflow Flag.						
	Set to 1 by hardware when Timer 0 overflows. This flag can be cleared but is automatically cleared when the CPU vectors to the Timer 0 interrur routine.							
4	TR0	Timer 0 Run Control.						
		Timer 0 is enabled by setting this bit to 1.						
3	IE1	External Interrupt 1. This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine in edge-triggered mode.						
2	IT1	 IT1 Interrupt 1 Type Select. This bit selects whether the configured /INT1 interrupt will be edge or level sensitive /INT1 is configured active low or high by the IN1PL bit in the IT01CF register (see SFR Definition 18.7). 0: /INT1 is level triggered. 1: /INT1 is edge triggered. 						
1	IE0	External Interrupt 0.						
		This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine in edge-triggered mode.						
0	IT0	Interrupt 0 Type Select.						

 This bit selects whether the configured INT0 interrupt will be edge or level sensitive.

 INT0 is configured active low or high by the IN0PL bit in register IT01CF (see SFR Definition 18.7).

 0: INT0 is level triggered.

 1: INT0 is edge triggered.



28.2.3. Comparator 0 Capture Mode

The capture mode in Timer 2 allows Comparator 0 rising edges to be captured with the timer clocking from the system clock or the system clock divided by 12. Timer 2 capture mode is enabled by setting TF2CEN to 1 and T2SPLIT to 0.

When capture mode is enabled, a capture event will be generated on every Comparator 0 rising edge. When the capture event occurs, the contents of Timer 2 (TMR2H:TMR2L) are loaded into the Timer 2 reload registers (TMR2RLH:TMR2RLL) and the TF2H flag is set (triggering an interrupt if Timer 2 interrupts are enabled). By recording the difference between two successive timer capture values, the Comparator 0 period can be determined with respect to the Timer 2 clock. The Timer 2 clock should be much faster than the capture clock to achieve an accurate reading.

This mode allows software to determine the time between consecutive Comparator 0 rising edges, which can be used for detecting changes in the capacitance of a capacitive switch, or measuring the frequency of a low-level analog signal.



Figure 28.6. Timer 2 Capture Mode Block Diagram





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