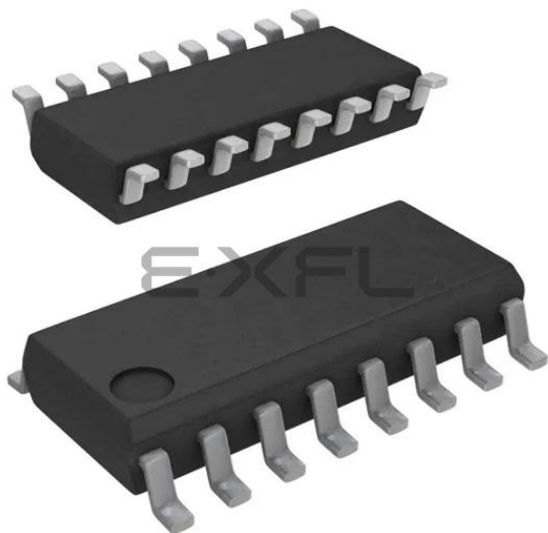




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Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f826-gs

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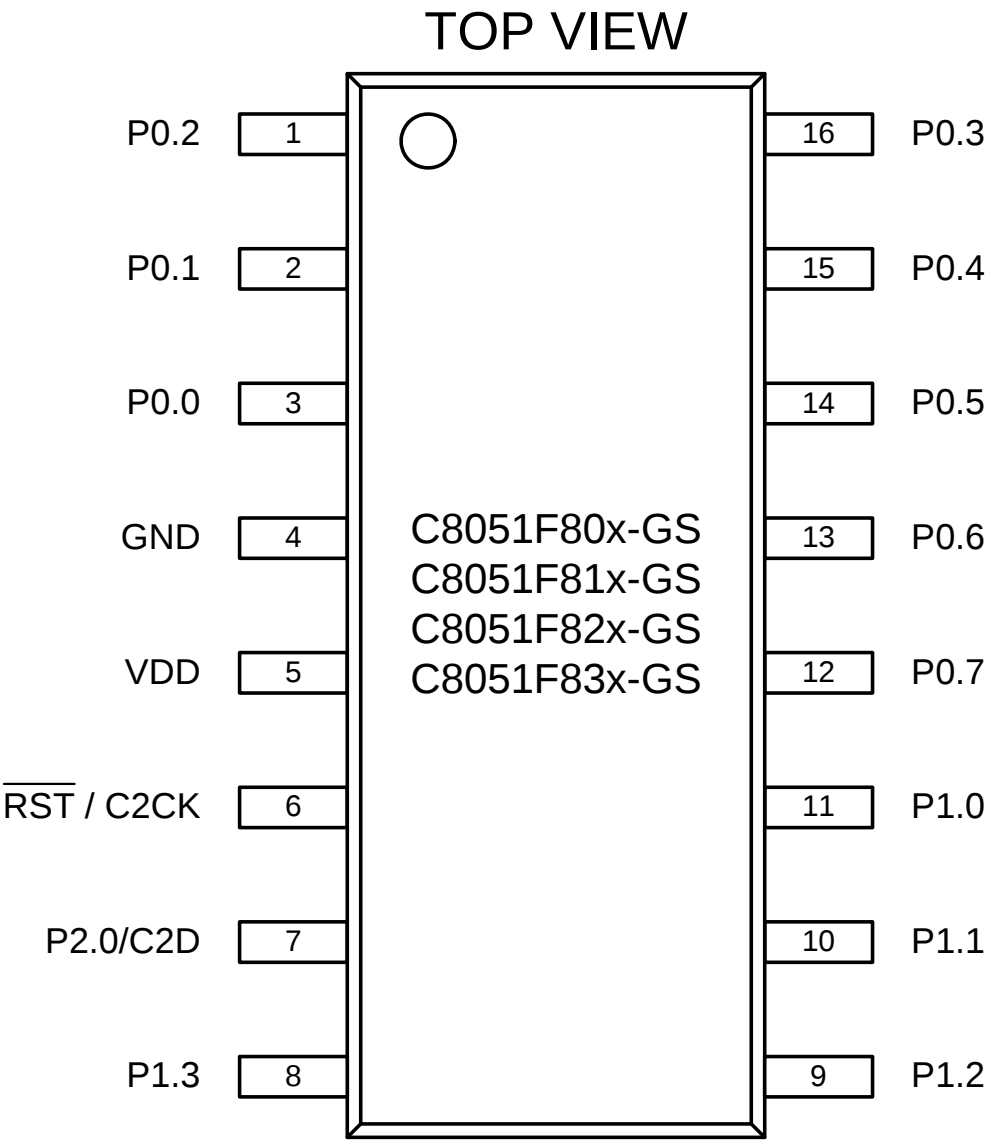


Figure 3.3. SOIC-16 Pinout Diagram (Top View)

C8051F80x-83x

Table 7.6. Flash Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Flash Size (Note 1)	C8051F80x and C8051F810/1 C8051F812/3/4/5/6/7/8/9 and C8051F82x C8051F830/1/2/3/4/5		16384 8192 4096		bytes bytes bytes
Endurance (Erase/Write)		10000	—	—	cycles
Erase Cycle Time	25 MHz Clock	15	20	26	ms
Write Cycle Time	25 MHz Clock	15	20	26	μs
Clock Speed during Flash Write/Erase Operations		1	—	—	MHz
Note: Includes Security Lock Byte.					

Table 7.7. Internal High-Frequency Oscillator Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V; $T_A = -40$ to $+85$ °C unless otherwise specified. Use factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	IFCN = 11b	24	24.5	25	MHz
Oscillator Supply Current	25 °C, $V_{DD} = 3.0$ V, OSCICN.7 = 1, OCSICN.5 = 0	—	350	650	μA

Table 7.8. Capacitive Sense Electrical Characteristics

$V_{DD} = 1.8$ to 3.6 V; $T_A = -40$ to $+85$ °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Conversion Time	Single Conversion	26	38	50	μs
Capacitance per Code		—	1	—	fF
External Capacitive Load		—	—	45	pF
Quantization Noise ¹	RMS	—	3	—	fF
	Peak-to-Peak	—	20	—	fF
Supply Current	CS module bias current, 25 °C	—	40	60	μA
	CS module alone, maximum code output, 25 °C	—	75	105	μA
	Wake-on-CS Threshold ² , 25 °C	—	150	165	μA
Notes: 1. RMS Noise is equivalent to one standard deviation. Peak-to-peak noise encompasses ± 3.3 standard deviations. 2. Includes only current from regulator, CS module, and MCU in suspend mode.					

10.1. External Voltage References

To use an external voltage reference, REFSL[1:0] should be set to 00. Bypass capacitors should be added as recommended by the manufacturer of the external voltage reference.

10.2. Internal Voltage Reference Options

A 1.65 V high-speed reference is included on-chip. The high speed internal reference is selected by setting REFSL[1:0] to 11. When selected, the high speed internal reference will be automatically enabled on an as-needed basis by ADC0.

For applications with a non-varying power supply voltage, using the power supply as the voltage reference can provide ADC0 with added dynamic range at the cost of reduced power supply noise rejection. To use the 1.8 to 3.6 V power supply voltage (V_{DD}) or the 1.8 V regulated digital supply voltage as the reference source, REFSL[1:0] should be set to 01 or 10, respectively.

10.3. Analog Ground Reference

To prevent ground noise generated by switching digital logic from affecting sensitive analog measurements, a separate analog ground reference option is available. When enabled, the ground reference for ADC0 is taken from the P0.1/AGND pin. Any external sensors sampled by ADC0 should be referenced to the P0.1/AGND pin. The separate analog ground reference option is enabled by setting REFGND to 1. Note that when using this option, P0.1/AGND must be connected to the same potential as GND.

10.4. Temperature Sensor Enable

The TEMPE bit in register REF0CN enables the temperature sensor. While disabled, the temperature sensor defaults to a high impedance state and any ADC0 measurements performed on the sensor result in meaningless data.

SFR Definition 13.1. CS0CN: Capacitive Sense Control

Bit	7	6	5	4	3	2	1	0
Name	CS0EN		CS0INT	CS0BUSY	CS0CMPEN			CS0CMPF
Type	R/W	R	R/W	R/W	R/W	R	R	R
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xB0; Bit-Addressable

Bit	Name	Description
7	CS0EN	CS0 Enable. 0: CS0 disabled and in low-power mode. 1: CS0 enabled and ready to convert.
6	Unused	Read = 0b; Write = Don't care
5	CS0INT	CS0 Interrupt Flag. 0: CS0 has not completed a data conversion since the last time CS0INT was cleared. 1: CS0 has completed a data conversion. This bit is not automatically cleared by hardware.
4	CS0BUSY	CS0 Busy. Read: 0: CS0 conversion is complete or a conversion is not currently in progress. 1: CS0 conversion is in progress. Write: 0: No effect. 1: Initiates CS0 conversion if CS0CM[2:0] = 000b, 110b, or 111b.
3	CS0CMPEN	CS0 Digital Comparator Enable Bit. Enables the digital comparator, which compares accumulated CS0 conversion output to the value stored in CS0THH:CS0THL. 0: CS0 digital comparator disabled. 1: CS0 digital comparator enabled.
2:1	Unused	Read = 00b; Write = Don't care
0	CS0CMPF	CS0 Digital Comparator Interrupt Flag. 0: CS0 result is smaller than the value set by CS0THH and CS0THL since the last time CS0CMPF was cleared. 1: CS0 result is greater than the value set by CS0THH and CS0THL since the last time CS0CMPF was cleared.

Note: On waking from suspend mode due to a CS0 greater-than comparator event, the CS0CN register should be accessed only after at least two system clock cycles have elapsed.

Table 14.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
XRL direct, #data	Exclusive-OR immediate to direct byte	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through Carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through Carry	1	1
SWAP A	Swap nibbles of A	1	1
Data Transfer			
MOV A, Rn	Move Register to A	1	1
MOV A, direct	Move direct byte to A	2	2
MOV A, @Ri	Move indirect RAM to A	1	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, A	Move A to Register	1	1
MOV Rn, direct	Move direct byte to Register	2	2
MOV Rn, #data	Move immediate to Register	2	2
MOV direct, A	Move A to direct byte	2	2
MOV direct, Rn	Move Register to direct byte	2	2
MOV direct, direct	Move direct byte to direct byte	3	3
MOV direct, @Ri	Move indirect RAM to direct byte	2	2
MOV direct, #data	Move immediate to direct byte	3	3
MOV @Ri, A	Move A to indirect RAM	1	2
MOV @Ri, direct	Move direct byte to indirect RAM	2	2
MOV @Ri, #data	Move immediate to indirect RAM	2	2
MOV DPTR, #data16	Load DPTR with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A, @A+PC	Move code byte relative PC to A	1	3
MOVX A, @Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri, A	Move A to external data (8-bit address)	1	3
MOVX A, @DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR, A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange Register with A	1	1
XCH A, direct	Exchange direct byte with A	2	2
XCH A, @Ri	Exchange indirect RAM with A	1	2
XCHD A, @Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear Carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set Carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement Carry	1	1
CPL bit	Complement direct bit	2	2

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SFR Definition 14.3. SP: Stack Pointer

Bit	7	6	5	4	3	2	1	0
Name	SP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	1	1

SFR Address = 0x81

Bit	Name	Function
7:0	SP[7:0]	Stack Pointer. The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 14.4. ACC: Accumulator

Bit	7	6	5	4	3	2	1	0
Name	ACC[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE0; Bit-Addressable

Bit	Name	Function
7:0	ACC[7:0]	Accumulator. This register is the accumulator for arithmetic operations.

Table 17.2. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
P1MAT	0xED	P1 Match	152
P1MDIN	0xF2	Port 1 Input Mode Configuration	156
P1MDOUT	0xA5	Port 1 Output Mode Configuration	156
P1SKIP	0xD5	Port 1 Skip	157
P2	0xA0	Port 2 Latch	157
P2MDOUT	0xA6	Port 2 Output Mode Configuration	158
PCA0CN	0xD8	PCA Control	238
PCA0CPH0	0xFC	PCA Capture 0 High	243
PCA0CPH1	0xEA	PCA Capture 1 High	243
PCA0CPH2	0xEC	PCA Capture 2 High	243
PCA0CPL0	0xFB	PCA Capture 0 Low	243
PCA0CPL1	0xE9	PCA Capture 1 Low	243
PCA0CPL2	0xEB	PCA Capture 2 Low	243
PCA0CPM0	0xDA	PCA Module 0 Mode Register	241
PCA0CPM1	0xDB	PCA Module 1 Mode Register	241
PCA0CPM2	0xDC	PCA Module 2 Mode Register	241
PCA0H	0xFA	PCA Counter High	242
PCA0L	0xF9	PCA Counter Low	242
PCA0MD	0xD9	PCA Mode	239
PCA0PWM	0xF7	PCA PWM Configuration	240
PCON	0x87	Power Control	122
PSCTL	0x8F	Program Store R/W Control	118
PSW	0xD0	Program Status Word	91
REF0CN	0xD1	Voltage Reference Control	62
REG0CN	0xC9	Voltage Regulator Control	64
REVID	0xB6	Revision ID	96
RSTSRC	0xEF	Reset Source Configuration/Status	128

18.1. MCU Interrupt Sources and Vectors

The C8051F80x-83x MCUs support 15 interrupt sources. Software can simulate an interrupt by setting an interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in Table 18.1. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

18.1.1. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP or EIP1) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate, given in Table 18.1.

18.1.2. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

SFR Definition 18.3. EIE1: Extended Interrupt Enable 1

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	ECP0	EADC0	EPCA0	EWADC0	EMAT	ESMB0
Type	W	W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xE6

Bit	Name	Function
7	Reserved	Must write 0.
6	Reserved	Reserved. Must write 0.
5	ECP0	Enable Comparator0 (CP0) Interrupt. This bit sets the masking of the CP0 rising edge or falling edge interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the CP0RIF and CP0FIF flags.
4	EADC0	Enable ADC0 Conversion Complete Interrupt. This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the AD0INT flag.
3	EPCA0	Enable Programmable Counter Array (PCA0) Interrupt. This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
2	EWADC0	Enable Window Comparison ADC0 interrupt. This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (AD0WINT).
1	EMAT	Enable Port Match Interrupts. This bit sets the masking of the Port Match event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.
0	ESMB0	Enable SMBus (SMB0) Interrupt. This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

SFR Definition 18.7. IT01CF: INT0/INT1 Configuration

Bit	7	6	5	4	3	2	1	0
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
Type	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	0	0	1

SFR Address = 0xE4

Bit	Name	Function
7	IN1PL	INT1 Polarity. 0: $\overline{\text{INT1}}$ input is active low. 1: INT1 input is active high.
6:4	IN1SL[2:0]	INT1 Port Pin Selection Bits. These bits select which Port pin is assigned to $\overline{\text{INT1}}$. Note that this pin assignment is independent of the Crossbar; INT1 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7
3	IN0PL	INT0 Polarity. 0: $\overline{\text{INT0}}$ input is active low. 1: INT0 input is active high.
2:0	IN0SL[2:0]	INT0 Port Pin Selection Bits. These bits select which Port pin is assigned to $\overline{\text{INT0}}$. Note that this pin assignment is independent of the Crossbar; INT0 will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P0.6 111: Select P0.7

22. Oscillators and Clock Selection

C8051F80x-83x devices include a programmable internal high-frequency oscillator and an external oscillator drive circuit. The internal high-frequency oscillator can be enabled/disabled and calibrated using the OSCICN and OSCICL registers, as shown in Figure 22.1. The system clock can be sourced by the external oscillator circuit or the internal oscillator (default). The internal oscillator offers a selectable post-scaling feature, which is initially set to divide the clock by 8.

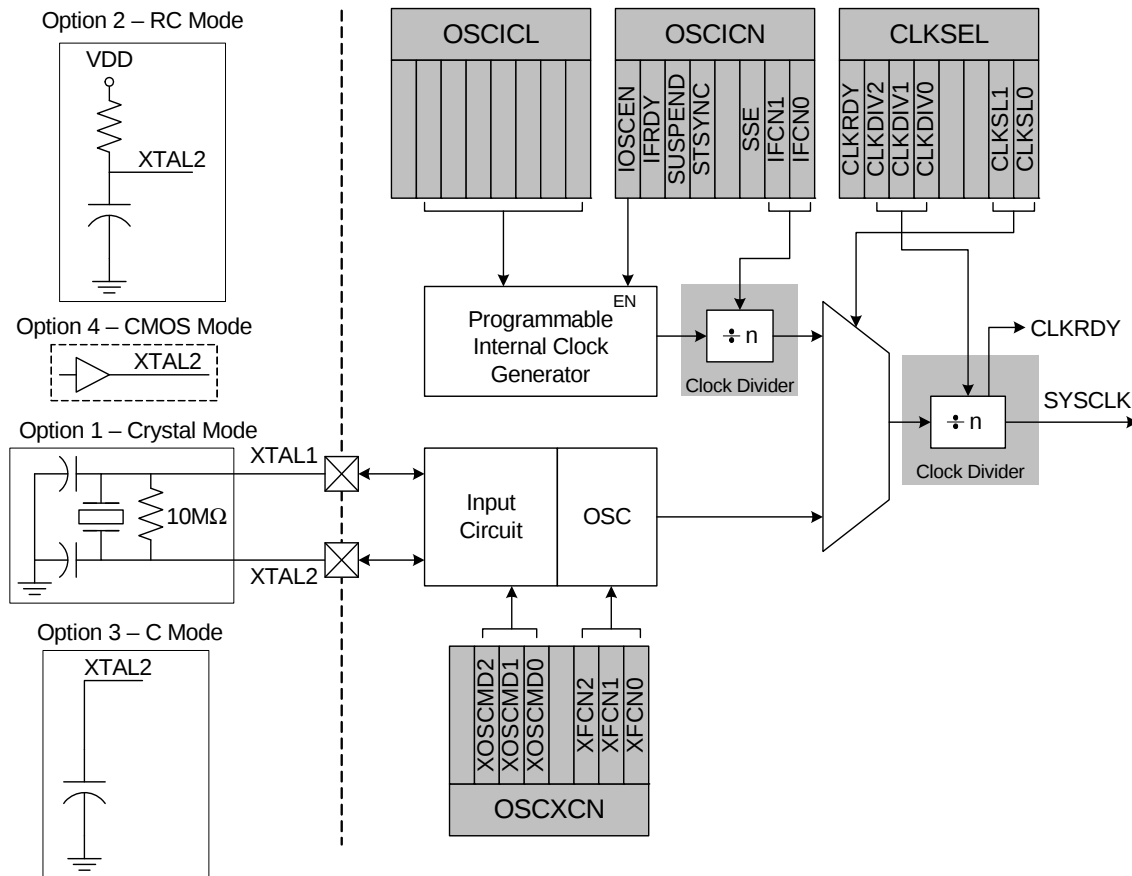


Figure 22.1. Oscillator Options

22.1. System Clock Selection

The system clock source for the MCU can be selected using the CLKSEL register. The clock selected as the system clock can be divided by 1, 2, 4, 8, 16, 32, 64, or 128. When switching between two clock divide values, the transition may take up to 128 cycles of the undivided clock source. The CLKRDY flag can be polled to determine when the new clock divide value has been applied. The clock divider must be set to "divide by 1" when entering Suspend mode. The system clock source may also be switched on-the-fly. The switchover takes effect after one clock period of the slower oscillator.

C8051F80x-83x

SFR Definition 22.1. CLKSEL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name	CLKRDY	CLKDIV[2:0]				CLKSEL[2:0]		
Type	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA9

Bit	Name	Function
7	CLKRDY	System Clock Divider Clock Ready Flag. 0: The selected clock divide setting has not been applied to the system clock. 1: The selected clock divide setting has been applied to the system clock.
6:4	CLKDIV	System Clock Divider Bits. Selects the clock division to be applied to the selected source (internal or external). 000: Selected clock is divided by 1. 001: Selected clock is divided by 2. 010: Selected clock is divided by 4. 011: Selected clock is divided by 8. 100: Selected clock is divided by 16. 101: Selected clock is divided by 32. 110: Selected clock is divided by 64. 111: Selected clock is divided by 128.
3	Unused	Read = 0b. Must write 0b.
2:0	CLKSEL[2:0]	System Clock Select. Selects the oscillator to be used as the undivided system clock source. 000: Internal Oscillator 001: External Oscillator All other values reserved.

SFR Definition 22.3. OSCICN: Internal H-F Oscillator Control

Bit	7	6	5	4	3	2	1	0
Name	IOSCEN	IFRDY	SUSPEND	STSYNC	SSE		IFCN[1:0]	
Type	R/W	R	R/W	R	R/W	R	R/W	
Reset	1	1	0	0	0	0	0	0

SFR Address = 0xB2

Bit	Name	Function
7	IOSCEN	Internal H-F Oscillator Enable Bit. 0: Internal H-F Oscillator Disabled. 1: Internal H-F Oscillator Enabled.
6	IFRDY	Internal H-F Oscillator Frequency Ready Flag. 0: Internal H-F Oscillator is not running at programmed frequency. 1: Internal H-F Oscillator is running at programmed frequency.
5	SUSPEND	Internal Oscillator Suspend Enable Bit. Setting this bit to logic 1 places the internal oscillator in SUSPEND mode. The internal oscillator resumes operation when one of the SUSPEND mode awakening events occurs.
4	STSYNC	Suspend Timer Synchronization Bit. This bit is used to indicate when it is safe to read and write the registers associated with the suspend wake-up timer. If a suspend wake-up source other than Timer 2 has brought the oscillator out of suspend mode, it make take up to three timer clocks before the timer can be read or written. 0: Timer 2 registers can be read safely. 1: Timer 2 register reads and writes should not be performed.
3	SSE	Spread Spectrum Enable. Spread spectrum enable bit. 0: Spread Spectrum clock dithering disabled. 1: Spread Spectrum clock dithering enabled.
2	Unused	Read = 0b; Write = Don't Care
1:0	IFCN[1:0]	Internal H-F Oscillator Frequency Divider Control Bits. 00: SYSCLK derived from Internal H-F Oscillator divided by 8. 01: SYSCLK derived from Internal H-F Oscillator divided by 4. 10: SYSCLK derived from Internal H-F Oscillator divided by 2. 11: SYSCLK derived from Internal H-F Oscillator divided by 1.

Port	P0								P1								P2
Pin Number	0	1	2	3	4	5	6	7	0	1	2	3	4 ¹	5 ¹	6 ¹	7 ¹	0
Special Function Signals	VREF	AGND	XTAL1	XTAL2			CNVSTR										
TX0																	
RX0																	
SCK																	
MISO																	
MOSI																	
NSS ²																	
SDA																	
SCL																	
CP0																	
CP0A																	
SYSCLK																	
CEX0																	
CEX1																	
CEX2																	
ECI																	
T0																	
T1																	
Pin Skip Settings	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	P0SKIP								P1SKIP								

In this example, the crossbar is configured to assign the UART TX0 and RX0 signals, the SPI signals, and the PCA signals. Note that the SPI signals are assigned as multiple signals, and there are no pins skipped using the P0SKIP or P1SKIP registers.

■ These boxes represent the port pins which are used by the peripherals in this configuration.

1st TX0 is assigned to P0.4
2nd RX0 is assigned to P0.5
3rd SCK, MISO, MOSI, and NSS are assigned to P0.0, P0.1, P0.2, and P0.3, respectively.
4th CEX0, CEX1, and CEX2 are assigned to P0.6, P0.7, and P1.0, respectively.

All unassigned pins can be used as GPIO or for other non-crossbar functions.

Notes:

1. P1.4-P1.7 are not available on 16-pin packages.
2. NSS is only pinned out when the SPI is in 4-wire mode.

Figure 23.5. Priority Crossbar Decoder Example 1—No Skipped Pins

SFR Definition 23.8. P0MDIN: Port 0 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Address = 0xF1

Bit	Name	Function
7:0	P0MDIN[7:0]	Analog Configuration Bits for P0.7–P0.0 (respectively). Port pins configured for analog mode have their weak pullup, digital driver, and digital receiver disabled. In order for the P0.n pin to be in analog mode, there MUST be a '1' in the Port Latch register corresponding to that pin. 0: Corresponding P0.n pin is configured for analog mode. 1: Corresponding P0.n pin is not configured for analog mode.

SFR Definition 23.9. P0MDOUT: Port 0 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P0MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xA4

Bit	Name	Function
7:0	P0MDOUT[7:0]	Output Configuration Bits for P0.7–P0.0 (respectively). These bits are ignored if the corresponding bit in register P0MDIN is logic 0. 0: Corresponding P0.n Output is open-drain. 1: Corresponding P0.n Output is push-pull.

SFR Definition 25.1. SPI0CFG: SPI0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Address = 0xA1

Bit	Name	Function
7	SPIBSY	SPI Busy. This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	Master Mode Enable. 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	SPI0 Clock Phase. 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	SPI0 Clock Polarity. 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	Slave Selected Flag. This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	NSS Instantaneous Pin Input. This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	Shift Register Empty (valid in slave mode only). This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when in Master Mode.
0	RXBMT	Receive Buffer Empty (valid in slave mode only). This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. RXBMT = 1 when in Master Mode.

Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 25.1 for timing parameters.

Table 25.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing (See Figure 25.8 and Figure 25.9)				
T_{MCKH}	SCK High Time	$1 \times T_{SYSCLK}$	—	ns
T_{MCKL}	SCK Low Time	$1 \times T_{SYSCLK}$	—	ns
T_{MIS}	MISO Valid to SCK Shift Edge	$1 \times T_{SYSCLK} + 20$	—	ns
T_{MIH}	SCK Shift Edge to MISO Change	0	—	ns
Slave Mode Timing (See Figure 25.10 and Figure 25.11)				
T_{SE}	NSS Falling to First SCK Edge	$2 \times T_{SYSCLK}$	—	ns
T_{SD}	Last SCK Edge to NSS Rising	$2 \times T_{SYSCLK}$	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	$4 \times T_{SYSCLK}$	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	$4 \times T_{SYSCLK}$	ns
T_{CKH}	SCK High Time	$5 \times T_{SYSCLK}$	—	ns
T_{CKL}	SCK Low Time	$5 \times T_{SYSCLK}$	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	$2 \times T_{SYSCLK}$	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	$2 \times T_{SYSCLK}$	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	$4 \times T_{SYSCLK}$	ns
T_{SLH}	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	$6 \times T_{SYSCLK}$	$8 \times T_{SYSCLK}$	ns
Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).				

overflow after 25 ms (and SMBTOE set), the Timer 3 interrupt service routine can be used to reset (disable and re-enable) the SMBus in the event of an SCL low timeout.

26.3.5. SCL High (SMBus Free) Timeout

The SMBus specification stipulates that if the SCL and SDA lines remain high for more than 50 μ s, the bus is designated as free. When the SMBFTE bit in SMB0CF is set, the bus will be considered free if SCL and SDA remain high for more than 10 SMBus clock source periods (as defined by the timer configured for the SMBus clock source). If the SMBus is waiting to generate a Master START, the START will be generated following this timeout. A clock source is required for free timeout detection, even in a slave-only implementation.

26.4. Using the SMBus

The SMBus can operate in both Master and Slave modes. The interface provides timing and shifting control for serial transfers; higher level protocol is determined by user software. The SMBus interface provides the following application-independent features:

- Byte-wise serial data transfers
- Clock signal generation on SCL (Master Mode only) and SDA data synchronization
- Timeout/bus error recognition, as defined by the SMB0CF configuration register
- START/STOP timing, detection, and generation
- Bus arbitration
- Interrupt generation
- Status information
- Optional hardware recognition of slave address and automatic acknowledgement of address/data

SMBus interrupts are generated for each data byte or slave address that is transferred. When hardware acknowledgement is disabled, the point at which the interrupt is generated depends on whether the hardware is acting as a data transmitter or receiver. When a transmitter (i.e., sending address/data, receiving an ACK), this interrupt is generated after the ACK cycle so that software may read the received ACK value; when receiving data (i.e., receiving address/data, sending an ACK), this interrupt is generated before the ACK cycle so that software may define the outgoing ACK value. If hardware acknowledgement is enabled, these interrupts are always generated after the ACK cycle. See Section 26.5 for more details on transmission sequences.

Interrupts are also generated to indicate the beginning of a transfer when a master (START generated), or the end of a transfer when a slave (STOP detected). Software should read the SMB0CN (SMBus Control register) to find the cause of the SMBus interrupt. The SMB0CN register is described in Section 26.4.2; Table 26.5 provides a quick SMB0CN decoding reference.

26.4.1. SMBus Configuration Register

The SMBus Configuration register (SMB0CF) is used to enable the SMBus Master and/or Slave modes, select the SMBus clock source, and select the SMBus timing and timeout options. When the ENSMB bit is set, the SMBus is enabled for all master and slave events. Slave events may be disabled by setting the INH bit. With slave events inhibited, the SMBus interface will still monitor the SCL and SDA pins; however, the interface will NACK all received addresses and will not generate any slave interrupts. When the INH bit is set, all slave events will be inhibited following the next START (interrupts will continue for the duration of the current transfer).

SFR Definition 29.7. PCA0CPLn: PCA0 Capture Module Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPL0 = 0xFB, PCA0CPL1 = 0xE9, PCA0CPL2 = 0xEB

Bit	Name	Function
7:0	PCA0CPn[7:0]	PCA Capture Module Low Byte. The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n. This register address also allows access to the low byte of the corresponding PCA channel's auto-reload value for 9-bit through 15-bit PWM mode and 16-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.

Note: A write to this register will clear the module's ECOMn bit to a 0.

SFR Definition 29.8. PCA0CPHn: PCA0 Capture Module High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0CPn[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Addresses: PCA0CPH0 = 0xFC, PCA0CPH1 = 0xEA, PCA0CPH2 = 0xEC

Bit	Name	Function
7:0	PCA0CPn[15:8]	PCA Capture Module High Byte. The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n. This register address also allows access to the high byte of the corresponding PCA channel's auto-reload value for 9-bit through 15-bit PWM mode and 16-bit PWM mode. The ARSEL bit in register PCA0PWM controls which register is accessed.

Note: A write to this register will set the module's ECOMn bit to a 1.